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Preprint

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Presented at the 35th IEEE Photovoltaic Specialists Conference
Honolulu, Hawaii
June 20-25, 2010

Conference Paper
NREL/CP-5200-47755
October 2010

Contract No. DE-AC36-08GO28308

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TEST-TO-FAILURE OF CRYSTALLINE SILICON MODULES

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ABSTRACT

Accelerated lifetime testing of five crystalline silicon module designs was carried out according to the Terrestrial Photovoltaic Module Accelerated Test-to-Failure Protocol. This protocol compares the reliability of various module constructions on a quantitative basis. The modules under test are subdivided into three accelerated lifetime testing paths: 85°C/85% relative humidity with system bias, thermal cycling between –40°C and 85°C, and a path that alternates between damp heat and thermal cycling. The most severe stressor is damp heat with system bias applied to simulate the voltages that modules experience when connected in an array. Positive 600 V applied to the active layer with respect to the grounded module frame accelerates corrosion of the silver grid fingers and degrades the silicon nitride antireflective coating on the cells. Dark I-V curve fitting indicates increased series resistance and saturation current around the maximum power point; however, an improvement in junction recombination characteristics is obtained. Severe shunt paths and cell-metallization interface failures are seen developing in the silicon cells as determined by electroluminescence, thermal imaging, and I-V curves in the case of negative 600 V bias applied to the active layer. Ability to withstand electrolytic corrosion, moisture ingress, and ion drift under system voltage bias are differentiated according to module design. The results are discussed in light of relevance to field failures.

INTRODUCTION

Passing International Electrotechnical Commission qualification tests such as IEC 61215 and IEC 61646 for crystalline and thin-film silicon PV modules, respectively, are important thresholds to demonstrate the ability of modules to withstand some extent of environmental exposure in the field. The pass/fail criteria provided by such certifications, however, do not go far in differentiating which module technologies are better, nor do they provide a measure of module reliability over 25 or more years in the field. To address this gap, NREL has proposed a Test-to-Failure (TTF) protocol that prescribes a series of accelerated environmental stresses [1]. The protocol's utility includes the following:

- Test new module technologies on a comparative basis in a highly accelerated manner, such as to rate the performance of new designs to an incumbent.
- Perform due diligence between various module technologies before large capital outlays for PV power plants are committed.
- Characterize potential performance and reliability problems for high-voltage, 600 V systems in the United States according to the National Electric Code (NEC) and 1500 V systems according to IEC 60038 for low-voltage direct current.
- Accelerate the onset of failure so that failure mechanisms can be studied, compared to field failures, and then be addressed.

While the measured performances of modules undergoing this protocol do not yet translate to a module lifetime in the field, the information obtained is nevertheless useful for the comparison of the reliability of different module technologies in an accelerated manner and on a quantitative basis.

Corresponding to the IEC 61215 2nd Ed., Sec. 10.11, thermal cycling is applied in the TTF to accelerate diurnal solar thermal loading of the extreme conditions seen in the high desert. Extreme temperatures of rooftop modules in hot deserts may reach as high as 95°C during the day depending on the ventilation [2]. One-sun current is applied when the module is above 25°C to replicate the current concentrations and localized heating that would evolve from partially disbonded interconnects in fielded modules. BP Solar has concluded that 500 cycles is sufficient to warrantee performance for 25 years [3].

Damp heat tests are carried out to accelerate the hydrolytic and corrosive action of hot, humid environments. Rates for degradation by mechanisms such as discoloration and gridline metallization corrosion differ in 85°C/85% relative humidity (RH). The correspondence of damage per unit time at this stress condition to a fielded module may vary widely depending on activation energies for the process. Six days in test may correspond to 20 years in Miami, FL, USA for some degradation processes [4], but the 1000 h 85°C 85% RH test may not be sufficient to represent 20 years of fielding in hot humid environments for other degradation mechanisms, depending on the activation energy of the process [5, 6]. The level of stress to apply to a module in damp heat to match a particular field environment is not yet clear.

The majority of field failures in the collective inventory of modules deployed for the long term described in the literature are often not from arrays reaching the 600 V system voltage limit of the U.S. according to NEC, and even fewer are from those reaching the 1500 V IEC limit for low-voltage systems. While the Jet Propulsion Laboratories (JPL) studied and sought to implement the system bias factor in the Block Program [7], it was not implemented in IEC qualification testing because it was considered too strenuous [1]. Electrical bias has however been seen to remain an important cause of problems in recent history, leading to damage in fielded amorphous silicon and CdTe modules [8-10], attributed to Na

migration and corrosion of the SnO_2:F, the transparent conductive oxide layer [11]. Also, in high-efficiency, back-contact crystalline-silicon cells, a significant but readily reversible polarization affect was seen when a negative charge that developed over the cell surface in positively biased strings because of leakage current through the face glass led to annihilation of minority carriers in the n-type base. Specifying the positive terminal of the string as the grounded conductor has since mitigated this problem [12].

Wohlgemuth and coworkers found application of system voltage in damp heat to be an excellent way to quickly evaluate modules for rate of moisture ingress and determine potential failures in high-voltage arrays [8]. Considering these results from fielded and accelerated-tested modules, the TTF stresses the module at the rated system voltage of a module under 85°C/85% RH damp heat.

Finally, modules are alternated between damp heat and thermal cycling to represent the combined stress [1]. We can conceive of scenarios whereby high moisture can weaken interfaces, which will be further aggravated by the thermomechanical fatigue.

In this work, we report on the application of the TTF protocol as it was postulated in the document "Terrestrial Photovoltaic Module Accelerated Test-to-Failure Protocol" [1]. Some modules continue to be under test at this writing. We quantify the degradation under the accelerated testing and discuss some of the resulting failure mechanisms associated with the various stresses applied. We will also discuss factors that differentiate the performance of the modules.

EXPERIMENT

Five commercially available mc-Si flat-plate module designs in the 160–225 W range (six modules for test and two controls for each design) were subjected to the protocol sequences as defined in Table 1. All module designs that were tested passed either IEC 61215 or UL 1703 qualification testing. Four of the five were from producers in the top 20 manufactures in terms of megawatts sold in 2009. The samples were divided among four test sequences. Group (A), the controls; (B) 1000 hours of 85°C/85% RH with one each in positive or negative 600 V bias, DH(+), DH(-) respectively, to the shorted module leads and grounded frame; (C) 200 thermal cycles (TC) between –40° and 85°C with standard test condition (STC) peak current applied above 25°C; and (D) an alternating (Alt) sequence between tests (B) and (C), whereby the modules go through the damp heat stress first. The current that flows through each module under bias is monitored continuously over the course of the damp heat test.

At the start of the test, the modules were exposed to 5 kWh/m^2 light soaking. The initial power of each module (round 0) is defined from the measurement after the light soak. The modules were visually inspected; tested for dielectric withstand and wet insulation resistance, dark I-V; and imaged thermally, optically, and by electroluminescence. The module testing was performed with the IEC 60904-3 class A global spectrum with continuous light source to ISO standards. Current and power results measured on the stressed modules were normalized to the control modules. The range of power measured for the control modules was $\pm$2%. Measurements were repeated and compared against the failure criteria after each round of the TTF protocol.

		Sequence							
		A. Control		B. Damp Heat with Bias		C. Thermal Cycling		D. Alternating B/C	
		5 kW hrs/m^2 light soak							
Round	1			DH+	DH-	TC	TC	DH+	DH -
	2			DH+	DH-	TC	TC	TC	TC
	3			DH+	DH-	TC	TC	DH+	DH -
	4			DH+	DH-	TC	TC	TC	TC
	…								
	15			DH+	DH-	TC	TC	DH+	DH -

• DH refers to 1000 hrs 85°C and 85% relative humidity, IEC 61215 Ed. 2 sec. 10.13
• DH+(-) indicates +(-) voltage bias of 600 V or module's rated system voltage (whichever is greater) on shorted module leads with respect to grounded frame
• TC refers to 200 cycles between -40°C and 85°C, IEC 61215 Sec. 10.11 (I_{mp} applied when T> 25°C)
• Light and dark I-V, electroluminescence, thermal imaging, IEC 61215 dielectric withstand, insulation resistance, and visual inspection are done at the end of each round of stress testing

Table 1. The organization of the modules within the accelerated lifetime test sequences in the Test-to-Failure protocol.

The testing was carried out with the following failure criteria:

1. Loss of 20% of initial (round 0) power output
2. Arcing in module circuitry or junction box
3. Failure of dielectric withstand or wet insulation resistance tests at end of test segment
4. Leakage current greater than 1 mA during biased DH exposure
5. Open-circuit fault during forward-biased TC
6. Development of major visual defects.

Three changes were made from the original published protocol. For failure, the maximum loss in initial power was changed from 50% to 20%. This is because the nature of the modules' vulnerability at the stress level applied is apparent with a 20% power loss, and it corresponds to the limit of today's 25-year module warranties. The second change is that the acceptable leakage current during damp heat with bias was increased from 50 μA to 1 mA. While 50 μA may be a reasonable limit for a leakage test at room temperature, encapsulants such as EVA become significantly more conductive at 85°C [13]. Because the TTF protocol tests only six modules, which is not a statistical representation, the protocol considers a failure in any module to constitute failure of the group; however, as this is the first

implementation of the protocol, we seek to explore the effects of the stress and choose to continue the testing of the other modules in many cases. We also seek to evaluate the TTF protocol itself.

Deviations encountered during the course of test include an uncertainty in the RH (+10%/-0% from setpoint) in the damp heat test and the STC current setpoint, (+0%/-10%) in thermal cycling. The STC current deviation has no material effect on the results. The influence of the deviation of the RH will need to be studied further; however, there is published data that an increased RH beyond 85% has a relatively small effect on module leakage current and electrolytic corrosion [13].

RESULTS

The normalized module maximum power results are given in Fig. 1. With the exception of one design (module 5), module nameplate ratings were found to be consistently higher than the power that we measured. Module model 1 completed four rounds; models 2, 3, and 4 completed two rounds; and model 5 completed one round of the protocol at this writing.

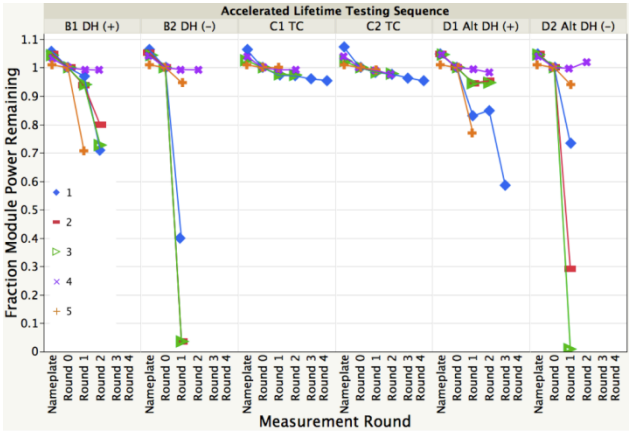

Figure 1. Table of results. Fraction module power remaining vs. measurement round by accelerated lifetime testing sequence. Module models 1-5 are indicated in the legend.

Thermal cycling

The modules subjected to the TC sequence can be seen to degrade slightly with each TC 200 cycle round (Fig. 1). Model 1 retains about 95.5% of the initial power after 800 cycles with an approximately linear degradation rate. The other module designs appear to be tracing this rate as well or performing slightly better. In some cases, crack growth in the cells was observed (Fig. 2). Considering this, the crystalline silicon modules under test are exhibiting good resilience to thermomechanical fatigue.

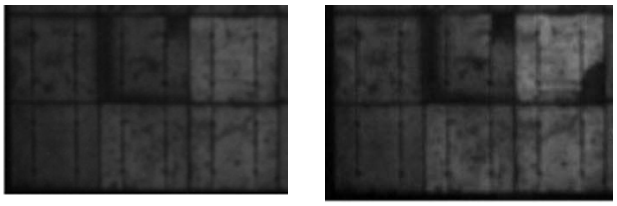

Figure 2. Development of a crack in a cell in thermal cycling imaged by electroluminescence in model 1 at the upper right cell. Left, initial; and right, after 200 cycles. This stress sequence has not caused significant power loss.

Damp heat with bias

When system voltage bias is applied, electrolytic corrosion and degradation signatures are seen to occur depending on the polarity of the bias as reported previously [8,13]. Four modules passed their first round (1000 h) in damp heat with positive bias to the active layer in DH(+) and Alt DH(+) sequences; however, there was some variation depending on the module design.

An image taken for failure analysis of model 1 stressed in DH(+) configuration after 2000 h is shown in Fig. 3. The following is observed:

- Silver grid finger corrosion
- Silicon nitride thinning, relatively uniformly
- Ionic transport from bus-straps to module edge
- Formation of bubbles in encapsulant
- Rear contact metallization degradation
- Corrosion of the aluminum frame
- Backsheet cracked (after 2000 h)
- Reduced electroluminescence efficiency around cell edges (significant after 2000 h)

Figure 3. Left, image of a module after 2000 hrs. in damp heat with + 600 V applied to the active layer with respect to the grounded module frame. There is evidence of grid finger and aluminum frame corrosion, metal ionic transport from the bus strap, and occasional delamination. Right, electroluminescence image of a four-cell region of this module, indicating darkening and degradation at positions around the rear bondpads.

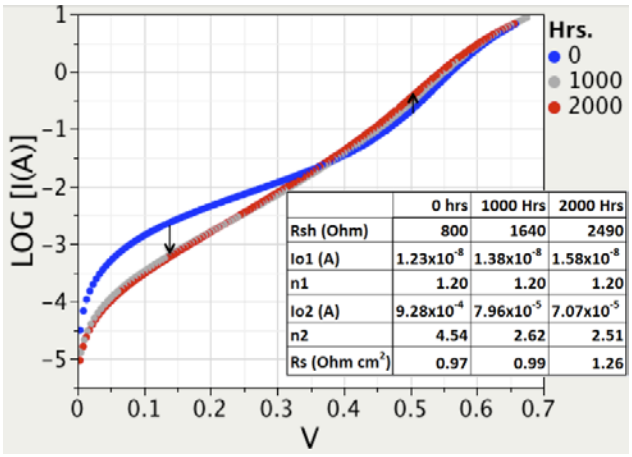

Figure 4. Dark I-V curves normalized with respect to the number of cells in the module, for module model 1 undergoing damp heat with +600 V bias measured initially, and after two rounds of 1000 h of stress testing. Results of the two-diode model fitting parameters are shown in the inset, including saturation currents (Id), ideality factors, and series (Rs) and shunt resistance (Rsh). Rsh and the parameters associated with junction quality (Id2, n2) improve with stressing, but Rs increases. The arrows indicate motion of the two regions of the curves over the stress intervals.

Silicon nitride antireflective (AR) coating degradation was significantly more severe in model 1 compared to others tested. Not only was this observed in the modules with bias applied, but also to a small extent in those tested in 1000 h at 85°C/85% RH without bias. Silicon nitride films are found to react with water at high temperature and pressure to form hydrous silica [14]. The degradation observed here appears to occur in the case of modules with high moisture ingress, is likely to vary with the density of the silicon nitride, and the degradation is accelerated

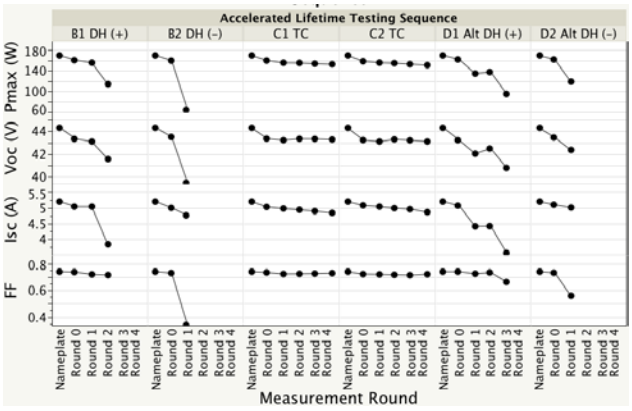

Figure 5. Maximum power, open-circuit voltage, short-circuit current and fill factor for the six modules of model 1 in each round undergoing the TTF protocol.

with increased leakage current associated with the application of system bias. The positive bias to the active layer has previously been associated with cell metallization corrosion such as that seen with Ag gridfingers [13] and Al cell metallization [15]. The previously reported gridline tip blossoming associated with electrolytic degradation [16] was not observed in any of the models tested in this work.

Dark I-V curves were obtained for the modules over the course of stress tests. Curve fitting of the results using a two-diode model is shown for model 1 in the DH (+) configuration (Fig. 4). Interestingly, the 2nd diode properties that were estimated, including the shunt resistance (Rsh), the second diode saturation current Io2 and the ideality factor n2 improve with the DH(+) stress. These improvements suggest a reduction in the leakage paths and carrier recombination across the p-n junction of the device because the second diode represents the junction properties [17]. Series resistance (Rs) degrades in each successive round. The Rs increase is likely associated in part with the observed metallization corrosion. Around 0.5 V, the measured saturation current increases with the increase in the first diode saturation current Io1, which would affect the maximum power point. The reduction in short-circuit current measured in the LIV tests is associated with the degradation in the AR coating and is most responsible for the power loss in model 1 (Fig. 5). For other models, loss of fill factor due to series resistance associated with metallization degradation was the greater contributor to power loss under DH(+) stress.

The modules subjected to damp heat with negative bias, DH(-), generally fared the worst, with power drop of much greater than 20% in just one round of stress with the exception of models 4 and 5. Degradation mechanisms observed include:

- Severe cell shunting
- Localized silicon nitride decomposition
- Localized bubbles and delamination
- Oxidation of the interconnect metallization and bussing
- Si-Ag metallization interface peeling/delamination
- Backsheet burns.

Depending on the extent of water ingress, the silicon nitride coating is degraded, but in a more localized manner than in the DH(+) modules (Fig. 6). The silicon nitride is least degraded in the middle of the cell, presumably because it is more difficult for the water reactant to diffuse there, unless delamination has occurred, in which case the silicon nitride is more extensively degraded. As with modules stressed in the DH(+) configuration, the silicon nitride degradation appears to be accelerated electrolytically.

The degradation in the power of the modules stressed in the DH(-) sequence is associated primarily with a loss in fill factor. Analysis of these modules by thermal and

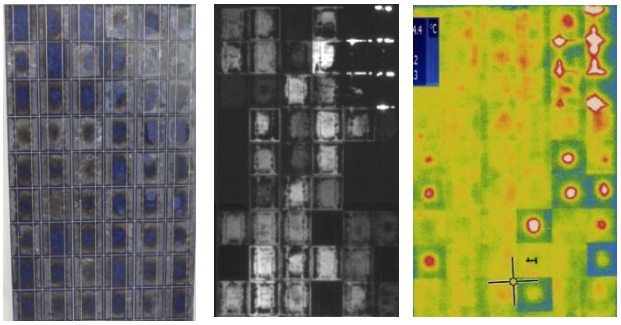

Figure 6. Model 1 after round 1 of DH(-) stress; left, optical image indicating silicon nitride degradation; middle, electroluminescence; and right, thermal imaging indicating severe shunting often in cell centers (white).

electroluminescence imaging indicate shunting with patterns that depend on the module design. Model 1, which uses glass with AR coating, exhibits localized hot spots in many cases, with those cells having significantly reduced electroluminescence, as is characteristic of shunted cells. The shunting was also confirmed by characterizing the cells by shading them individually in light I-V tests [18]. Modules without AR-coated glass that we tested exhibited greater and more uniform shunting in the DH(-) stress test.

Alternating damp heat and thermal cycling

In this test sequence, modules were cycled through damp heat with bias followed by TC, and then returned to the start of the cycle. Based on the tests carried out to date, we have not found that module power is significantly reduced after round 2, the thermal cycling round. After the third round in DH(+), the polyester (PET) backsheet in model 1 is hydrolytically degraded, embrittled, and cracked, leading to failure of both the wet insulation resistance test and a power loss >20% (Fig. 7). While such failure modes occurred after 2000 h in the DH(+) sequence discussed above, there were more cracks in the backsheet and greater power degradation after 3 rounds in the alternating sequence for this model. Other models

Figure 7. Hydrolytically degraded, embrittled, and cracked backsheet of model 1 after round 3 of the alternating DH+/TC sequence.

currently in line for test through this sequence will yield more statistics when completed.

DISCUSSION

The damp heat with bias test has proven to be significantly more severe than the thermal cycling test in the TTF protocol. Failures of c-Si modules during the thermal cycling phase of qualification testing have been increasing; it was the single largest failure in qualification testing between 2007 and 2009 at one laboratory [19]. This suggests thermal cycling remains a relevant leg of the protocol; however, no modules with such vulnerability have yet been found in this experiment.

The 85°C/85% RH test itself is a challenge for modules, and addition of system bias adds significant additional stress. Silicon nitride degradation seen here is not typically seen in fielded modules because the chemical activity of water to hydrolyze silicon nitride is much higher in the damp heat test. As has been previously pointed out [6], this test appears to be a good indicator of the extent of water diffusing into the module with the potential to cause damage. The extent to which silicon nitride damage occurred varied greatly over the modules examined, and the constructions least likely to allow moisture ingress exhibited much less of the silicon nitride degradation.

Field testing of modules to quantify the degradation associated with system bias has been well reported for thin-film modules, but less so for c-Si modules. Modules under constant system bias display maximum leakage current of 2 μA at the National Renewable Energy Laboratory (Golden, CO, USA) [20] and around 8 μA at the Florida Solar Energy Center (Cocoa, FL, USA) [21]. As an indicator of the acceleration factor, module leakage currents in the TTF are generally in the range of 10 to 100 μA, though some fall out of this range at either extreme, depending on the module design. While more tests are required to determine how system bias affects fielded modules, there is anecdotal evidence that arrays disconnected from a peak power tracking inverter may exhibit degradation, and it is likely that negative bias strings will experience module degradation by the shunting mechanism at some high system voltages.

SunPower has reported degradation of PV modules because of bias, attributed to a static charge that develops at the cell surface [12]. This static charge was also reported to be quickly and completely reversible. To see if an analogous mechanism was occurring in the mc-Si modules examined herein, the model 3 module that failed after one round of Alt DH (-) stress was subjected to +1000 V at room temperature in condensing humidity for 72 h with negligible power gain found. The module was then subjected to DH (+1000 V) at 85°C/85% RH for 144 h, and the power increased from 3% to 25% of original power with a fill factor increase from 0.25 to 0.33.

The differences between what is observed here with conventional cell modules and the high-efficiency SunPower back-contact cell are as follows: (1) Reversing the polarity to reverse the degradation is slow and incomplete in conventional cell modules, unlike what is reported for the SunPower module. (2) The polarity of the bias on the active layer that degrades multicrystalline modules is negative—which differs from the positive bias that degrades the SunPower high-efficiency module. The negative bias to active layer would tend to accumulate a positive charge over the cell surface, which would enhance the front surface field of the conventional cell. Because we are seeing degradation in this configuration, the surface charge mechanism would not appear to apply. (3) The degradation mechanism by a negative charge in the high-efficiency cell is reduction in minority-carrier lifetime, whereas it is shunting in the conventional cells tested herein. By the dark I-V analysis, junction properties are improved by positive bias to the active layer of the conventional cell modules. (4) n+ emitter surfaces of conventional cells need to be of much lower sheet resistivity, making it comparatively difficult to overcome its associated built-in surface field and significantly degrade cell properties.

The findings therefore point not to a surface charge created by the DH(-) stress, but to some ion drift in the silicon cell that can move to and shunt the front junction, typically 0.20–0.35 μm in depth into the silicon. While the ion species is not yet identified, elements exist that primarily act on junction properties, such as copper [22]. The evidence we obtained points to the leakage current through glass and the encapsulant as the enablers. This charge-induced degradation under bias has been reported to be a function of encapsulant resistivity, whereby more resistive encapsulants exhibit less degradation [23]. Approximate ranges of encapsulant resistivity have recently been summarized [24]. The present tests indicate approximately two orders of magnitude higher leakage current for the modules that degraded most under DH(-) configuration (model 3) compared to the module that degraded least (model 4). In these tests, we also found that modules with an AR coating on the glass such as model 1 exhibited better power retention through the DH(-) sequence than those without such coating. The enhancement in performance is consistent with the use of oxide barrier layers in thin-film modules that are used to minimize Na migration that causes degradation [25]. Other proposed methods of reducing leakage current or its effects and the resulting degradation of thin-film modules include [10]:

- Building arrays such that the active layer is at positive voltage potential with respect to the frame.
- Reducing frame area and use of mounting points bonded to the backplane.
- Reducing humidity in and around the module packaging, which increases conductivity.
- Reducing electrical potential between the external packaging and the active layer.

SUMMARY

The NREL Test-to-Failure protocol is demonstrating the ability to differentiate the performance of various module designs with the prescribed accelerated testing sequences, elucidating module weaknesses, and pointing to some failure mechanisms that should be examined in fielded c-Si modules, especially those in high-voltage arrays. The c-Si modules under test appear robust to thermomechanical fatigue according to the thermal cycling sequence of the protocol. Damp heat with system bias applied to the active layer with respect to the grounded module frame significantly accelerates electrolytic corrosion, and the observed silicon nitride degradation points to areas with higher moisture ingress. The results of dark I-V curve fitting indicate the properties of the cell p-n junction are affected, with positive bias to the active layer improving the p-n junction characteristics, but degrading the series resistance and the saturation current around the maximum power point. Negative bias catastrophically shunts the modules, excepting the case where the module packaging blocks leakage current effectively in the 85°C/85% RH condition.

ACKNOWLEDGEMENTS

Ed Gelak for tool construction, Steve Rummel, Allan Anderberg, and Keith Emery for module measurements, Michael Quintana and Prof. Govindasamy Tamizhmani for helpful discussions, and Ron Sinton and Kaitlyn VanSant for the technical review of the manuscript. This work was supported by the U.S. Department of Energy under Contract No. DE-AC3608GO28308 with the National Renewable Energy Laboratory.

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REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

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1. REPORT DATE *(DD-MM-YYYY)*	2. REPORT TYPE	3. DATES COVERED *(From - To)*
October 2010	Conference Paper	

4. TITLE AND SUBTITLE
Test-to-Failure of Crystalline Silicon Modules: Preprint

5a. CONTRACT NUMBER
DE-AC36-08-GO28308

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)
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5d. PROJECT NUMBER
NREL/CP-5200-47755

5e. TASK NUMBER
PVD9.1320

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
National Renewable Energy Laboratory
1617 Cole Blvd.
Golden, CO 80401-3393

8. PERFORMING ORGANIZATION REPORT NUMBER
NREL/CP-5200-47755

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSOR/MONITOR'S ACRONYM(S)
NREL

11. SPONSORING/MONITORING AGENCY REPORT NUMBER

12. DISTRIBUTION AVAILABILITY STATEMENT
National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161

13. SUPPLEMENTARY NOTES

14. ABSTRACT *(Maximum 200 Words)*

Accelerated lifetime testing of five crystalline silicon module designs was carried out according to the Terrestrial Photovoltaic Module Accelerated Test-to-Failure Protocol. This protocol compares the reliability of various module constructions on a quantitative basis. The modules under test are subdivided into three accelerated lifetime testing paths: 85°C/85% relative humidity with system bias, thermal cycling between –40°C and 85°C, and a path that alternates between damp heat and thermal cycling. The most severe stressor is damp heat with system bias applied to simulate the voltages that modules experience when connected in an array. Positive 600 V applied to the active layer with respect to the grounded module frame accelerates corrosion of the silver grid fingers and degrades the silicon nitride antireflective coating on the cells. Dark I-V curve fitting indicates increased series resistance and saturation current around the maximum power point; however, an improvement in junction recombination characteristics is obtained. Shunt paths and cell-metallization interface failures are seen developing in the silicon cells as determined by electroluminescence, thermal imaging, and I-V curves in the case of negative 600 V bias applied to the active layer. Ability to withstand electrolytic corrosion, moisture ingress, and ion drift under system voltage bias are differentiated.

15. SUBJECT TERMS
Photovoltaics; PV; Modules; Corrosion; Electrolytic corrosion; leakage current; test-to-failure; accelerated lifetime testing; ALT; Crystalline silicon

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			19b. TELEPHONE NUMBER *(Include area code)*
Unclassified	Unclassified	Unclassified	UL		

Standard Form 298 (Rev. 8/98)
Prescribed by ANSI Std. Z39.18