NASA/CR—2006-214258

Junction-to-Case Thermal Resistance of a Silicon Carbide Bipolar Junction Transistor Measured

Janis M. Niedra
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November 2006

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Prepared under Contract NAS3–00145

National Aeronautics and
Space Administration

Glenn Research Center
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November 2006

Acknowledgments

This work was sponsored by the NASA Glenn Research Center under NAS3–00145,
with G.E. Schwarze as the Project Manager.

Level of Review: This material has been technically reviewed by expert reviewer(s).

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Abstract

Junction temperature of a prototype SiC-based bipolar junction transistor (BJT) was estimated by using the base-emitter voltage (V_{BE}) characteristic for thermometry. The V_{BE} was measured as a function of the base current (I_B) at selected temperatures (T), all at a fixed collector current (I_C) and under very low duty cycle pulse conditions. Under such conditions, the average temperature of the chip was taken to be the same as that of the temperature-controlled case. At increased duty cycle such as to substantially heat the chip, but same I_C pulse height, the chip temperature was identified by matching the V_{BE} to the thermometry curves. From the measured average power, the chip-to-case thermal resistance could be estimated, giving a reasonable value. A tentative explanation for an observed bunching with increasing temperature of the calibration curves may relate to an increasing dopant atom ionization. A first-cut analysis, however, does not support this.

Source of the Problem

Intelligent use of a transistor in power management applications requires control of its junction temperature to some specified limits. The commonly specified thermal conductivity, junction to case, is not always available for packaged experimental or prototype devices obtained from R&D laboratories. Packaging obviously prevents the direct observation of the semiconductor chip. The sole recourse then is to find a terminal electrical property that can be exploited for thermometry. This paper reports an attempt to estimate the thermal resistance of a packaged SiC based BJT, from observations of electrical characteristics under low and high duty cycle power switching.

Procedure Explained

The regulation or switching of collector current, I_C, to a load is the most direct way of setting the temperature rise of the chip above its case. And the case is assumed mounted to a temperature-controlled heat sink. The base-to-emitter junction voltage, V_{BE}, depends on the base current, I_B, and the junction temperature T. And so $V_{BE}(I_B, T)$ and I_C are two elements on which the temperature rise thermometry can be based. But of course there are complications.

A key realization is that external measurements at the base and emitter leads include bulk voltage drops in the chip added to the junction voltage. Ohmic drops due to the flow of I_C can be both significant as compared to the junction V_{BE} as well as temperature dependent in doped SiC. In SiC, usually the dopant atoms are not fully ionized at room temperature, leading to a significant temperature dependence of bulk electrical resistivity as the temperature is raised. And there may be other temperature dependencies. Therefore our V_{BE} thermometer must be calibrated taking I_C into account. And this I_C must have the same pulse height as will be finally used in a higher duty cycle mode to heat the chip internally. At room and selected higher case temperatures, as set by an external heater, the external V_{BE} is plotted against I_B, in a very low duty cycle pulse mode. The I_C is set to a fixed pulse height that is representative of practical application of the particular BJT, by say a resistive load and a dc power supply. And the I_B

pulses should be kept sufficiently high to ensure saturated switching of the BJT and just long enough to get steady V_{BE} and I_B readings. If properly done, internal heating of the chip then should be negligible.

The so generated thermometry curves can be used to obtain an estimate of the junction-to-case thermal resistance. The duty cycle now has to be substantially increased to get a measurable increase of the steady state chip temperature above that of the heat-sunk case, while maintaining the same I_C pulse height. Comparison of the V_{BE} pulse height with that of the calibration curves then gives the temperature. The thermal resistance then follows from the known case temperature and the average power loss in the chip shown by the displayed waveforms.

Basic Experiment

All thermometry work was done with variations of the circuit shown in figure 1. This circuit was built primarily for establishing a turn-off transient that is as rapid as the turn-on transient, but modifications worked well also for thermometry.

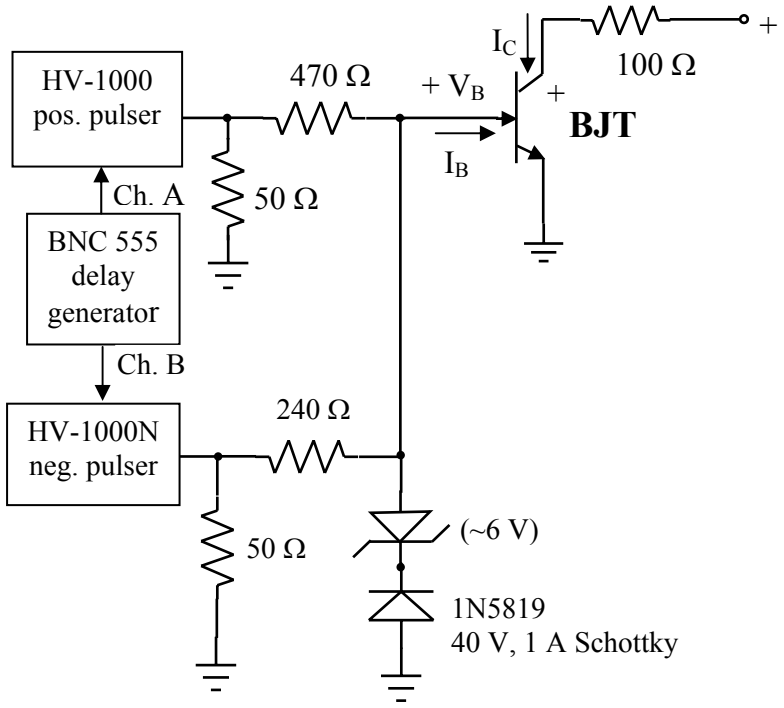

Figure 1.—This switching speed test circuit was used for thermometry calibration work. In the higher duty cycle, chip heating case, the negative pulser and its 50 Ω load resistor were simply replaced by a dc power supply. Also at higher duty cycle, other resistors were varied to reduce their dissipation. The positive pulser provides the constant pulse height I_B.

Temperature calibration data are shown in figure 2 below for a 4 A, 600 V rated SiC BJT made by United Silicon Carbide, Inc., and labeled P2. The decrease of V_{BE} with increasing T at constant I_B is equivalent to the usual shifting to the left of the I vs. V curves for say silicon P-N junction diodes, with the I-axis drawn vertically. But the curve bunching seen in figure 2 is not usual. However, in SiC devices the dopants are usually not fully ionized at room temperature. Hence as the temperature is raised, the degree of ionization increases and the body resistance drops. And the terminally measured V_{BE} includes the resistive drop due to I_C, which thus decreases with increasing temperature until the dopants are fully ionized. The degree of ionization also plays a more subtle effect through the complicated physics of the so-called reverse saturation current I_0 in the diode equation. In fact, the simple diode equation, when solved for the junction voltage in the form

$$V = (\kappa\, T/q)\, \ln[(I/I_0) + 1], \tag{1}$$

can be misleading as to temperature effects, because the complicated T-dependence of I_0 is not manifest. Being an aside, details of the mechanism that can (and usually do) generate a negative $\partial V/\partial T$ in the diode equation are ferreted out in appendix A. The bunching of the curves seen in figure 2 is not, however, predicted there. This bunching is in any case undesirable, as it reduces temperature resolution and here especially in the region of interest around 200 °C.

The P2 device was next mounted to a temperature controlled heat sink plate and set up to switch a pulsed 3 A current into a 100 Ω non-inductive load resistor that was also mounted to the same heat sink. Pulses of about 640 ns were spaced 5 μs, making a duty cycle of 0.13. The combined heat from the load

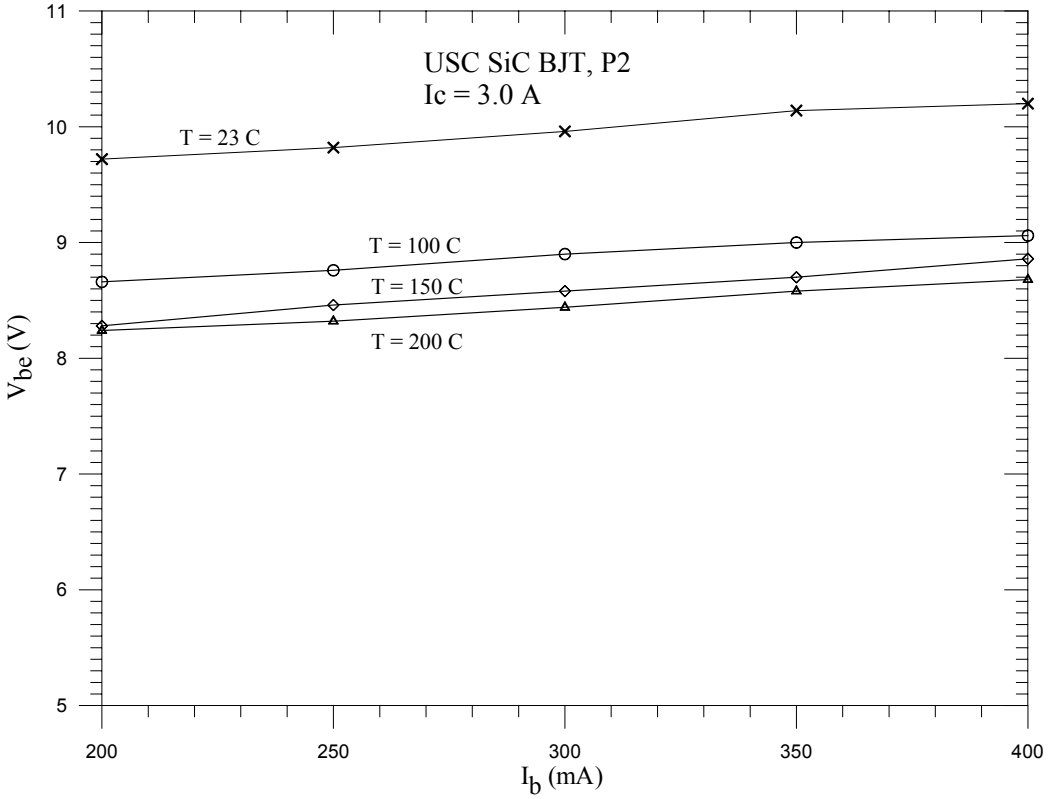

Figure 2.—Temperature dependence of the V_{BE} versus I_B curves. The duty cycle here is sufficiently low such that the chip and case temperatures are practically identical.

resistor and the transistor caused the temperature of the heat sink to slowly rise. When the V_{BE} pulse height matched the V_{BE} of the 100 °C calibration curve (see fig. 2), waveforms were recorded, plate temperature (80 °C) was noted and operation ceased. Hence the case-to-chip temperature rise was then 20 °C.

Various scope measurements could then be done on the recorded traces. The exponential rise-time for the I_C was τ_{on} = 68.3 ns and the linearly approximated fall-time was τ_{off} = 134 ns. The formulas giving the energy loss in these approximations are

$$E_{on} = (1/2)\, V_0\, I_0\, \tau_{on} \quad \text{(exponential approximation)}$$

and

$$E_{off} = (1/6)\, V_0\, I_0\, \tau_{off} \quad \text{(linear approximation)},$$

where V_0 and I_0 (= I_C) are the switched voltage and current. The arithmetic then gives $E_{on} = 3.16\times10^{-5}$ J and $E_{off} = 2.07\text{x}10^{-5}$ J. According to the scope measurement, the on-state V_{CE} was only 0.4 V, whereas according to the static characteristics of the P2, about 4 V was expected at 100 °C and 3 A. Using the scope measurement, the conduction loss is only 7.6×10^{-7} J, which is quite small compared to the switching loss. The base-drive energy was also small, being about 0.15×10^{-5} J. Finally, adding all losses and dividing by the 5 μs period gives an average power of 11 W into the chip.

The junction-to-case thermal resistance $R_{\theta JC}$ is thus about 20/11 = 1.8 °C/W. This is somewhat lower than that of a roughly comparable silicon BJT, such as the planar BUH50 (50 W, 800 V, 4 A). But such a comparison can only be very rough, because the P2 has no given power rating. Nevertheless, the value of the thermal resistance obtained appears to be reasonable and gives some confidence in the method.

Final Remarks

The initial experimental evidence supports the feasibility of the presented method of temperature rise thermometry. But it also points out the problem of curve bunching and consequent loss of temperature resolution seen in figure 2. The root cause in the described experiment appears to be the increase in body conductivity as more dopants in SiC (especially the acceptors) become ionized with increasing temperature. This problem may be a characteristic of a material, such as SiC, whose commonly used dopant atoms are not fully ionized at room temperature. However, a workaround may be possible by using pulse control methods..

Alternative Schemes

In a modified procedure, consider generating the low duty cycle, calibration curve set (fig. 2.) with the collector lead open. Making I_C = 0 hopefully should reduce the nonlinear bunching with increasing T of the V_{BE} versus I_B curves, if dopant ionization is at the heart of the matter. The general idea is to use higher duty cycle pulses of I_C to substantially heat the chip, but measure a steady V_{BE} and I_B while I_C = 0. For example, after a sufficient number of base drive pulses to cause a substantial temperature rise of the chip, the collector power supply could be effectively disconnected, for the duration of one base pulse or one period. This would be a matter of pulse control logic. A scheme might utilize a commercially available high voltage pulser for the collector supply, with base drive applied continuously or pulsed in a synchronism. Values of V_{BE} and I_B could be measured during the I_C dead time. In all such schemes, a fast-recovery diode (GaAs, Schottky) is needed in the collector lead to block current flow in the base-to-collector direction.

Conduction and Switching Losses

Occasionally the concern has been voiced that higher on-state conduction losses in a SiC based, as compared to a Si based, BJTs would be seriously adverse to their application as switches. The present example of the P2 device, however, shows that this is circumstantial and not always so. Therefore, let us look a little closer at the comparison of conduction losses to switching losses expected for a waveform of essentially square pulses of width w, repeated with a period τ. The duty cycle D then is $D = w/\tau$. Let the switched voltage and current be V_0 and I_0.

Approximating both turn-on and turn-off by the same exponential function, the total switching loss in one period then is

$$E_S = V_0 I_0 \tau_s \ ,$$

where the exponential switching time constant τ_s is related to the usual scope measured 10 to 90 percent switching time $\tau_{s,10\text{-}90}$ by $\tau_s = \tau_{s,10\text{-}90}/\ln 9$. The conduction loss in one period is simply

$$E_C = I_0^2 R_{CE,on} w \ ,$$

where $R_{CE,on}$ is the collector-to emitter on-resistance, mimicking MOSFET terminology. Division of E_S and E_C by τ then gives the average switching and conduction loss powers P_S and P_C. The ratio of these powers thus is

$$P_C/P_S = E_C/E_S = I_0 R_{CE,on} w/(V_0 \tau_s) \ .$$

To get a numerical feel, assume a switching frequency of 200 kHz and a duty cycle of 0.5, giving w = 2.5 μs. The $\tau_{s,10\text{-}90}$ is not likely to be significantly less than 50 ns even for SiC power BJTs, giving τ_s = 23 ns. At least for the P2 device, the $R_{CE,on}$ was observed to be about 1.5 Ω at room temperature on a static curve tracer, but appeared to be less under fast pulse conditions. 3 A is about the rated current for this device, but operation at 300 V is at about ½ of the rated voltage. With these values, $P_C/P_S = 1.6$. But operation at higher frequency (smaller w) and higher voltage is clearly possible for this device and $\tau_{s,10\text{-}90}$ = 50 ns is likely to be on the short side. Hence the evidence shown here does not support the claim of necessarily unacceptably high conduction losses in SiC based BJTs.

Appendix A

Temperature Dependences in the Diode Equation Applied to SiC

The usual observed decrease of V with increasing T at constant I means that in the simplest p-n junction diode modeling equation, i.e., Eq. (1), the so-called reverse saturation current I_0 must have a T-dependence of at least exponential order. We shall review here this dependence, pointing out the source of the usually negative $(\partial V/\partial T)|_I$ and the effect of dopant degree of ionization. A caveat is that Eq. (1) may be inadequate if there is significant recombination in the depletion region, in which case additional terms are required.

A standard form for I_0, written in terms of the electron and hole diffusion constants, minority carrier diffusion lengths, intrinsic carrier density and the ionized dopant densities, is

$$I_0 = q\,A\left[\frac{D_N\,n_i^2}{L_N\,N_A^-}+\frac{D_P\,n_i^2}{L_P\,N_D^+}\right] \tag{A1}$$

The above I_0 can be put in more fundamental terms such as the temperature, electron and hole mobilities, densities and effective masses, and minority carrier lifetimes and the band gap energy. Use is made of the Einstein relation and standard textbook formulas [1] for n_i, etc., to finally give

$$I_0 = 4A\,q^{1/2}\,h^{-6}\,(2\pi)^3\left(m_n^*\,m_p^*\right)^{3/2}\left[p^{-1}\left(\frac{\mu_n}{\tau_n}\right)^{1/2}+n^{-1}\left(\frac{\mu_p}{\tau_p}\right)^{1/2}\right](\kappa T)^{7/2}\,e^{-\frac{E_g}{\kappa T}}\,, \tag{A2}$$

where A is the junction area, q is the magnitude of the electronic charge, $p = N_A^-$ and $n = N_D^+$. In the case of an NPN transistor, the emitter region will be more heavily doped than the base and so the n^{-1} in the bracket can be neglected.

Some of the terms in the above expressions can vary widely, even in Si. The lifetimes are sensitive to temperature and the presence of recombination centers. The mobilities vary as $T^{-\alpha}$, where $2<\alpha<2.5$. The effective masses are not particularly temperature sensitive. Unlike in Si, the dopants used in SiC are far from being fully ionized at room temperature and hence their degree of ionization must be calculated from their positions in the bandgap and the temperature. The following values have been suggested [2]:

$m_n^* = 0.5\ m_0$	$\tau_n = 100$ ns	$\mu_n = 900\ cm^2V^{-1}s^{-1}$	$N_A \approx 3\times10^{17}\ cm^{-3}$
$m_p^* = 0.3\ m_0$	$\tau_p = 100$ ns	$\mu_p = 90\ cm^2V^{-1}s^{-1}$	$J \approx 500\ A/cm^2$
$E_C - E_D = 0.05$ eV	$E_A - E_V = 0.25$ eV		

In spite of uncertainties, a rough estimate for SiC of the terms in Eq. (A1) or Eq. (A2) can be obtained.

Let us write I_0 in the form

$$I_0 = A\,f(T)\,e^{-\frac{E_g}{\kappa T}}\,, \tag{A3}$$

where the function f is defined by

$$f(T)=4q^{1/2}\,h^{-6}\,(2\pi)^3\,(m_n^*\,m_p^*)^{3/2}\left[p^{-1}\left(\frac{\mu_n}{\tau_n}\right)^{1/2}+n^{-1}\left(\frac{\mu_p}{\tau_p}\right)^{1/2}\right](\kappa T)^{7/2}\quad . \tag{A4}$$

and the mobilities, lifetimes and carrier densities are functions of T.

The most temperature-sensitive terms in Eq. (A4) are assumed to be the p and n, as the degree of ionization involves an exponential dependence on T. Finding only the p is sufficient here, since the emitter is assumed to be heavily doped and the donors sit much shallower in energy. The ionization formula is developed in reference 3, the result for acceptors being

$$p=\frac{N_\zeta}{2}\left[\left(1+\frac{4N_A}{N_\zeta}\right)^{1/2}-1\right]\ , \tag{A5}$$

where

$$N_\zeta=\frac{2}{g_D}\left(2\pi m_p^*\,\kappa T/h^2\right)^{3/2}e^{-\frac{\Delta E_A}{\kappa T}}\ , \tag{A6}$$

and the degeneracy factor g_D is usually set to 2. If $N_A>>N_\zeta$, such when nearing carrier freeze-out, then $p\approx(N_A\,N_\zeta)^{1/2}$ is a good approximation. Thus at 300 K, where $N_\zeta = 1.39\times10^{14}$, only $p = 6.46\times10^{15}$ cm^{-3} out of the 3×10^{17} cm^{-3} acceptors are ionized, compared to $p = 5.80\times10^{16}$ cm^{-3} at 500 K. The corresponding change in body resistivity is obviously quite large.

For any reasonable forward current, the "1" in Eq. (1) can be neglected and hence Eq. (1) can be written in the form

$$qV = E_g + \kappa\,T\,\ln[J/f(T)]\ , \tag{A7}$$

where J = I/A is the current density and E_g is the band gap (about 3 eV in SiC). From this follows the sensitivity

$$(\partial V/\partial T)|_J = (\kappa/q)\,[\ln(J/f) - (T/f)\,(df/dT)]\ , \tag{A8}$$

of the junction voltage to temperature.

A rough estimate in SiC shows that at room temperature, the value of J/f(T) is considerably below unity, making ln[J/f(T)] negative. Indeed, $f(300)\approx1.4\times10^7$A/cm^2, giving $(\kappa/q)\ln(J/f)\approx-8.8\times10^{-4}$ V/K, which is much below the roughly -1.3×10^{-2} V/K observed. Moreover, the uncertainties in mobilities, lifetimes and ionized dopant densities seem insufficient to correct for this discrepancy.

Let us ferret out more systematically the main T-dependences hidden in the function f and contributing via the df/dT. The simplest such in Eq. (A4) is some power of T. Besides the manifest $T^{7/2}$, the mobilities too have been modeled as proportional to $T^{-2.3}$. The contribution to $(\partial V/\partial T)|_J$ in Eq. (A8) from total power law T^α proportionality in f is

$$-\frac{\kappa T}{q f}\left(\frac{\partial f}{\partial(T^\alpha)}\frac{\partial(T^\alpha)}{\partial T}\right)=-\frac{\kappa}{q}\alpha=-8.61\text{x}10^{-5}\alpha\ (V/K)\quad . \tag{A9}$$

But from Eq. (A4) and the above remarks, $\alpha \sim 1$ and surely below 10. Hence this contribution is rather small and constant.

The exponential T-dependence of p seems likely to contribute more. Its complications are best ironed out step by step. After some tedious algebra, one finds that

$$\frac{\partial p}{\partial T} = \frac{1}{2}\frac{\partial N_\zeta}{\partial T}\left[\frac{\left(1+2\frac{N_A}{N_\zeta}\right)}{\left(1+4\frac{N_A}{N_\zeta}\right)^{1/2}} - 1\right] \tag{A10}$$

and also that

$$\frac{\partial N_\zeta}{\partial T} = \frac{1}{T}\left(\frac{3}{2} + \frac{\Delta E_A}{\kappa T}\right) N_\zeta \quad , \tag{A11}$$

where $\Delta E_A \equiv E_A - E_V$. Again in the case of $N_A >> N_\zeta$, which is applicable here at 300 K,

$$\frac{\partial p}{\partial T} \approx \frac{1}{2T}\left(\frac{3}{2} + \frac{\Delta E_A}{\kappa T}\right)\left(N_A\, N_\zeta\right)^{1/2} \approx \frac{p}{2T}\left(\frac{3}{2} + \frac{\Delta E_A}{\kappa T}\right) \quad . \tag{A12}$$

Using the above results, the contribution to $(\partial V/\partial T)|_J$ arising from $\partial p/\partial T$ is found to be

$$-\frac{\kappa T}{q f}\left(\frac{\partial f}{\partial p}\frac{\partial p}{\partial T}\right) = \left(\frac{\kappa T}{q f}\right)\left(\frac{f}{p}\frac{\partial p}{\partial T}\right) \approx \frac{\kappa}{2q}\left(\frac{3}{2} + \frac{\Delta E_A}{\kappa T}\right) \quad , \tag{A13}$$

within the approximation based on $N_A >> N_\zeta$. At 300 K, the value of this positive contribution is 4.79×10^{-4} V/K.

For general interest, the above contributions can be totaled. Omitting considerable algebra, the final form is

$$\left(\frac{\partial V}{\partial T}\right)_{|J} = \frac{\kappa}{q}\left\{\frac{3}{4} - \alpha + \ln\left[\frac{J}{C_0\left(\kappa T\right)^{11/4}}\right]\right\} \quad , \tag{A14}$$

where

$$C_0 \equiv 2(2\pi)^{9/4}\, g_D\, q^{1/2}\, h^{-9/2}\, N_A^{-1/2}\left(m_n^*\right)^{3/2}\left(m_p^*\right)^{3/4}\left(\frac{\mu_n}{\tau_n}\right)^{1/2} \quad . \tag{A15}$$

For the given numerical values (and $g_D = 2$), $C_0 = 1.28\times10^{65}$ A m^{-2} (Joule)$^{-11/4}$. At K = 300, and J = 500 A/cm^2, $(\partial V/\partial T)|_J = 8.61\times10^{-5}\,[3/4 - \alpha + \ln(4.36\times10^{-3})]$ V/K $= 8.61\times10^{-5}\,(3/4 - \alpha - 5.44)$ V/K.

This diode equation based analysis applied to SiC predicts that $(\partial V/\partial T)|_J$ is, with high confidence, negative and increasing in magnitude with increasing temperature at room temperature. It provides no support for the curve bunching seen in figure 2.

Worth a passing note is the absence of ΔE_A in Eq. (A14). This is actually apparent from the outset from Eqs. (A7), (A4) and (A6), whenever $p \approx (N_A N_\zeta)^{1/2}$ is a valid approximation. The $\kappa T \ln$ operation in Eq.(A7) then reduces the $e^{-\frac{\Delta E_A}{2\kappa T}}$ factor, arising from Eq.(A6), to $-\Delta E_A/2$, which contributes zero to $(\partial V/\partial T)|_J$. The band gap factor $e^{-\frac{E_g}{\kappa T}}$ appearing in Eq.(A2) suffers a similar fate. The fact that E_g and ΔE_A may themselves have a temperature dependence was simply ignored here.

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3. R.F. Pierret, Advanced Semiconductor Fundamentals, Modular Series on Solid State Devices, vol. VI, G.W. Neudeck and R.F. Pierret, editors, Addison-Wesley, 1983.

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY (*Leave blank*)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	November 2006	Final Contractor Report

4. TITLE AND SUBTITLE

Junction-to-Case Thermal Resistance of a Silicon Carbide Bipolar Junction Transistor Measured

5. FUNDING NUMBERS

WBS 423799.03.01
NAS3–00145

6. AUTHOR(S)

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7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

QSS Group, Inc.
21000 Brookpark Road
Cleveland, Ohio 44135

8. PERFORMING ORGANIZATION REPORT NUMBER

E–15541

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

National Aeronautics and Space Administration
Washington, DC 20546–0001

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

NASA CR—2006-214258

11. SUPPLEMENTARY NOTES

Project Manager, Gene E. Schwarze, Power and Propulsion Division, NASA Glenn Research Center, organization code RPE, 216–433–6117.

12a. DISTRIBUTION/AVAILABILITY STATEMENT

Unclassified - Unlimited
Subject Category: 33

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13. ABSTRACT ***(Maximum 200 words)***

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14. SUBJECT TERMS

SiC bipolar junction transistor; Junction temperature; V_{BE} thermometry; Switching losses; Pulse techniques

15. NUMBER OF PAGES

16

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	