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On The Effect of Ramp Rate in Damage Accumulation of the CPV Die-Attach

Nick S. Bosco, Timothy J. Silverman, and Sarah R. Kurtz

National Renewable Energy Laboratory, Golden, Colorado, 80401, USA

***Abstract*–It is commonly understood that thermal cycling at high temperature ramp rates may activate unrepresentative failure mechanisms. Increasing the temperature ramp rate of thermal cycling, however, could dramatically reduce the test time required to achieve an equivalent amount of thermal fatigue damage, thereby reducing overall test time. Therefore, the effect of temperature ramp rate on physical damage in the CPV die-attach is investigated. Finite Element Model (FEM) simulations of thermal fatigue and thermal cycling experiments are made to determine if the amount of damage calculated results in a corresponding amount of physical damage measured to the die-attach for a variety of fast temperature ramp rates. Preliminary experimental results are in good agreement with simulations and reinforce the potential of increasing temperature ramp rates. Characterization of the microstructure and resulting fatigue crack in the die-attach suggest a similar failure mechanism across all ramp rates tested.**

***Index Terms* — Photovoltaic Cells, Soldering, Materials Reliability, Reliability Theory.**

I. Introduction

Thermal fatigue in the CPV die-attach will result in cracking and ultimately lead to thermal runaway and cell failure [1]. Simulating the extent of thermal fatigue both in an accelerated test environment and in service conditions is therefore of primary importance to develop a lifetime prediction. Currently, the IEC 62108 qualification thermal cycling sequence requires at least 28 days to complete. Considering the efforts of the IEC QA Task Force to develop lifetime-related accelerated test procedures will likely seek to extend the thermal cycling sequence, developing a more damaging yet shorter test is of primary interest. Previous work demonstrated that the normalized test time (wall clock time required to complete a test that induces an equivalent amount of thermal fatigue damage) may be significantly reduced by increasing the temperature ramp rate of the cycle [2]. According to this work, just increasing the temperature ramp rate from 3.75 to 7.5 °C/min will halve the normalized test time, Fig. 1. This simple adjustment to the thermal cycling sequence could, therefore, be extremely valuable in moving forward with development of an economical lifetime-related thermal cycling sequence.

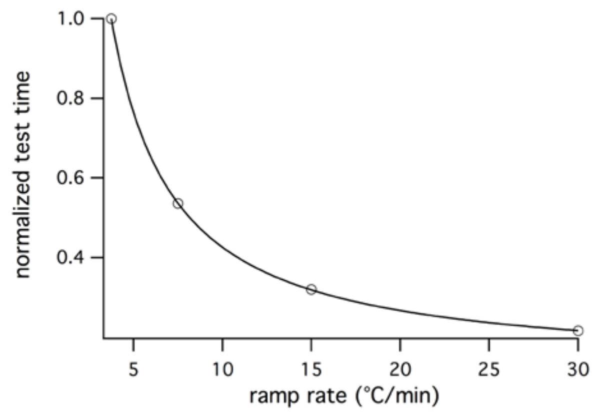

Fig. 1. FEM simulation results: normalized test time vs. cycle temperature ramp rate.

In development of such a sequence, its equivalence to outdoor exposure is paramount. In an analysis of one year of climatic data in Golden, Colorado it is found that while CPV cell temperature ramp rates up to 30 °C/min are experienced, over 95 % are under 6 °C/min, Figs. 2 and 3. Since the current approach uses a FEM to calculate equivalent damage between the accelerated thermal cycle and outdoor exposure, it must be validated to work across a large regime of temperature ramp rates in order to be confidently applied in developing a highly accelerated thermal cycling test sequence.

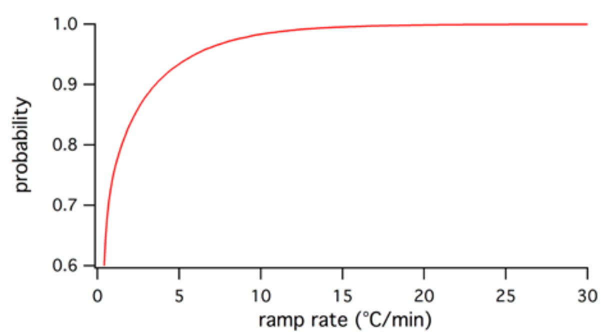

Fig. 2. Cumulative Density Function of CPV cell temperature ramp rates experienced during one year in Golden, Colorado.

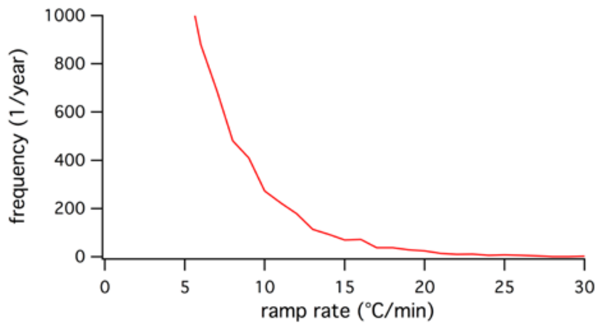

Fig. 3. Histogram of CPV cell temperature ramp rates experienced during one year in Golden, Colorado.

We have previously reported progress on developing a thermal fatigue model to simulate both service and accelerated testing conditions [3]. The model employed was developed to consider both the high- and low-stress regimes of creep (inelastic strain) where the physical mechanism changes from dislocation climb and glide to grain boundary sliding. The crux of the method is to calculate the amount of inelastic strain energy (damage) accumulated upon failure through accelerated thermal cycling and relate this to the amount of on-sun exposure that will accumulate a similar amount of damage. A key assumption is that the inelastic energy accumulated at the temperature ramp rates of accelerated testing results in a similar amount of physical damage as when accumulated at temperature ramp rates commensurate with service conditions.

In the current work, we repeat thermal cycling experiments to failure with four temperature ramp rates: 7.5, 15, 60 and 140 °C/min. Each test is also simulated to calculate the amount of damage accumulated. The thermal cycling experiments will determine if the amount of damage calculated through simulation for the different ramp rates result in a corresponding amount of physical damage to the die-attach. The result of this work will provide confidence for moving forward to develop an efficient highly accelerated thermal cycling sequence for lifetime-related evaluations.

II. Methods

A. Experimental

To conduct the thermal cycling tests, either a chamber that uses forward bias of the CPV cell for the heat source or a traditional oven style chamber is used [4]. The test articles are commercial CPV cell assemblies consisting of a 1 cm^2 III-V multijunction solar cell soldered to a substrate with eutectic PbSn solder. For the current study, four temperature profiles are explored and are primarily distinguished by their unique temperature ramp rates. Profiles 1 and 2 are performed with forward bias heating (blue curves) with temperature ramp rates of 140 and 60 °C/min, respectively, with a maximum temperature of 110 °C and minimum temperature of –40 °C and symmetric dwell times of 40 seconds, Fig. 4. These test are performed with only one sample each. Profile 3 is also conducted with forward bias heating for a ramp rate of 15 °C/min, a maximum and minimum temperature of 110 and –40 °C and symmetric dwell times of five minutes, Fig. 5. Profile 4 is conducted in an oven style chamber (red curve) and achieves a temperature ramp rate of 7.5 °C/min with a maximum temperature of 110°C and minimum temperature of –40 °C, Fig. 5. Profiles 3 and 4 are conducted with 15 samples each.

Prior to and periodically through cycling, each sample is ultrasonically imaged to monitor crack growth in the die-attach layer. Cycling on all test articles is conducted at least until the defined failure criterion is achieved: a 3.5 area% crack in the corner of the die-attach. Following failure, each sample is cross-sectioned and the limiting crack and die-attach microstructure imaged.

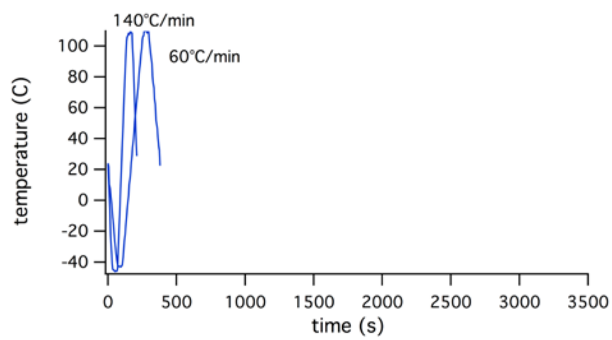

Fig. 4. Measured temperature profiles 1–2.

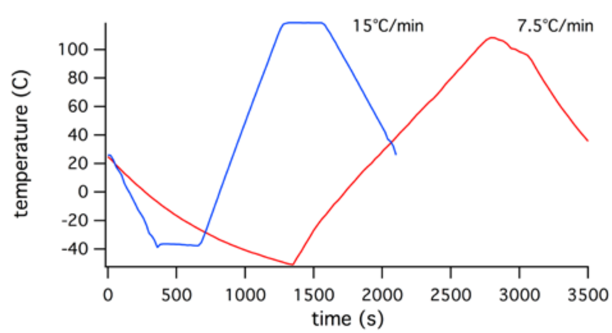

Fig. 5. Measured temperature profiles 3–4. Forward bias heating (blue) and conventional temperature chamber (red).

B. Modeling and Simulation

A 3D finite element model (FEM) of the CPV cell assembly used in this study was generated using

COMSOL. The rate-dependent creep behavior and the time-independent plasticity of the solder is characterized by Anand's model [5]. This constitutive model accounts for the two different creep mechanisms of Sn-containing solders: grain boundary sliding or dislocation glide (low stress and high temperature) and dislocation climb (high stress and low temperature).

An accumulated energy approach is taken to evaluate the solder's lifetime. This approach considers the inelastic strain energy density as a damage indicator [6]. Accordingly, both crack initiation and growth are functions of the average inelastic strain energy density (plastic work) accumulated per thermal cycle. In the current study, the two phases of failure are not differentiated, therefore only the total plastic work is considered as the metric for damage. It is proposed that a typical cell assembly will fail after it has sustained a characteristic quantity of damage.

Each thermal cycle was simulated with the FEM model. Due to the extremely fast temperature ramp rates, exact control of the assembly's temperature is difficult. Therefore each assembly's actual temperature measured through cycling serves as the input for each simulation.

III. Results and Analysis

A. Thermal Cycling

The results of the thermal cycling experiments are summarized in Figs. 6 and 7. Crack area percent was measured relative to the complete cell area from CSAM images. Crack area emanating from multiple corners was not differentiated in the measurements and therefore is included in the total area calculation. Crack growth with number of cycles is presented in Fig. 6. Imposed on this plot is the defined failure criterion of a 3.5 area% crack. The number of cycles to failure was evaluated with a Weibull fit for the 7.5 and 15 °C/min data sets while a linear interpolation was employed for the 60 and 140 °C/min rates since they each only contained a single sample. The number of cycles to failure are calculated to be 1210 and 690 for the 7.5 and 15 °C/min tests and 710 and 610 for the 60 and 140 °C/min tests, respectively. The measurements are plotted in terms of test time in Fig. 7. Here the expected trend is observed: the faster ramp rate tests reach the failure criteria faster than the slower ramp rate tests.

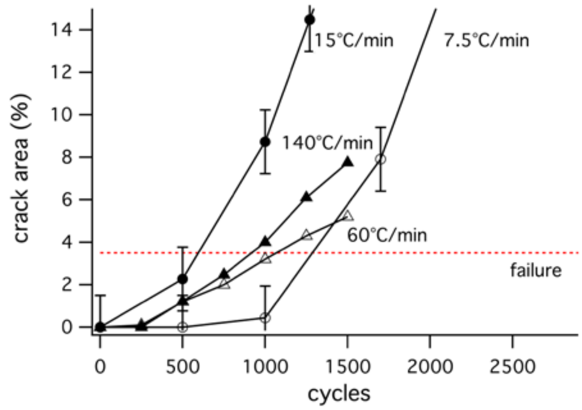

Fig. 6. Crack growth vs. number of cycles

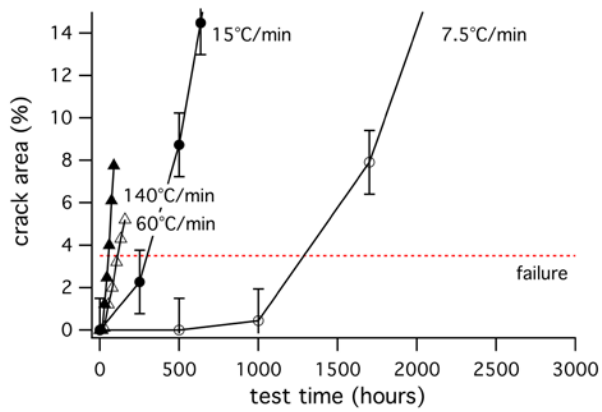

Fig. 7. Crack growth vs. test time

B. Simulation

The results of the FEM simulation are summarized in Figs. 8 and 9. Reported first is the amount of inelastic strain energy accumulated for each cycle, normalized with respect to the most damaging cycle: the 15 °C/min ramp rate, Fig 8. The current results are consistent with previous simulations when the large difference in cycle times between the 7.5 and 15 °C/min, and 60 and 140 °C/min profiles is considered, i.e. for similar cycle times, the faster ramp rate cycle is more damaging [2]. Also presented in Fig. 8 is the corresponding experimental observation of physical damage per cycle, similarly normalized to the 15 °C/min ramp rate cycle. This value is obtained by assuming even incremental crack growth is occurring every cycle until failure.

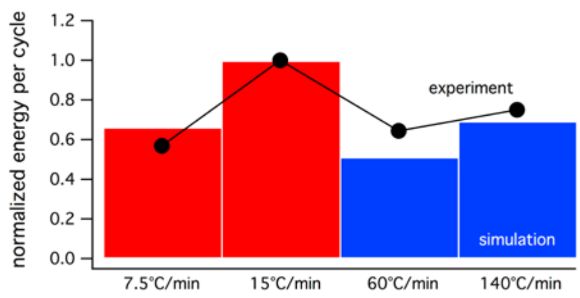

Fig. 8. Normalized inelastic strain energy (damage) per cycle for the four accelerated thermal cycles simulated.

The consequence of increasing the temperature ramp rate on overall test time is illustrated in Fig. 9. This plot is constructed by considering the amount of time each cycle requires achieving a similar amount of accumulated damage, and normalized with respect to the cycle that accumulates damage slowest. Simulations suggest that changing the ramp rate from 7.5 to 15 °C/min reduces test time by over 60 % and further reductions may be achieved with the very fast temperature ramp rates explored in this study: just over 5% of the time is required for the 140 °C/min profile to achieve a similar amount of thermal fatigue damage. Similarly imposed on the simulation results are the experimental observations related to crack growth: test time required to produce an equal sized crack.

A comparison of the simulated damage rate and the experimentally observed crack growth rate is presented in Fig. 10. A line of slope one that represents perfect agreement between simulation and experiment is also included on the plot. Points lying above the line suggest that crack growth is occurring faster than the simulation suggests, and points lying below suggest slower than expected crack growth. Considering the single point measurements for the two faster ramp rate cycles, it appears the experimental observations are in good agreement with simulation.

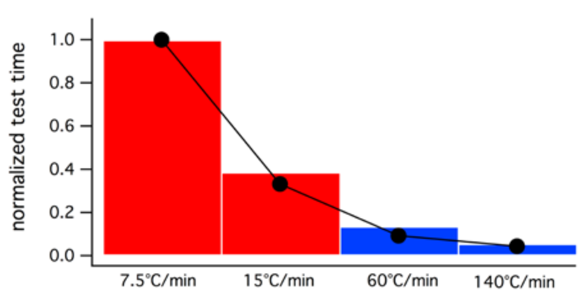

Fig. 9. Resulting accumulated damage from simulated cycles presented in Fig. 4.

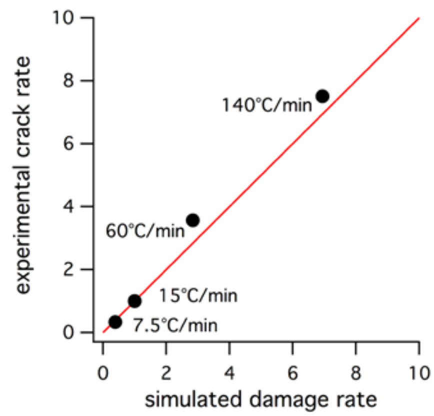

Fig. 10. Comparison of simulation and experiment.

To illustrate the significance of this work, the test time required to complete the current IEC 62108 thermal cycling sequence is considered, Table I. The energy accumulated during the defined test was first simulated [7]. Next, the energy per cycle for two alternative tests was calculated through similar simulations. Reported are both the number of cycles required to achieve a similar amount of thermal fatigue damage as the defined test, and the actual time required to complete the tests. By increasing the temperature ramp rate from the highest IEC definition of 5 °C/min to 15 °C/min the time required to complete an equivalent test is reduced from 28 to 10 days.

TABLE I
EQUIVALENT TEST TIMES FOR INCREASING TEMPERATURE RAMP RATES OF THE IEC 62108 THERMAL CYCLING QUALIFICATION TEST

Option	Ramp (°C/min)	Cycles	Time (days)
TCA-2	5	500	28
TCA-2*	7.5	530	22
TCA-2**	15	350	10

*,** cycle profiles adjusted only by changing temperature ramp rate.

C. Microscopy

Optical micrographs of the test articles cross sections' are presented in Fig 11-14. Imaged in each micrograph is a section of the die-attach crack precipitated through thermal fatigue. Also apparent is the character of the lead-tin solder microstructure, composed of separate lead and tin rich phases. The path of the fatigue crack is consistent through all samples: in the solder near the cell interface.

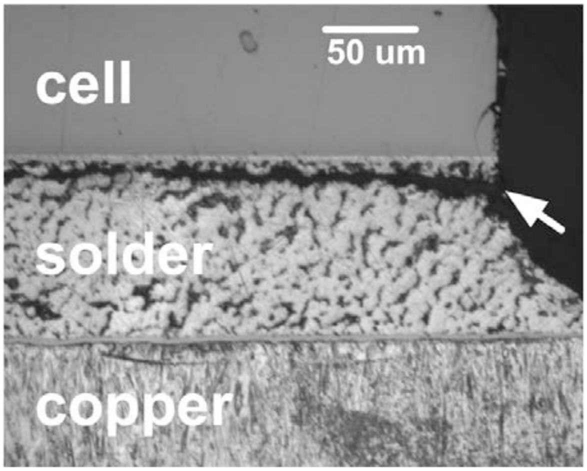

Fig. 11. Optical micrograph of the 7.5°C/min sample illustrating the fatigue crack initiating at the edge of the cell.

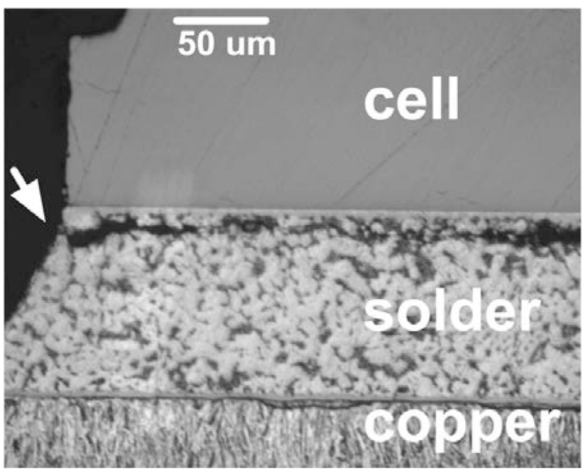

Fig. 12. Optical micrograph of the 15°C/min sample illustrating the fatigue crack initiating at the edge of the cell.

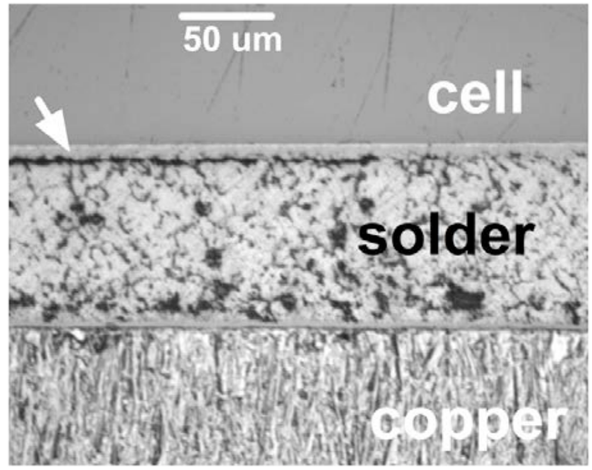

Fig. 13. Optical micrograph of the 60°C/min sample illustrating the fatigue crack initiating at the edge of the cell.

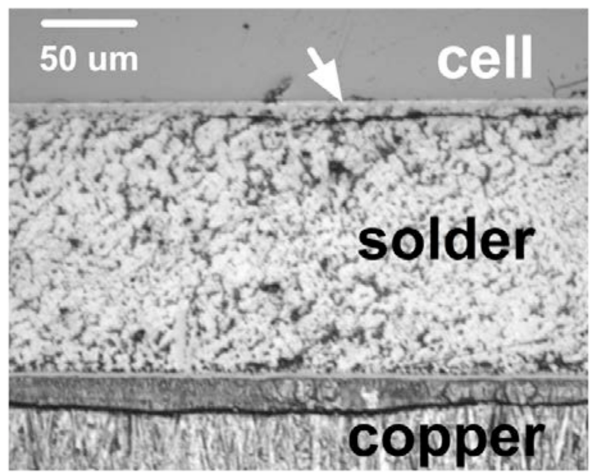

Fig. 14. Optical micrograph of the 60°C/min sample illustrating the fatigue crack initiating at the edge of the cell.

IV. Conclusions

Preliminary simulations indicated that the rate of inelastic energy (damage) accumulation dramatically increases with increasing temperature ramp rates in accelerated thermal cycling. Thermal cycling experiments with temperature ramp rates up to 140°C/min were explored. The resulting experimentally measured crack growth was found to be consistent with FEM simulations. This agreement between simulation and experiment provides confidence for using this simulated energy approach to develop efficient thermal cycling test sequences. The prospect of this work is a significant decrease in overall accelerated test time to reach an equivalent amount of thermal fatigue damage.

Acknowledgement

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