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FINAL REPORT FOR THE

COSMIC RAY SIMULATION AND TESTING PROGRAM

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PREFACE

OBJECTIVE:

The objectives of this study were to:

1. Measure the threshold LETs and cross-sections for single event upset and latchup.
2. Predict the upset and latchup frequency of the test devices in a cosmic ray environment provided by NASA.
3. Correlate the predictions, based on the ground-test data with Space Shuttle results, where possible.

SCOPE OF WORK:

In attaining the above objective, the devices of interest were to be tested with heavy ion and proton beams and the data obtained in these tests were to be used to make predictions of upset in low inclination Space Shuttle orbits. Where possible, these predictions were to be validated by comparison with flight data from the NASA Cosmic Ray Upset Experiment.

CONCLUSIONS:

The required heavy ion and proton data have been obtained and upset rates calculated. In case of the static RAMs tested on the ground and flown on the Space Shuttle, predictions yielded no upsets as the most probable outcome of the Shuttle mission. While this result agrees with the observed lack of upsets in the mission, it does not constitute a validation of the predictive technique.

RECOMMENDATIONS:

The devices which already have been flown, as well as other sensitive ones tested in this study should be flown on polar, or at least high inclination STS orbits.

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I. INTRODUCTION

Various observed anomalies in spacecraft-systems operation have been attributed to upset of electronic logic circuits, stemming from charge generated by the passage of an energetic cosmic ray through a sensitive region of the device. These upsets, termed Single Event Upsets or SEU for short, have been extensively discussed in the technical literature[1-5], and have been simulated in ground tests with beams of heavy ions and protons from nuclear particle accelerators (e.g. Refs. 3-5). The effort described in this report arose as an investigation designed to complement the NASA Cosmic Ray Upset Experiment (CRUX) conducted on several Space Shuttle flights in 1984.[6]

Until approximately five years ago, there was little if any concern in the engineering community about SEU in space programs, especially where spacecraft in low altitude and low inclination orbits were concerned. The need for reliability discouraged the use of state-of-the-art electronic devices. Those actually flown tended to be of the "tried and true" variety, except in relatively few, non-critical applications. These older, small and medium scale integration (SSI and MSI) components are intrinsically hard against SEU. Also, particles with large LET (i.e. high atomic number and low energy) are excluded from the low altitude, equatorial regions around the Earth. Hence few if any SEU were observed on these older, low altitude spacecraft.

In recent years, however, the technology explosion and constantly increasing demand for ever larger and faster information throughput in space have pushed the use of devices at or near the frontier of technology. With more and more VLSI devices being incorporated in designs of future spacecraft, and with VHSIC looming on the horizon, SEU phenomena have become a critical concern of the aerospace engineering community. Both the CRUX program and

this effort were undertaken as a two-pronged campaign to characterize a number of device types already in use or about to be used in NASA space programs, and to validate upset-rate predictions based on ground-test data combined with space-environment models, by comparison with actual flight data. The parts tested under this program are listed in Table 1. Of these, the HM6504 RAMS already have been flown as part of the CRUX Program; the results of the comparison of flight data with ground-test predictions have been published.[6]

II. TEST TECHNIQUES

Ideally, the device characterization tests should be conducted in a way which approximates to the greatest extent possible conditions encountered in space. Such a test procedure implies the use of the same ion species as those present in the space-radiation environment, the procedure also requires that the measurements be performed over a wide energy range for each ion species. Since following such a procedure would be prohibitively expensive, a more practical method, both from the point of view of cost and time, was used in conducting these tests. The method has been described in considerable detail elsewhere.

Briefly, the method relies on the assumption that to first order, particles with the same linear energy transfer (LET) but widely differing atomic number (and hence, energy), will have the same effect on any given device, as far as SEU is concerned. The second assumption is made that to first order, all particle tracks in the sensitive volume produce the same effect, as long as the product of the track length and LET is the same.

A discussion of conditions under which the above assumptions are valid would lead us too far field from the subject of hand. Suffice it to say that

as long as the range of the particles used in the tests is reasonably large in comparison with the distance traversed within the sensitive volume, following the assumptions in the selection of test beams and use of the experimental results in predicting SEU roles leads to conservative results. Thus, a selection of ions is made such as that shown in Table 2, with energies and atomic numbers attainable with an accelerator for which operating costs are not prohibitive. Since changes in particle energy and species are in general very time consuming (and therefore costly), such changes are kept to a minimum. The range of particle atomic numbers and energies is selected to span the range of LET values required to characterize the device response to the environment encountered in space. A more detailed discussion of the experimental techniques used in the present tests follows.

A. Beam-Delivery System

Figure 1 shows the test hardware in schematic form. The beam monitors and the mechanism for rotating and positioning devices under test are located inside the vacuum chamber, when heavy ion tests are conducted. The heavy ion beam enters the chamber at the left, passes through a 0.6 in. diameter collimating aperture and traverses a 0.0001 in. scintillation foil, optically coupled to an RCA8850 photomultiplier tube (PMT). After passing through the foil, the particles illuminate a circular area 0.6 inches in diameter, with the device window test in the center. Every particle reaching the vicinity of the test device must pass through the thin scintillation foil, and in so doing, produce a pulse at the output of the PMT. The pulses are counted and provide a direct measure of the total fluence at the test chip. A remotely controlled shutter, placed between the PMT flux/fluence monitor and the test devices is used to control exposure to the beam. A boron-implanted position sensitive detector, shown mounted near the test devices in Fig. 1, is

used to monitor the beam uniformity. A 1-mm thick surface barrier detector, shown on the right of the chamber in Fig. 1, is used to measure the beam energy. For tests with heavy ions, the test devices must be delidded, since the range of the ions is only a few microns in metals, and tens of microns in silicon. The various relevant properties of the heavy ion beams used in these tests are summarized in Table 2.

During device testing with protons, only the remotely controlled device holder mechanism was used. It was placed in air, near the beam exit port. Dosimetry was performed by means of a thick plastic scintillation counter and activation analysis of metal foils placed in the beam path.

B. Test-Computer Hardware and Software

All of the test devices were exercised with the computer system shown in Fig. 2. The LSI11 computer was located inside the beam cave, close to the vacuum chamber. Communication between the computer and a remote terminal located in the the data-acquisition area was accomplished via an approximately 100 foot long RS232 link. The computer was operated under control of the RT11 operating system. Most of the display and device-excercise software was written in FORTRAN. Programs for testing the microprocessors were written in assembly language.

C. Device Irradiation Procedures

The planned test procedure called for testing at least four devices of a given type, unless device availability, available beam time or the responses of the test devices to the beam dictated otherwise. Unless unusual circumstances existed, an upset threshold and asymptotic cross-section were to be determined for each device type. Because of time constraints associated with tuning the accelerator, all devices were to be tested initially with the

highest LET beam (150 MeV krypton). Subsequently, devices with threshold LET below that of krypton were tested with ions having progressively lower LETs, until the threshold LET was determined.

While undergoing tests, the devices were oriented at various angles to the incident beam, in order to attain intermediate, "effective" LET values (LET divided by the cosine of exposure angle). Care was taken to check that there was agreement among cross-section values obtained with different particles with the same effective LET.

During each irradiation, the device under test was exercised by appropriate software and interrogated for errors. A generalized flow chart of the exercise routines is shown in Fig. 3. At the end of the irradiation, the total numbers of errors in various categories were recorded, together with the accumulated beam fluence, for further off-line analysis.

D. Description of Special Test-Device Software

Each of the device types tested had to have special software written for it. The simplest type of exercise program was that used for testing RAMs like the HM6504, and the MWS5114. Provision was made for reading checkerboard patterns or their complements into the RAMs, holding the information for a predetermined time and checking for upsets. In case of the NSC810, routines designed to exercise the RAM portion of the circuit, output latches A and B, and the timer mode registers were written.

Programs written to exercise the Z-80 and NSC800 microprocessors operated these devices in a single step mode, under control of the LSI11 computer. After each machine cycle, the outputs of the device under irradiation were compared with those of a standard one ("Golden Chip") not in the beam. Upon detection of an error, appropriate information was transferred to

the LSI11 computer and stored in an error table. The error-table data contained the states of the data, control and address bus lines at the time of error detection, and the number of machine cycles from the start of the program loop prior to error detection. As soon as the data were entered into the error table, the LSI11 computer would reinitialize both microprocessors and program execution would start at the beginning.

Several different programs were used to exercise the devices under irradiation, in order to obtain data on as many of the various functional elements of the devices as possible. Software for controlling these devices was written in assembly language.

A slightly different form of the "Golden Chip" method was used to test the 9989 microprocessor. Here the microprocessors were allowed to run in a tight loop under self- control, and were reset when errors were detected by the hardware.

Finally, the M6800 microprocessor was tested while operating in a tight loop under the "Self Test" Method. Several programs were written, in order to identify and accumulate errors associated with the various circuits on the chip.

III. RESULTS AND DISCUSSION

Heavy ions test data have been obtained on all the device types listed in Table 1. Proton tests were carried out on device types where the threshold LET with heavy ions was found to be sufficiently low to render the parts vulnerable to SEU induced by protons via nuclear interactions within the silicon chip. Table 3 is a summary of the proton test results for all of the devices exposed to protons. The number of samples of each device type tested with protons was determined by the available beam time.

A. Latchup and Bit-Error Results for HM6504 Static RAM's

Both the latchup and bit-error data are summarized in Fig. 4. A total of six devices was tested for latchup and bit errors. Results for the individual devices are shown in Figs. 5 to 10. Comparison of the latchup and bit-error cross-sections, plotted as functions of LET, shows the threshold LET for latchup to be approximately twice that for bit error. The latchup cross section is at least a factor of ten less than the bit-error cross-section in the equilibrium region of high LET.

Because of time constraints, extensive latchup data were obtained only on two devices, and these data are shown in Fig. 4. The order of magnitude difference in the respective latchup cross-sections for the two test devices, is representative of the variability in latchup cross-sections observed in the course of other device tests. Latchup has been observed in all devices during SEU testing. Figures 5-10 indicate the range of LETs for which latchup was seen to occur.

Turning to the bit-error results for the individual samples (Figs. 5-10), we note that all the cross-sections reach approximately the same equilibrium value at high LET, in the neighborhood of 4×10^{-3} cm^2/device. In contrast to the above trend, the threshold LET values are scattered over an LET range between 5 and 15 MeV-cm^2/mg. Within the statistics of the available data, the differences in threshold LET are not related to the differences in lot or date code.

The above heavy ion test results strongly suggest that the SEU rate due to proton induced interactions should be negligible in comparison with that due to heavy ions. The number of nuclear reaction channels corresponding to the charge deposit equal or greater than that produced in the same region

by a single ion with an LET of approximately 10^{-9} is severely limited - hence the number of expected upsets will be small. The proton-test results certainly bear out that hypothesis. With 200 MeV protons, somewhere between 10^9 and 10^{10} protons/cm2 are needed to produce one upset. Upsets were observed in the samples with threshold LET between 5 and 10 MeV-cm^2/mg (samples 6 and 11) while none were seen in sample 8, with a threshold LET of approximately 15 MeV-cm^2/mg. No upsets at all were observed with 100 MeV protons. The above results are consistent with the often used empirical rule that devices with threshold LET for upset above 10 MeV-cm^2/mg are hard against proton-induced upsets.

No latchup was observed with any of the proton irradiations. Again this is not surprising, in view of the higher threshold LET and drastically lower cross-section for latchup measured with heavy ions.

B. Results for the MWS 5114 1Kx4 Static RAM

As befits a RAM based on CMOS/SOS technology, the data in Fig. 11 show the MWS5114 devices to have a relatively high LET threshold for SEU. If one neglects the possibility of funneling, it is easy to estimate the critical charge for upset. Given the epi-layer to be 0.5 micron thick and taking the LET threshold from Fig. 11 as 60 MeV-cm2/mg (0.6pC/micron), we obtain 0.3pC for the critical charge. A circuit analysis such as a SPICE simulation should be performed to obtain a critical charge prediction for comparison with the above unambiguous result. Note that the asymptotic value of the cross-section could not be reached with the particle beams available at the 88-inch cyclotron. However, this is only of academic interest, since with a 60 MeV-cm^2/mg threshold LET the expected upset rate in space is negligible. Because of the high threshold, the device was not tested with protons.

C. The XICOR 2816A PROM results

During the initial beam exposures, the response of this device was quite puzzling, and a couple of iterations of testing and data analysis were needed before the results shown in Figs. 12 and 13 were understood. The effects observed in these early tests were 1) permanent failure with anomalously low fluences of particles, 2) latchup requiring a power interruption for recovery, 3) latchup with spontaneous recovery after several seconds ("pseudo-latchup"), and 4) bit errors observed both during the write cycle and quiescent state (PROM deselected). With protons, only the first effect above could be observed, since the devices died following exposures of a few seconds' duration.

After a period of anxiety occasioned by the unexplained device failures in the initial heavy ion and proton exposures, we learned that the parts were apt to fail following exposure to several hundred rads(Si). A check of total fluences of particles to which the failed devices had been exposed, confirmed that the failures were due to total dose. The proton data showed, in this new light, that total dose failure is apt to occur before observation of upset. Subsequently heavy ion tests were performed in a second effort to obtain some upset data. These tests were designed to minimize the total dose delivered to the devices in the course of the testing. The limited data obtained in these later tests are summarized in Figs. 12 and 13. No proton-induced upsets were observed.

D. The NSC810 Two-Port RAM and Timer Results

This device consists of a RAM accessed via two ports whose output can be latched, and a timer-register. All of the above elements on the chip are vulnerable to SEU, and the test results are presented in Figs. 14-17.

As Fig. 14 shows, this device type exhibits heavy ion induced latchup. However, the cross-section for latchup appears to be between one and two orders of magnitude less than the latchup cross section seen in the HM6504 RAMs. Moreover, the latchup cross section in the NSC810 is more than three orders of magnitude less than the total upset cross-section. This implies that only a small portion of the circuit elements on the chip is susceptible to latchup. Comparison of the threshold LET for latchup in Fig. 14 with threshold LETs for bit error in Figs. 15, 16 and 17 shows that only the RAM has a lower threshold for bit error than the measured latchup threshold. This observation implies that latchup is somehow associated with elements on the RAM portion of the chip.

The data in Figs. 15-17 suggest that a careful analysis of the device circuits and mask design could yield very useful results for estimating SEU rates in more complex devices of the 800 family, such as the microprocessor discussed below. Vulnerabilities to SEU of three different functional elements on the chip have been measured, and it is not outside the realm of possibility that these form a significant subset of building blocks in the more complex devices, not as amenable to testing.

No proton tests were carried out on these devices because of the relatively high threshold LETs for the various circuits with heavy ions.

E. The NSC800 Microprocessor Results

Latchup, as well as SEU were observed in the NSC800 microprocessor. Because of the complexity of the test hardware, resetting of the system after occurrence of latchup required considerable time and was wasteful of the expensive beam time. Consequently, only limited data on bit-error type upsets were obtained for these devices. The data are summarized in Fig. 18. Avail-

able beam time did not permit a threshold LET determination with heavy ions or any testing to be performed with protons.

F. The Z-80 Microprocessor Results

A complete and thorough reduction of upset data obtained while running the various programs during the cosmic ray simulation tests requires laborious analysis of the error table values associated with each upset, and a detailed knowledge of the duty cycle associated with the instruction being executed when the error occurred. For each of the several exercise programs executed in the course of the particle irradiations, the errors associated with each instruction were combined in several categories and stored on floppy disks in the form of LOTUS files for further analysis. Such an analysis has been performed and published in Ref. 7.

A summary of the test data is shown in Fig. 19, where the upset cross-sections for various programs are plotted as functions of LET. The cross-sections are given on a per-bit basis, with a register-usage factor provided for each program. This factor represents an average number of the 26 8-bit registers utilized in the course of execution of any of the test programs. Thus, the upset cross-section per device is obtained by multiplying the value in Fig. 19 by eight times the appropriate usage factor. Because of the uncertainties associated with the identification of individual errors and poor statistics associated with many of the data points, the error associated with each data point is ± 50% of the plotted value.

In the course of testing the Z-80 microprocessor, the heavy ion LET was decreased until almost two orders of magnitude in LET were spanned. Despite that fact, and an absolute threshold LET could not be reached. The upset cross-section extends over more than three orders of magnitude in this

LET range, indicating interplay of many elements with widely different threshold LETs. A rigorous calculation of the upset rate for this device in space would require a great deal of effort, but a reasonable estimate might be made by an appropriate weighting of the cross-sections associated with the various functional elements identified on the device.

As might be expected with the low threshold LET for upset of the device, upsets were observed during tests with protons. The results are summarized in Table 3.

G. Results for the 9989 Microprocessor

The tests on these devices were conducted in collaboration with D. Platteter and T. Ellis of the Naval Weapons Support Center. The results of these tests were analyzed by them, and are plotted in Fig. 20. Fig. 21 shows the same results superimposed on similar data obtained in 1981 by Price et al.[8]. The agreement between the two sets of data is reasonably good, despite the fact that the devices tested under this program came from different lots and date codes. This agreement contrasts sharply with the fact that these latter devices have been found to be significantly softer to total dose than the ones tested by Price et al.

H. The M6800 Microprocessor Results

Summaries of the various types of test results are shown in Figs. 22, 23 and 24. Of all the microprocessors tested, this one was subjected to the most comprehensive series of tests. The "semi-static" tests for which results are shown in Fig. 22, were essentially simple RAM-type tests, where vulnerability of the various registers was measured. The absolute upset threshold LET lies value between 2 and 3 MeV-cm2/mg, and the asymptotic cross section ranges between approximately 4×10^{-6} and 1.5×10^{-5} cm^2/bit, with the

program counter having the highest cross section and the flag register the lowest.

Turning to the "semi-dynamic" tests (Fig. 23) involving transfers of data between groups of two registers, some interesting features are observed. First of all, we note that the open circle and square data points, representing repeated transfers of data between A and B registers, and between the stack pointer and index register, respectively, have essentially the same values as their counterparts in the "semi-static" tests. On the other hand, as soon as the transfer takes place via the ALU (open triangles), the upset cross section takes on the values corresponding to those for the program counter. A combinatorial analysis, involving all of the functional elements tested and duty cycles associated with a "typical" program can then be performed to obtain a composite cross-section curve for computing upset rate in space. A simplified form of such an analysis has been performed and published in Ref. 9.

In addition to the above tests, the devices were irradiated while executing special software supplied by NASA/Goddard. Results from runs using this software are shown in Fig. 24. We see that within experimental error, the data for the two devices are in agreement. Furthermore, we note that the NASA program cross-section and LET threshold have values close to those for the program counter (counting all 16 bits). Since the data stored in the program counter are always subject to upset (100% duty cycle) the upset rate of a microprocessor in space can be expected to be dominated by the program-counter upset rate, unless elements with lower rate duty cycles are exceptionally vulnerable. If indeed the program counter dominates the upset rate, we would not expect that latter to be very program-dependent.

As can be seen from Table 3, two devices were tested with protons at 100 and 200 MeV. No upsets were observed at either energy, following exposure to a fluence in excess to 10^{11} protons/cm^2.

IV. ERROR RATE PREDICTIONS

Accurate prediction of error rates in space requires a detailed knowledge of mask geometry, process, and circuit design of the devices under study. Given the above data together with accurate environment models and test results, we should be able to compute with reasonable precision the device response to the environment in question. Unfortunately, experience shows that the above ideals are rarely if ever achieved, so less precise but nonetheless believable methods must be resorted to. One such technique is the semi-empirical approach of E. Petersen[10], which applies to regions of space not strongly affected by the Earth's magnetic field, at times near solar minimum. This method yields conservative estimates of upset rate caused by galactic cosmic rays under the conditions stated above. Since for purposes of this study predictions are needed for orbits where the influence of the Earth's magnetic field is quite strong, we used a different technique. In this approach, we assumed that a "typical" sensitive region for the devices under study has the dimensions close to 10x10x1 microns. We then modified the CRIER program[11] by introducing the cosmic ray environment at the 300 nautical-mile equatorial orbit (provided by E. G. Stassinopoulos of NASA/GSFC), and computed the upset rate of this "standard" cell as a function of critical charge, as shown in Fig. 25. Note that for a device with a 1 micron thick sensitive region, the critical charge is equal to the threshold LET in pC/μ. In case of the MWS 5114 RAM, the actual thickness of the epitaxial silicon layer (0.5 micron) was used to compute the critical charge

from the measured threshold LET. The upset rates shown in Table 4 were then computed by multiplying the upset rate in Fig. 25 corresponding to the appropriate critical charge by the ratio of the measured device cross-section area to the area of the standard cell (100 μm^2).

In computing the upset rate for the Z-80 microprocessor, two threshold LET values and two corresponding cross-sections were assumed. For purposes of obtaining an upset-rate prediction, per bit cross-section values of 8×10^{-7} and 2×10^{-5} were multiplied by an assumed usage factor of 10 to obtain the per device cross-sections of $(8 \times 10) \times 8 \times 10^{-7} = 6.4 \times 10^{-5}$ cm^2 and $(8 \times 10) \times 2 \times 10^{-5} = 1.6 \times 10^{-3}$ cm^2, corresponding to the respective LET values of 1 and 5 MeV-cm^2/mg. The total upset rate is the sum of the two values given in Table 4.

The calculations leading to the results in Table 4 assume that the cross-section as a function of LET is a step function. Since in reality this is not the case, a threshold LET value higher than the absolute threshold must be assumed to give a realistic result. In the present calculations, the LET value at which the cross-section assumes one tenth its asymptotic value was assumed to be the threshold LET. While we believe the upset-rate predictions in Table 4 to be conservative, they should be regarded as no more than order-of-magnitude estimates of the true rate.

V. SUMMARY AND CONCLUSIONS

Single event upset and latchup vulnerabilities have been determined for a number of parts of interest to NASA space programs. In cases where a threshold LET for SEU could be measured, an upset rate in a low inclination Space Shuttle orbit has been computed. As expected, the predicted upset rates are

extremely low, except for the devices with LET thresholds below the geomagnetic cutoff for altitude and inclination of the Space Shuttle orbit. While some of the devices do exhibit latchup, the cross-sections and threshold LETs are such that the risk associated with flying these devices in low, near-equatorial orbits is small if not negligible. For polar orbits, a more careful risk assessment should be made.

Finally, where proton upsets are concerned, even in the case of the part with the lowest threshold LET (the Z-80), the upset cross-section is approximately 1E-9 at 200 MeV. Thus, except perhaps in the heart of the inner zone and for extremely large memories, the upset rate due to protons will be negligible.

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Table 1. List of Test Devices and their Descriptions

Part #	Manufacturer	Technology	Functional description
HM6504	Harris	CMOS/Bulk	4Kxl Static RAM
MWS5114	RCA	CMOS/SOS	4Kxl Static RAM
X2816A	Xicor	N-Ch F/G MOS	EEPROM
Z-80	Zilog	NMOS	Microprocessor
NSC800	National	CMOS/Bulk	Microprocessor
NSC810	National	CMOS/Bulk	Two-port RAM and timer
SBP9989	Texas Inst.	Bipolar/I^2 L	Microprocessor
M6800	Motorola	NMOS	Microprocessor

Table 2. Heavy Ion Beams Used for SEU Testing

Ion	Atomic No.	Energy (MeV)	LET (Mev cm^2/mg)	LET ($pC/\mu m$)
Krypton	36	150	39.9	0.4
Argon	18	84	17.7	0.18
		176	14.3	0.14
Neon	10	92	5.5	0.055
Oxygen	8	32	5.3	0.053
		150	2.2	0.022
Nitrogen	7	69	2.8	0.028
Carbon	6	121	1.2	0.012
		240	0.7	0.007
Helium	2	48	0.6	0.006
Hydrogen	1	100	0.0058	5.8×10^{-5}
		200	0.0037	3.7×10^{-5}

Table 3. Summary of Proton-Test Results

Device Designation	Number of Samples Tested	Proton Energy (MeV)	Upset Cross-Section (cm^2/device)
HM 6504	3	100	$< 2 \times 10^{-10}$†
	3	200	$(1 \pm 0.5) \times 10^{-10}$
X2816A	2	100	$< 5 \times 10^{-11}$†
	1	200	$< 5 \times 10^{-11}$†
Z-80	3	100	$(2 \pm 1) \times 10^{-10}$
	2	200	$(2 \pm 0.6) \times 10^{-10}$
M6800	2	100	$< 1 \times 10^{-11}$†
	2	200	$< 1 \times 10^{-11}$†
SBP9989	2	100	$< 1 \times 10^{-11}$†
	2	200	$(1 \pm 0.8) \times 10^{-11}$

†Upper limit - no upsets seen.

Table 4. Measured SEU Parameters and Upset-Rate Predictions

Part #	LET Thr. (MeV-cm^2/chip)	Q-crit. (pC)	Cross-sect. (cm^2/chip)	Upset rate (upsets/chip-day)
HM6504	10	.1	$3x10^{-3}$	$1.1x10^{-7}$
MWS5114	60	.3	4×10^{-5}	$< 1.0 \times 10^{-10}$
X2816A	5	.05	5×10^{-5}	4.5×10^{-7}
Z-80	5	.05	$1x10^{-3}$	1.6×10^{-6}
		.01	$2x10^{-5}$	2.6×10^{-5}
SBP9989	10	0.1	$2x10^{-4}$	$7.2x10^{-9}$
M6800	5	.05	$3x10^{-4}$	$2.7x10^{-7}$
NSC810	18	0.18	$4x10^{-3}$	$< 1.0 \times 10^{-10}$

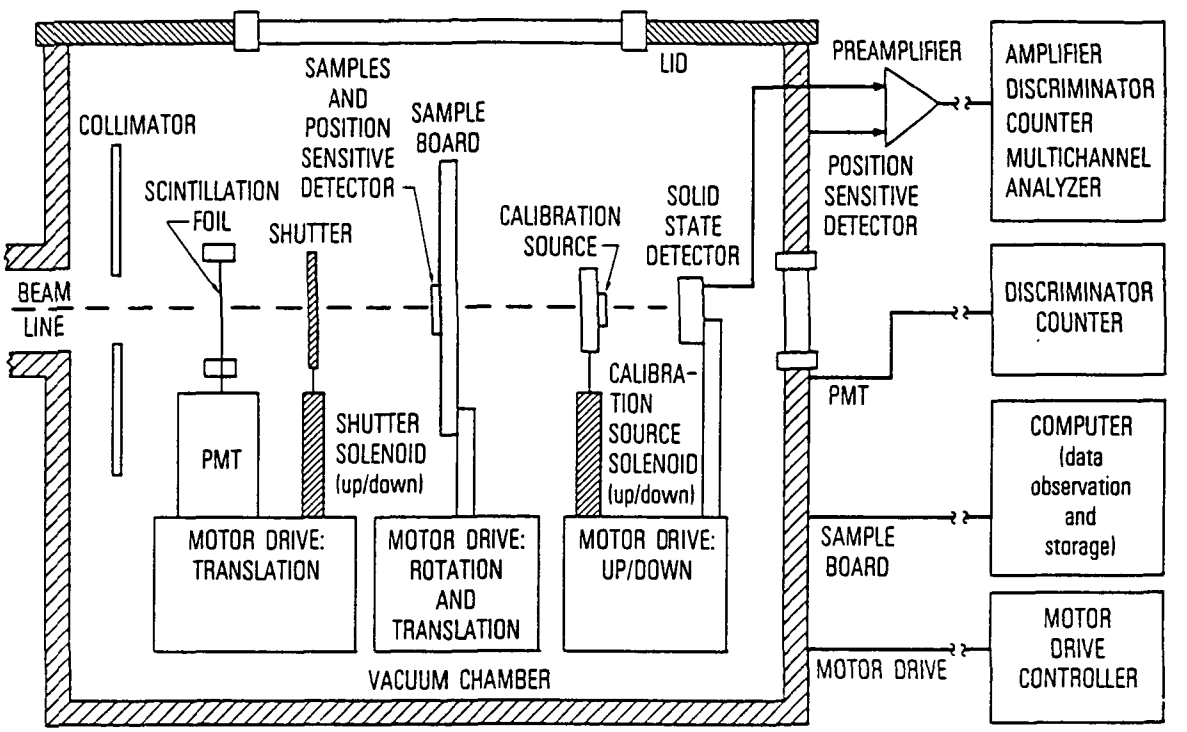

Fig. 1. Schematic representation of test hardware.

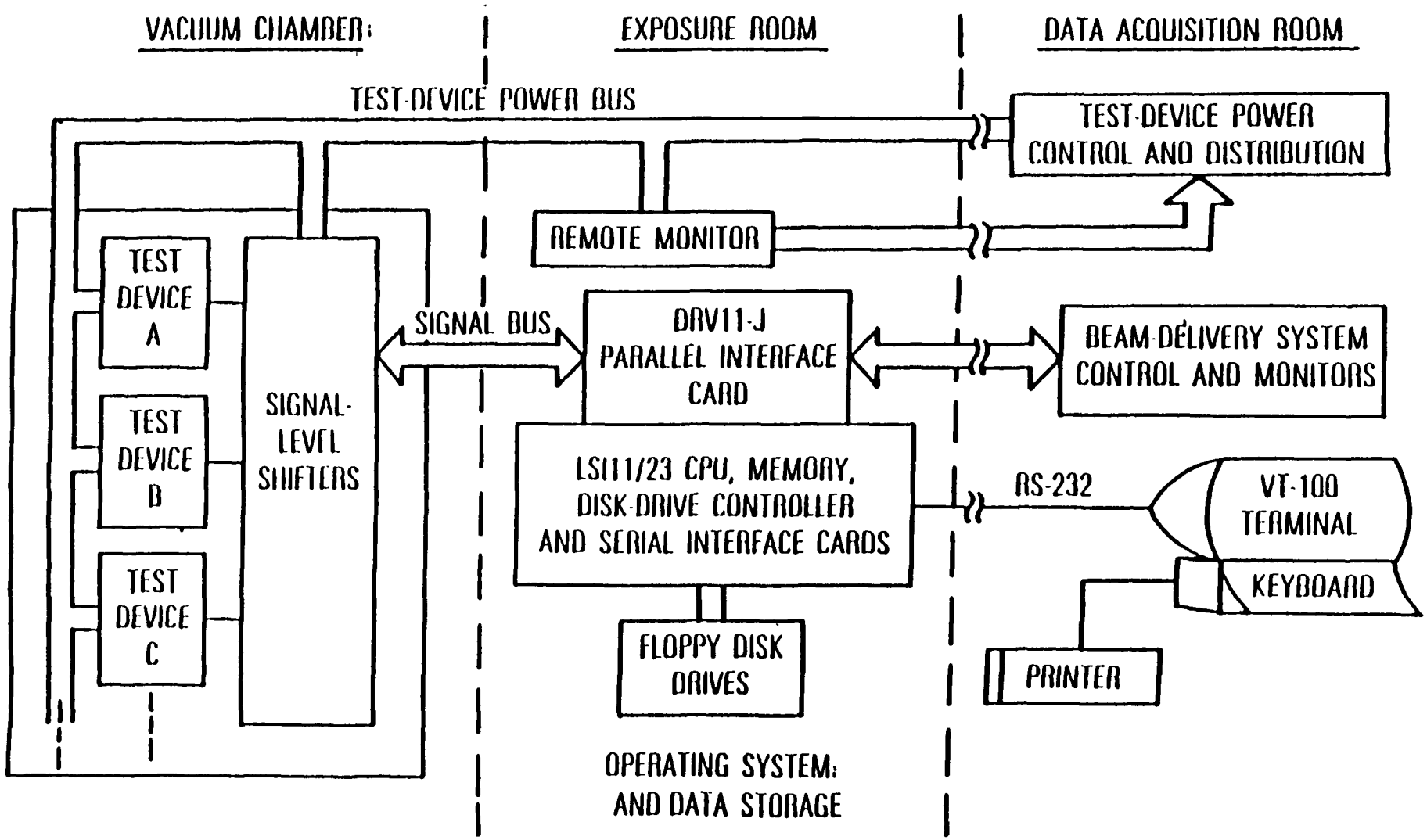

Fig. 2. Block diagram of test computer.

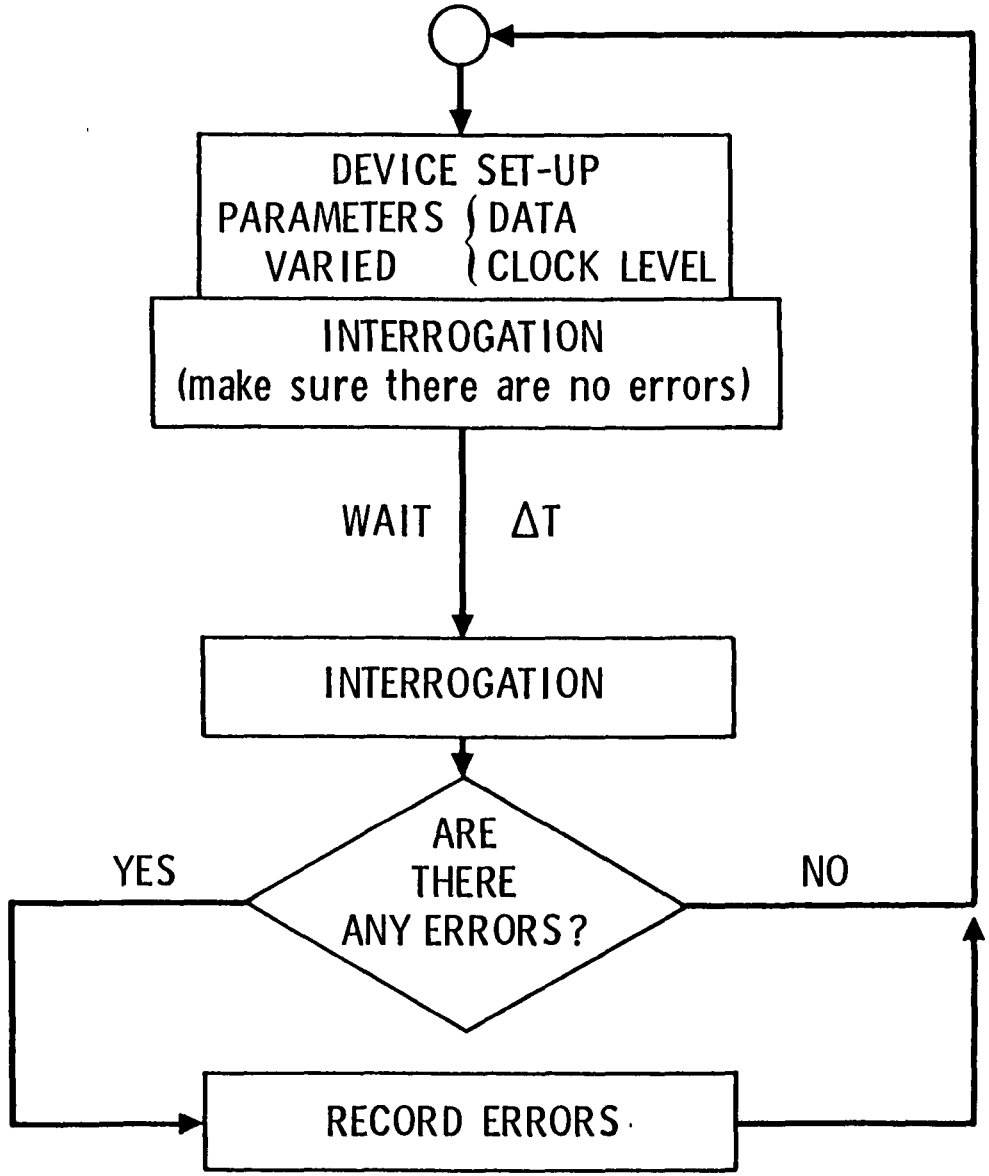

Fig. 3. Generalized flowchart of an exercise routine.

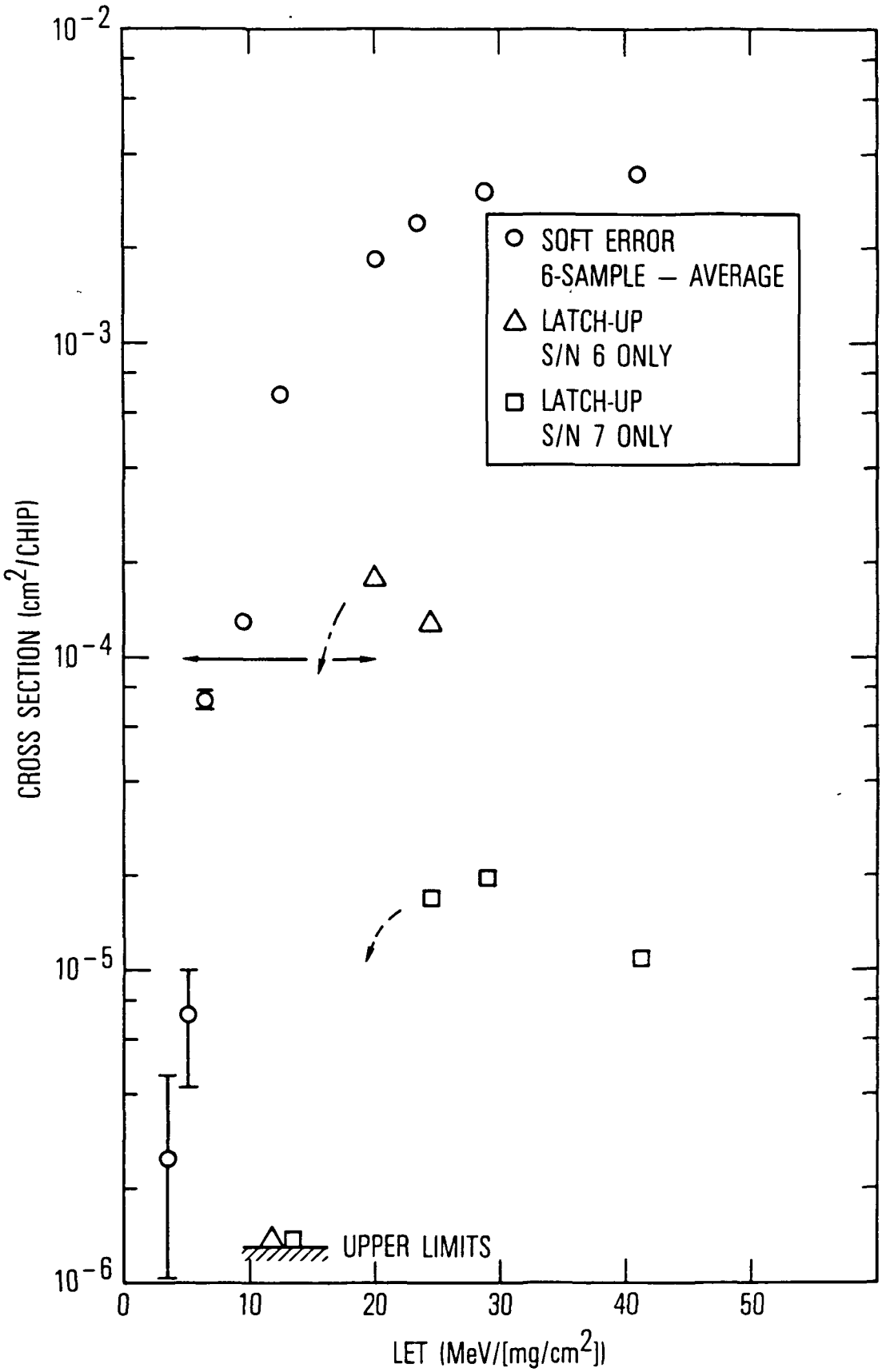

Fig. 4. Summary of HM6504 results.

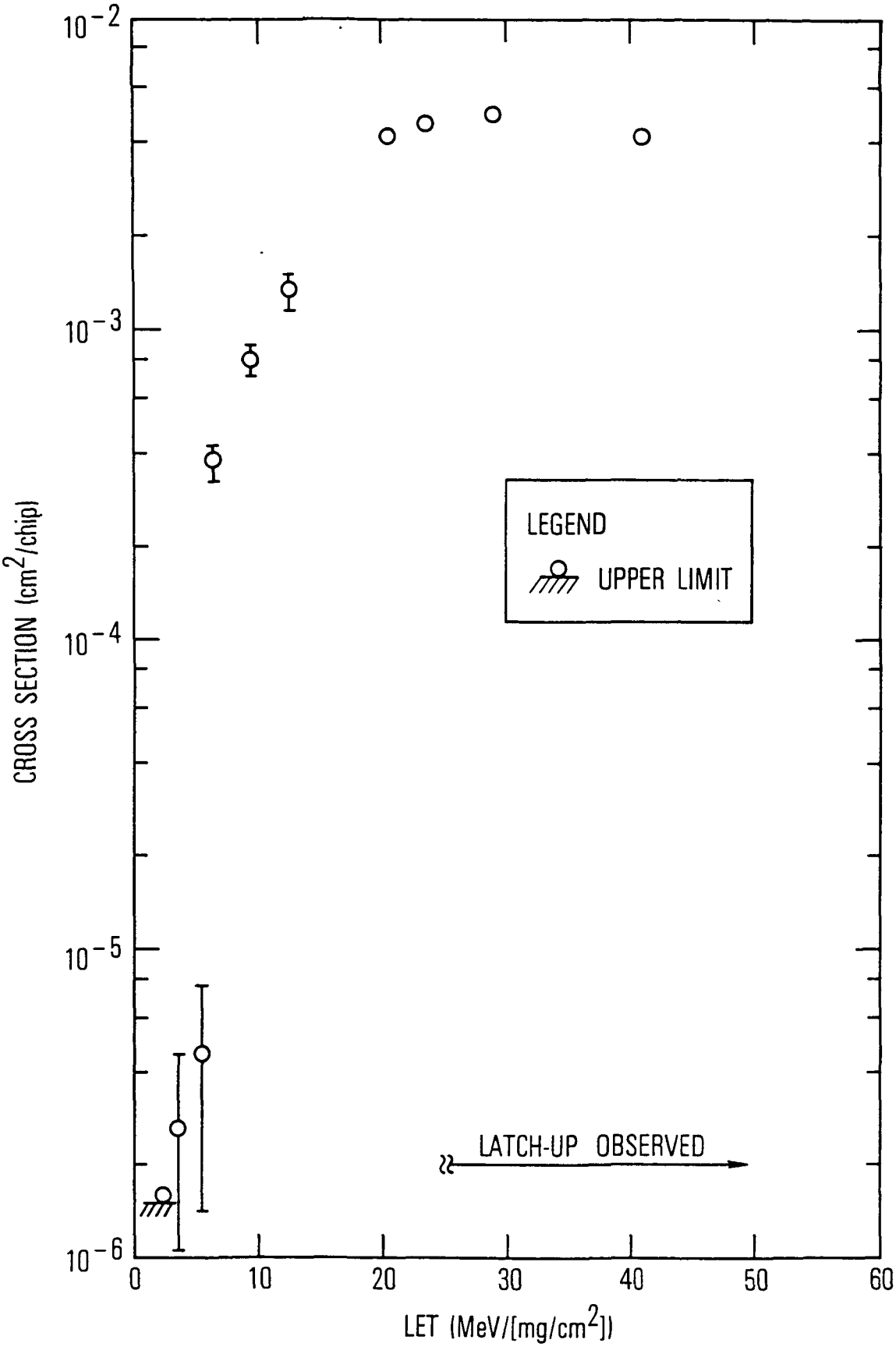

Fig. 5. HM6504 sample 5 results.

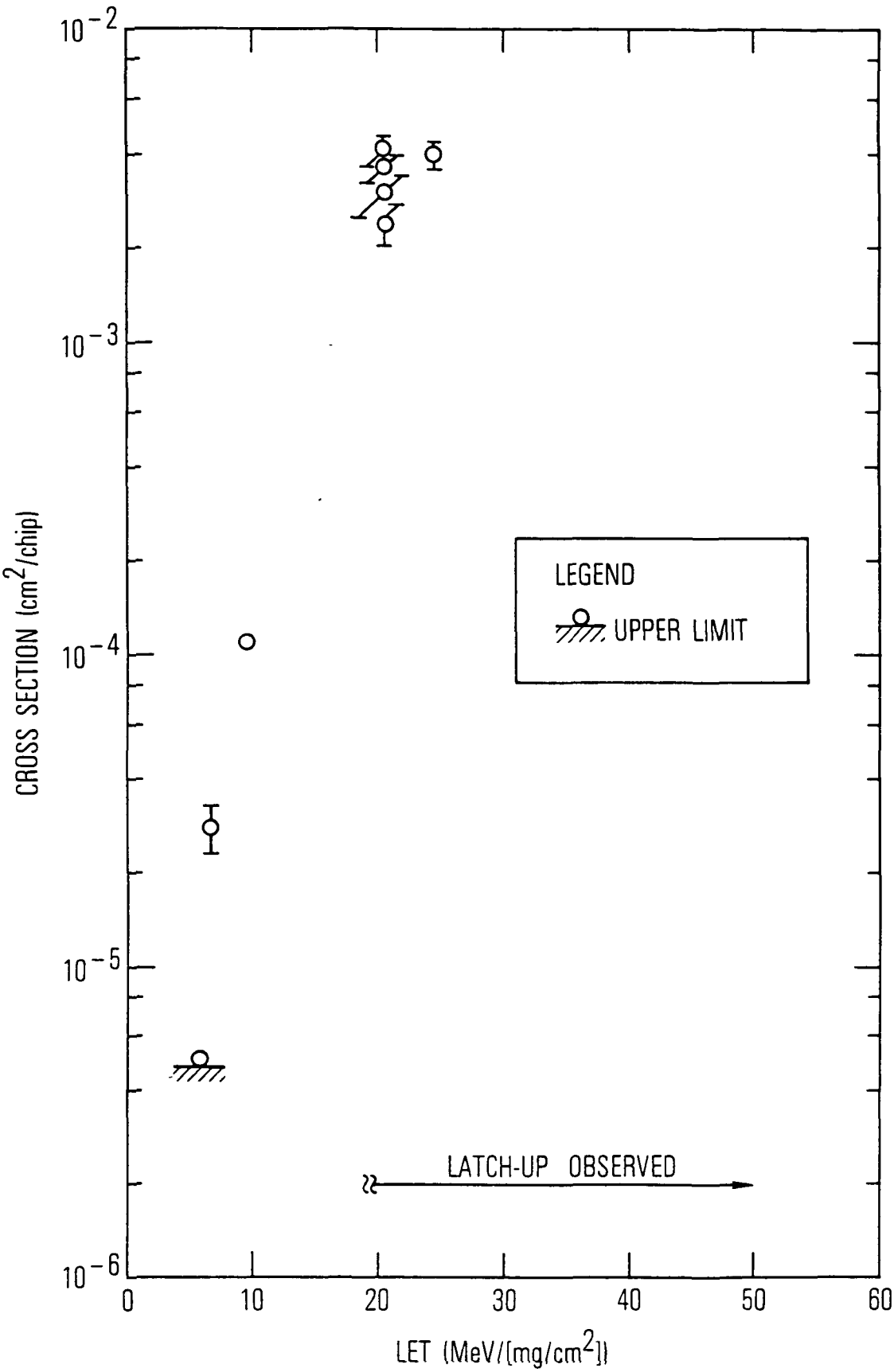

Fig. 6. HM6504 sample 6 results.

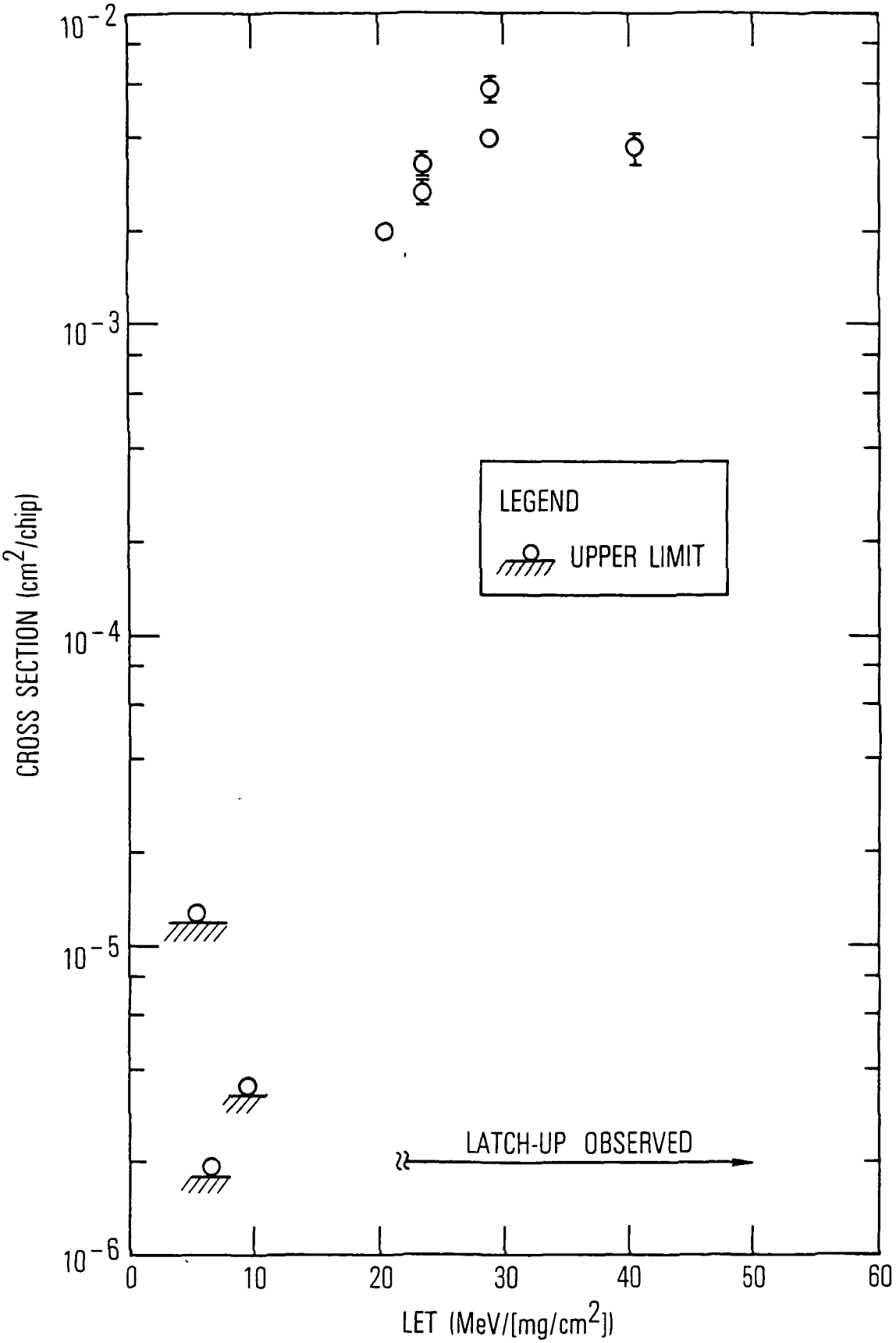

Fig. 7. HM6504 sample 7 results.

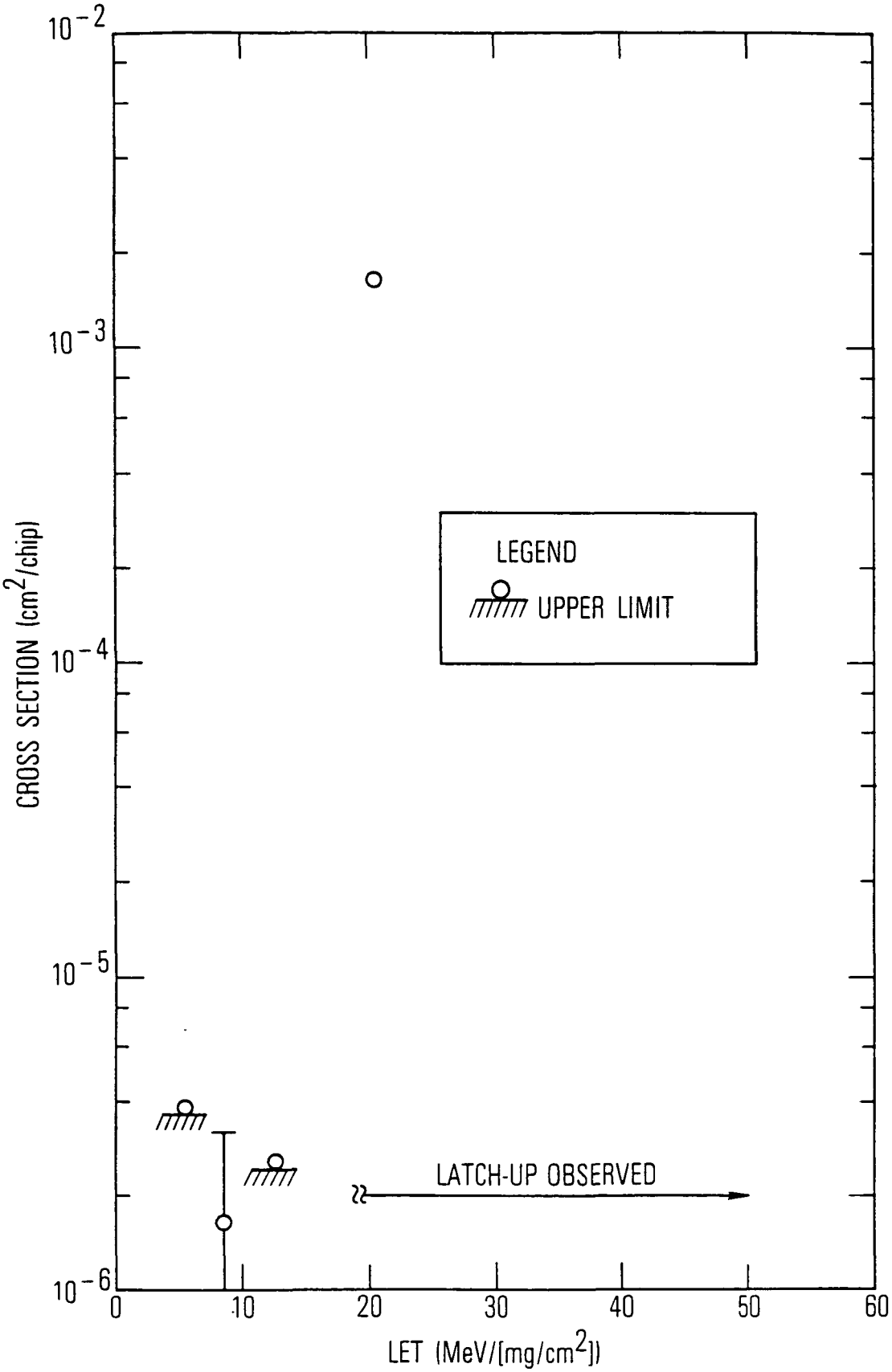

Fig. 8. HM6504 sample 8 results.

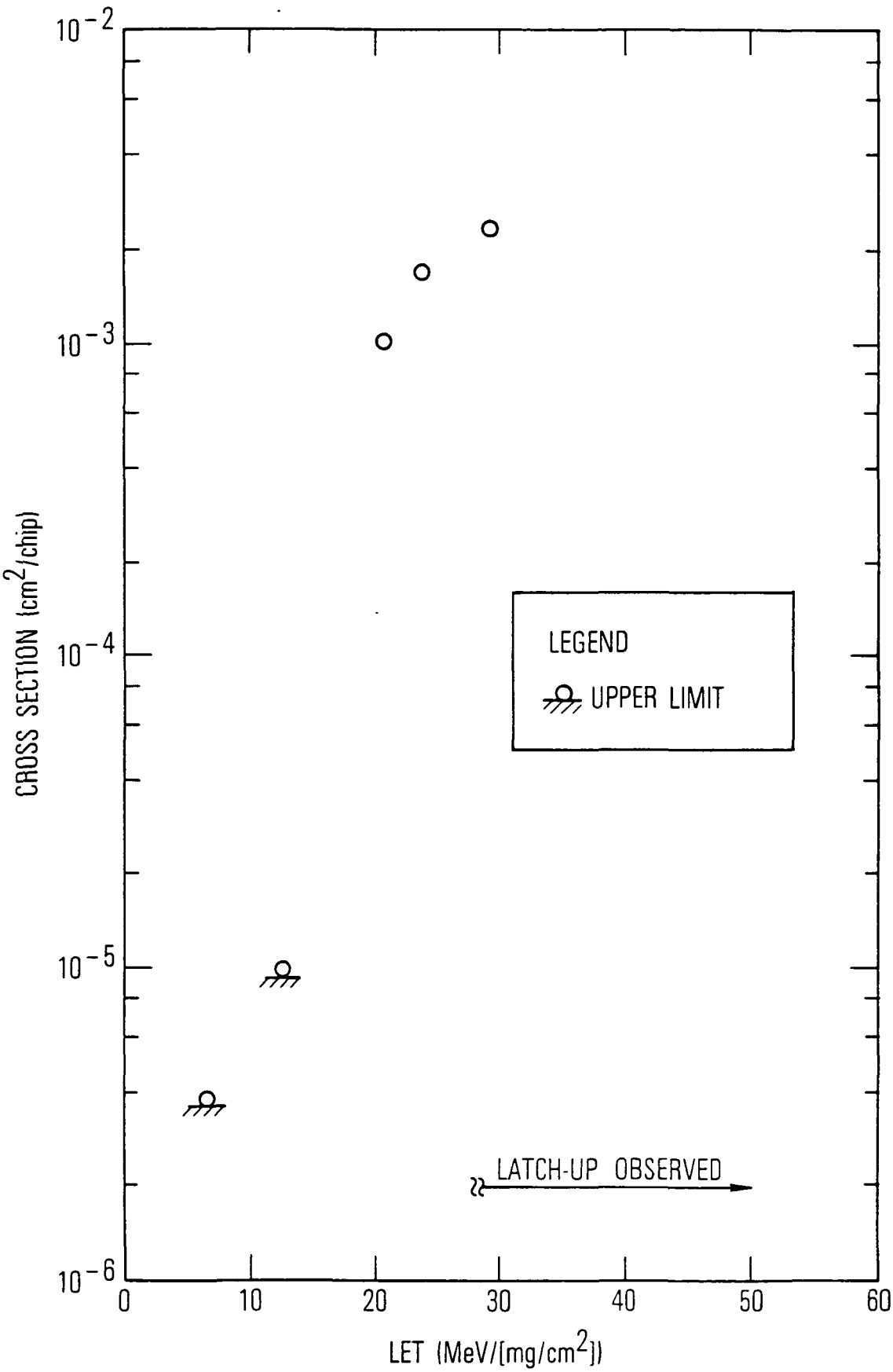

Fig. 9. HM6504 sample 10 results.

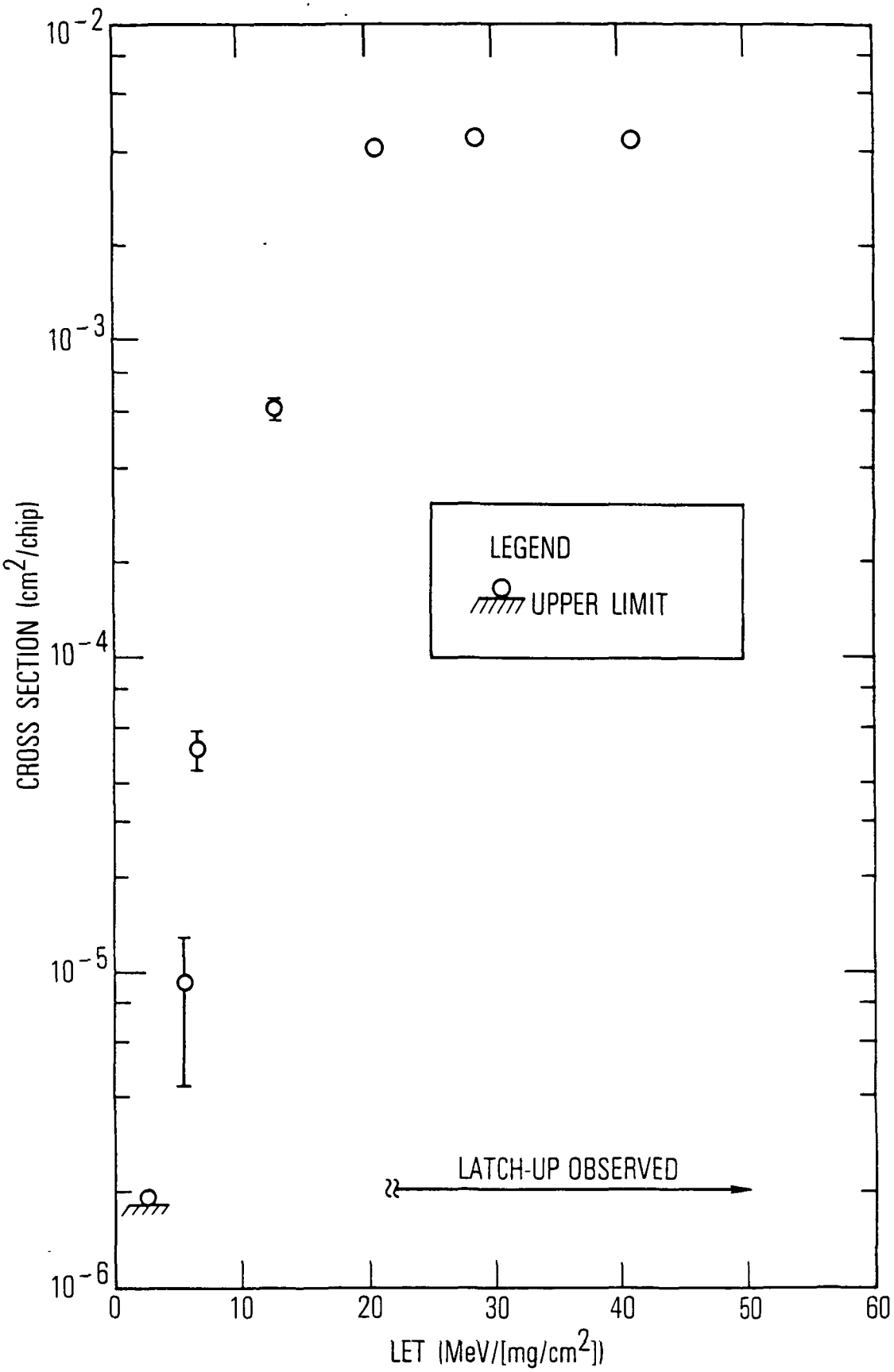

Fig. 10. HM6504 sample 11 results.

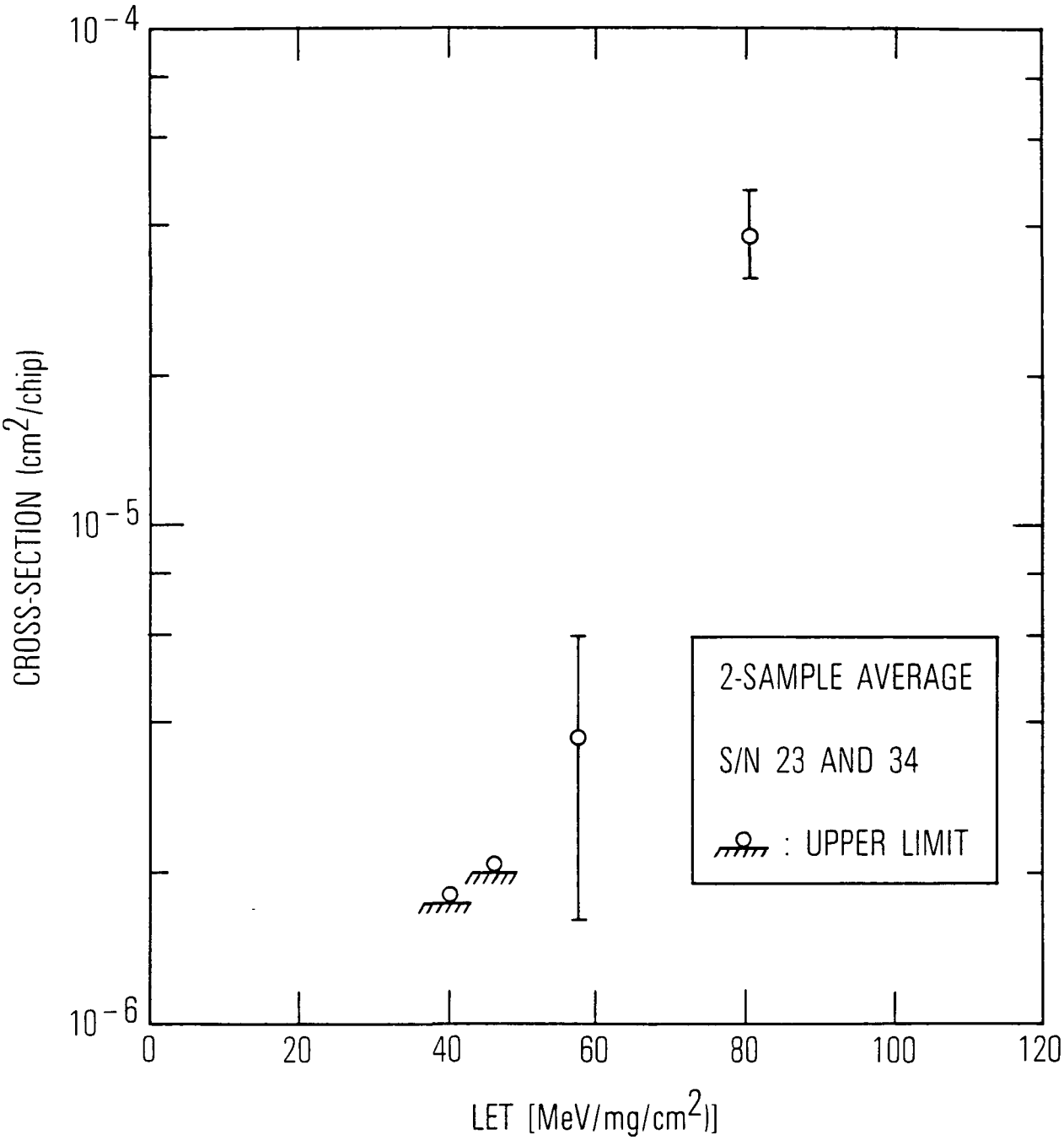

Fig. 11. MWS5114 results.

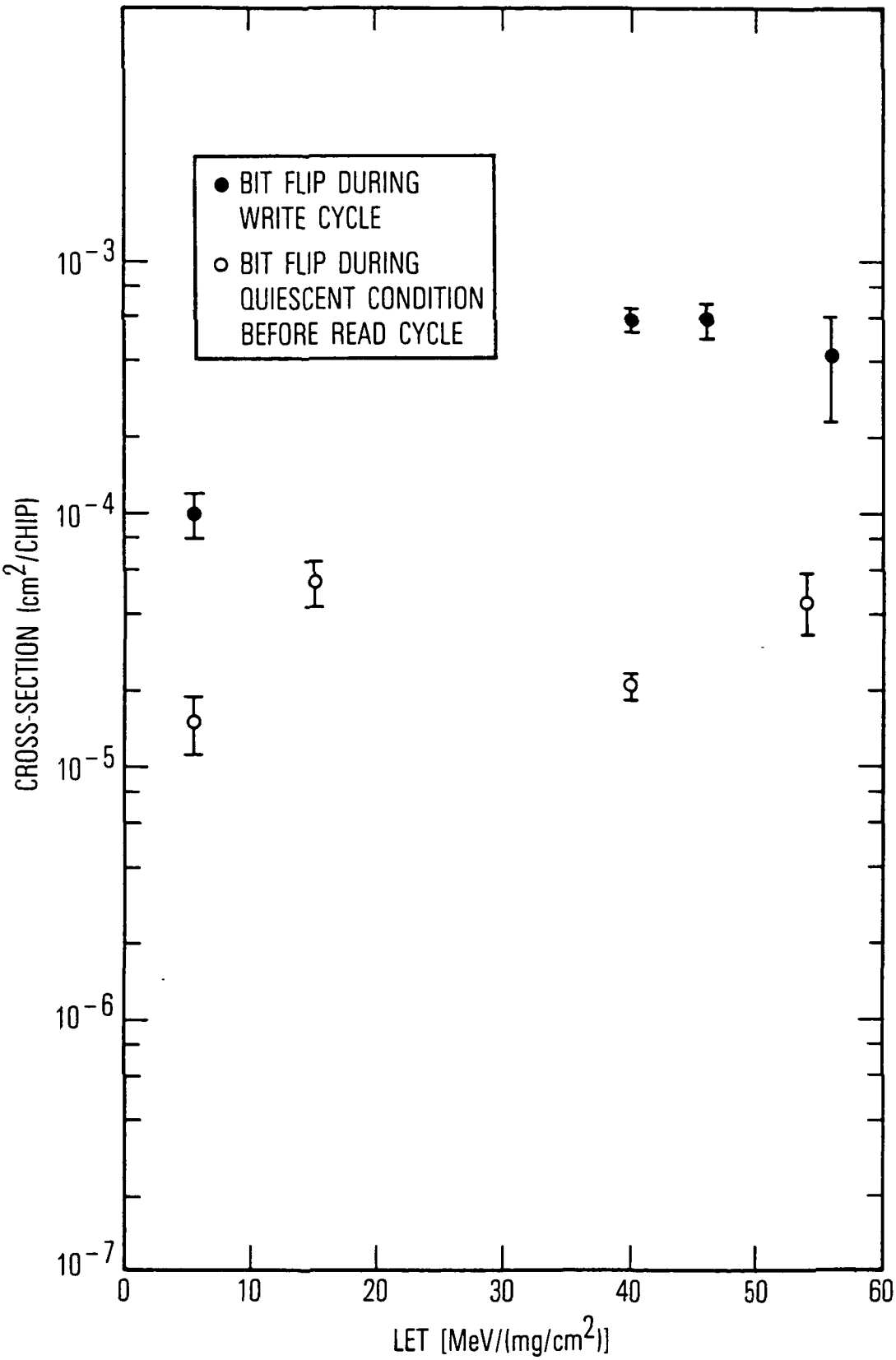

Fig. 12. XICOR 2816A results: SEU.

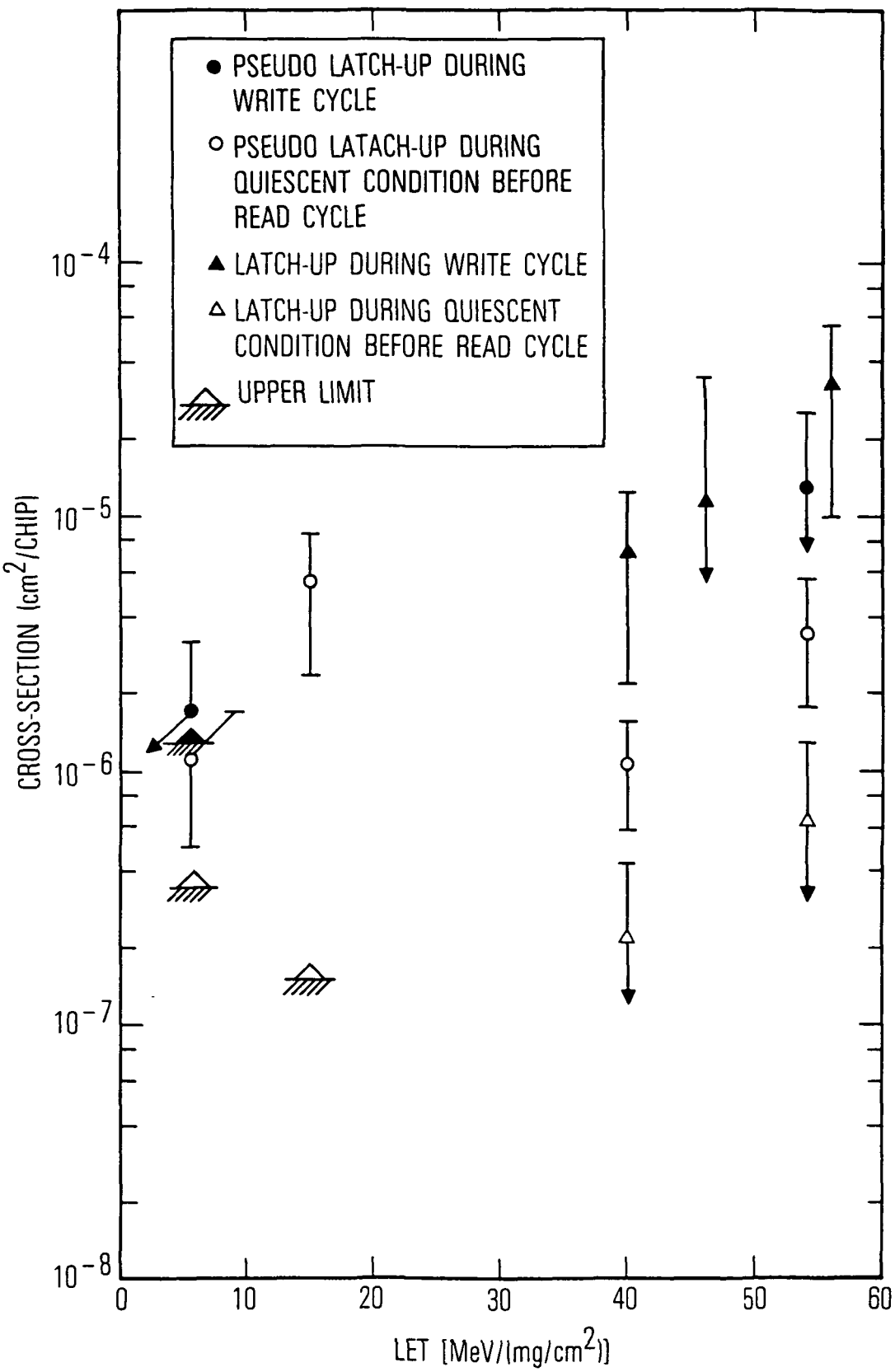

Fig. 13. XICOR 2816A results: latchup.

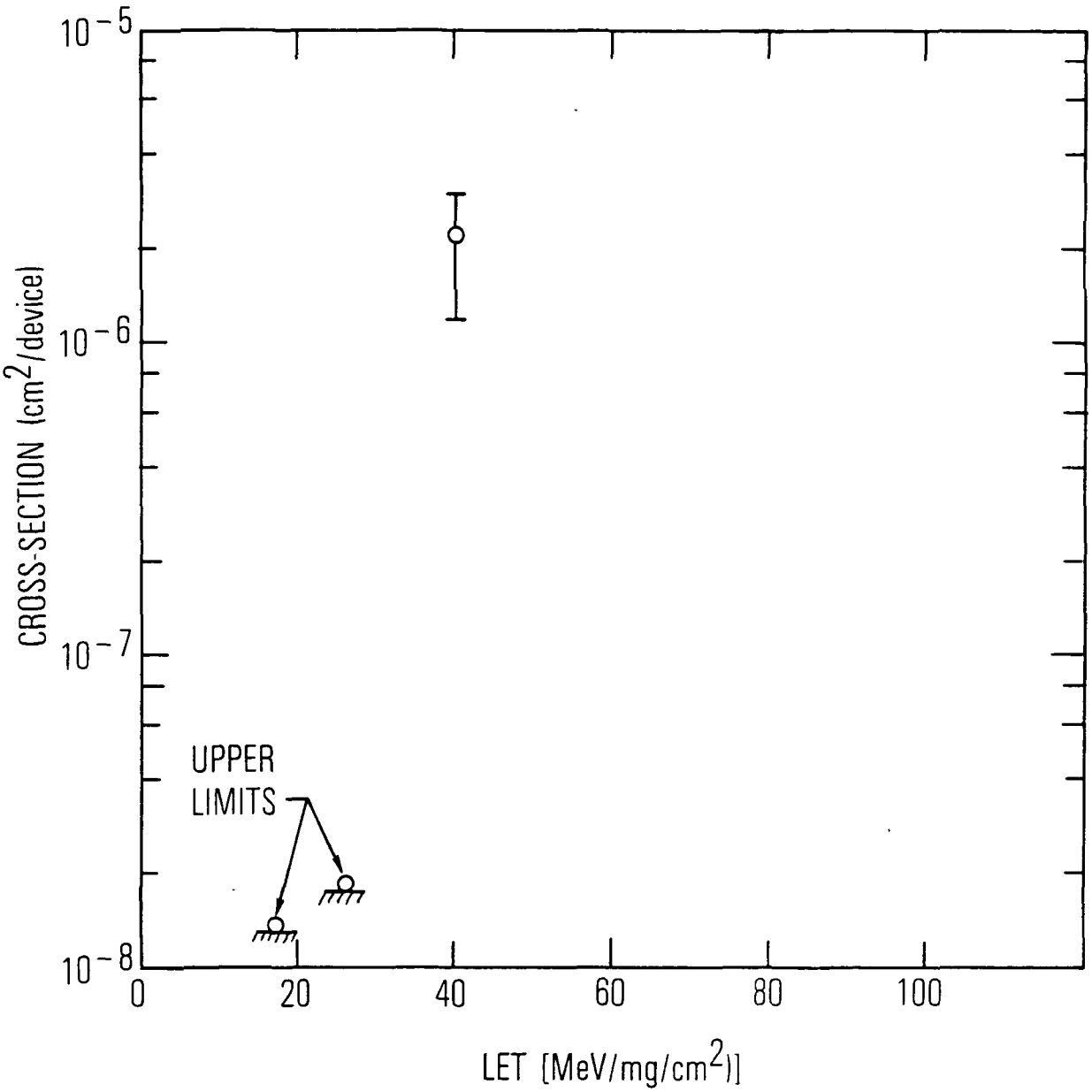

Fig. 14. NSC810 results: latchup.

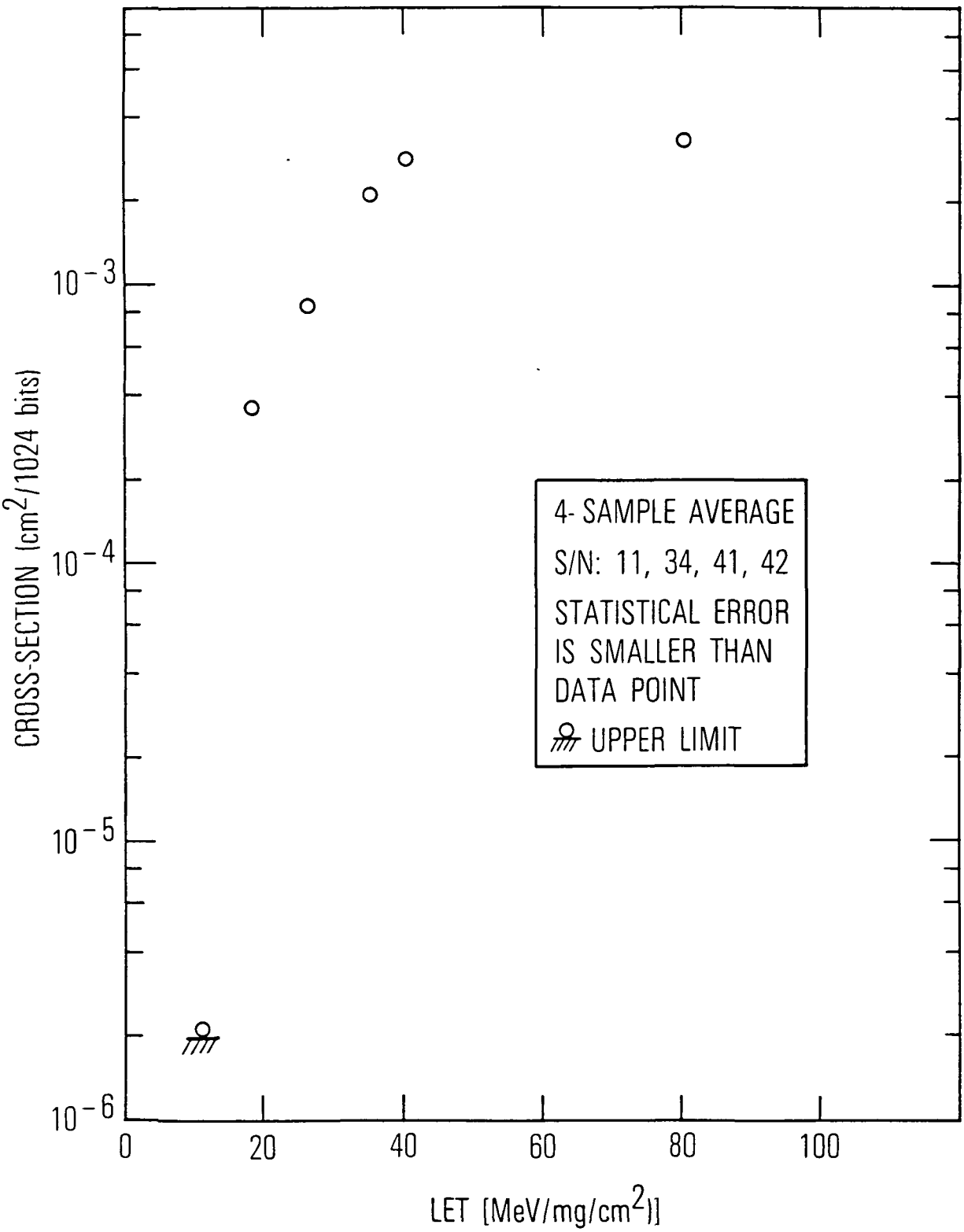

Fig. 15. NSC810 results: SEU, RAM section.

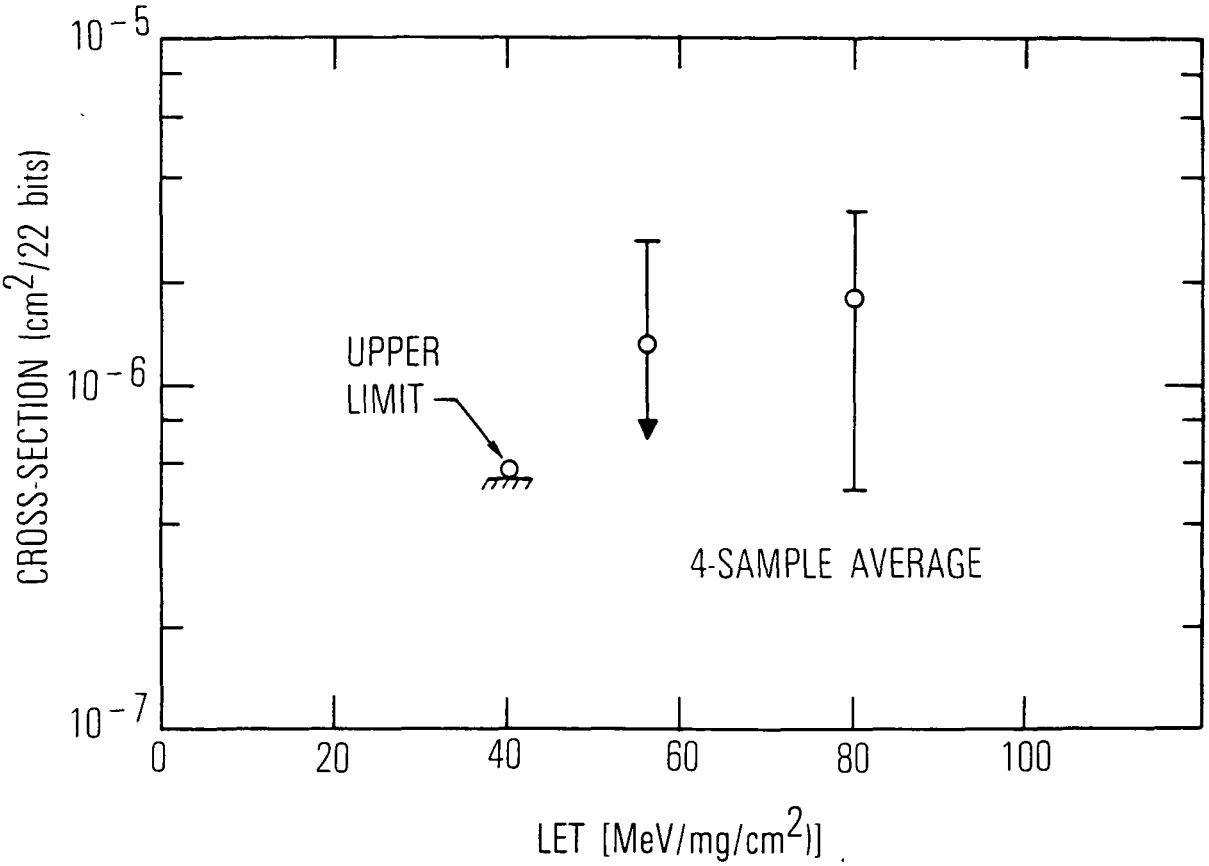

Fig. 16. NSC810 results: SEU, port-output latches.

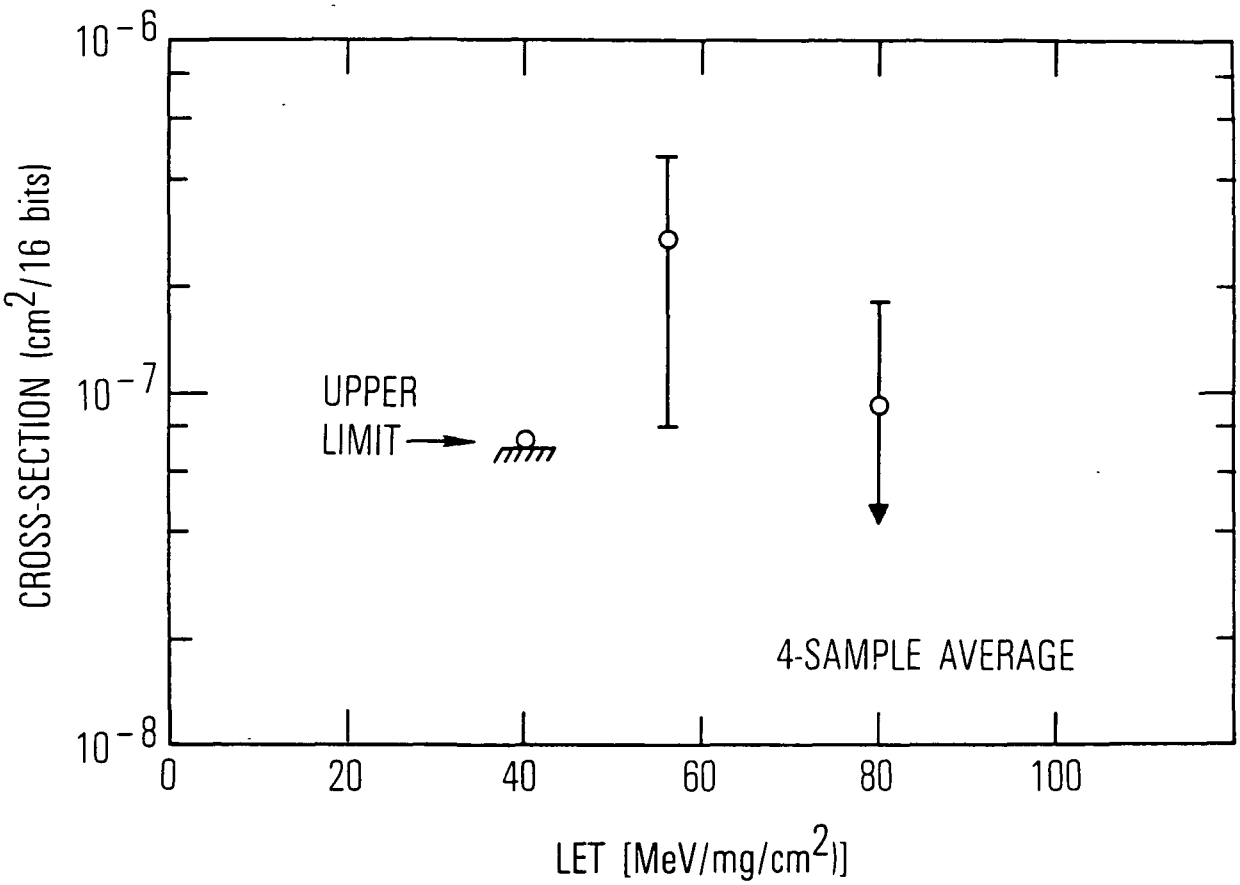

Fig. 17. NSC810 results: SEU, timer-mode latches.

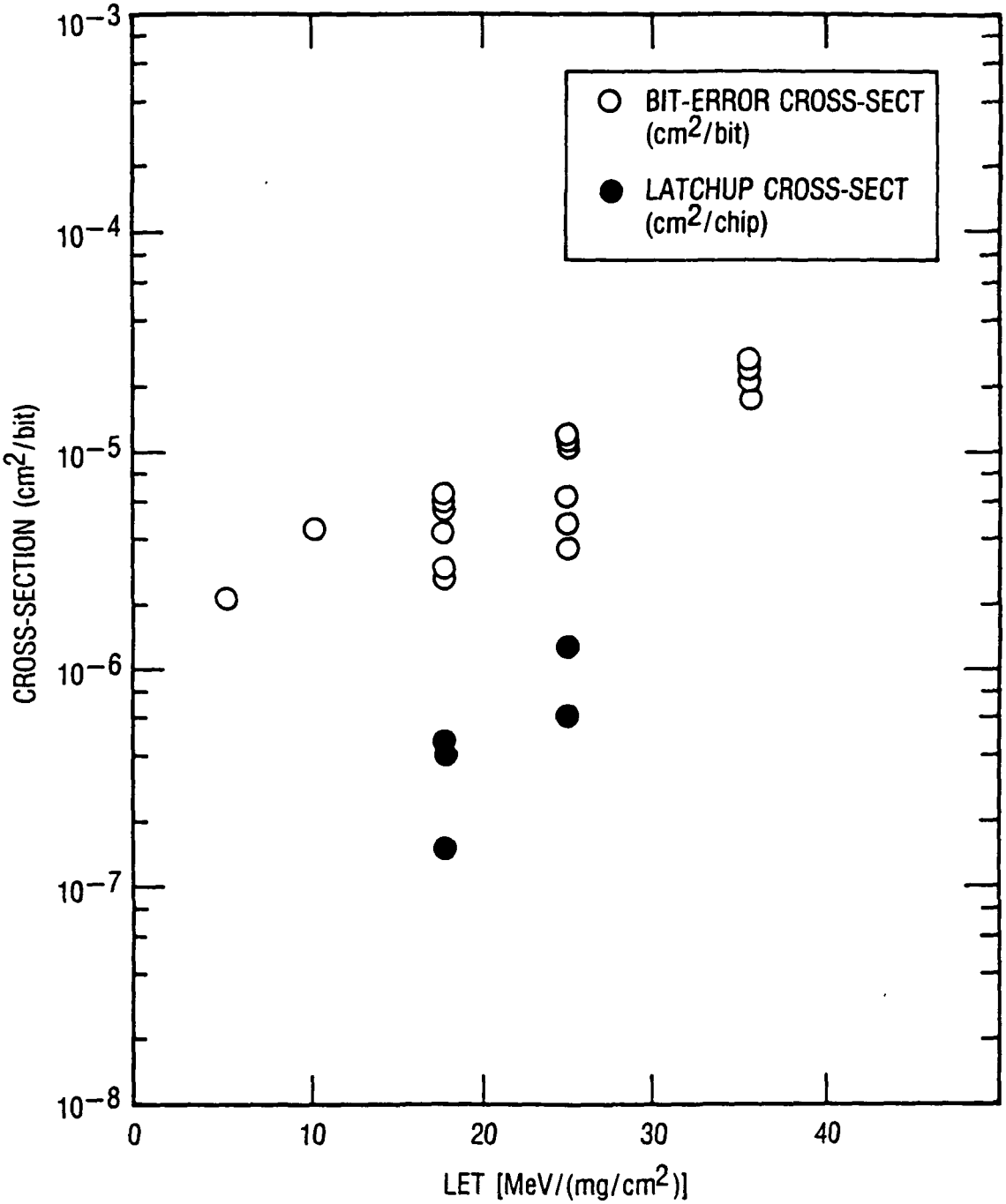

Fig. 18. NSC800 microprocessor results.

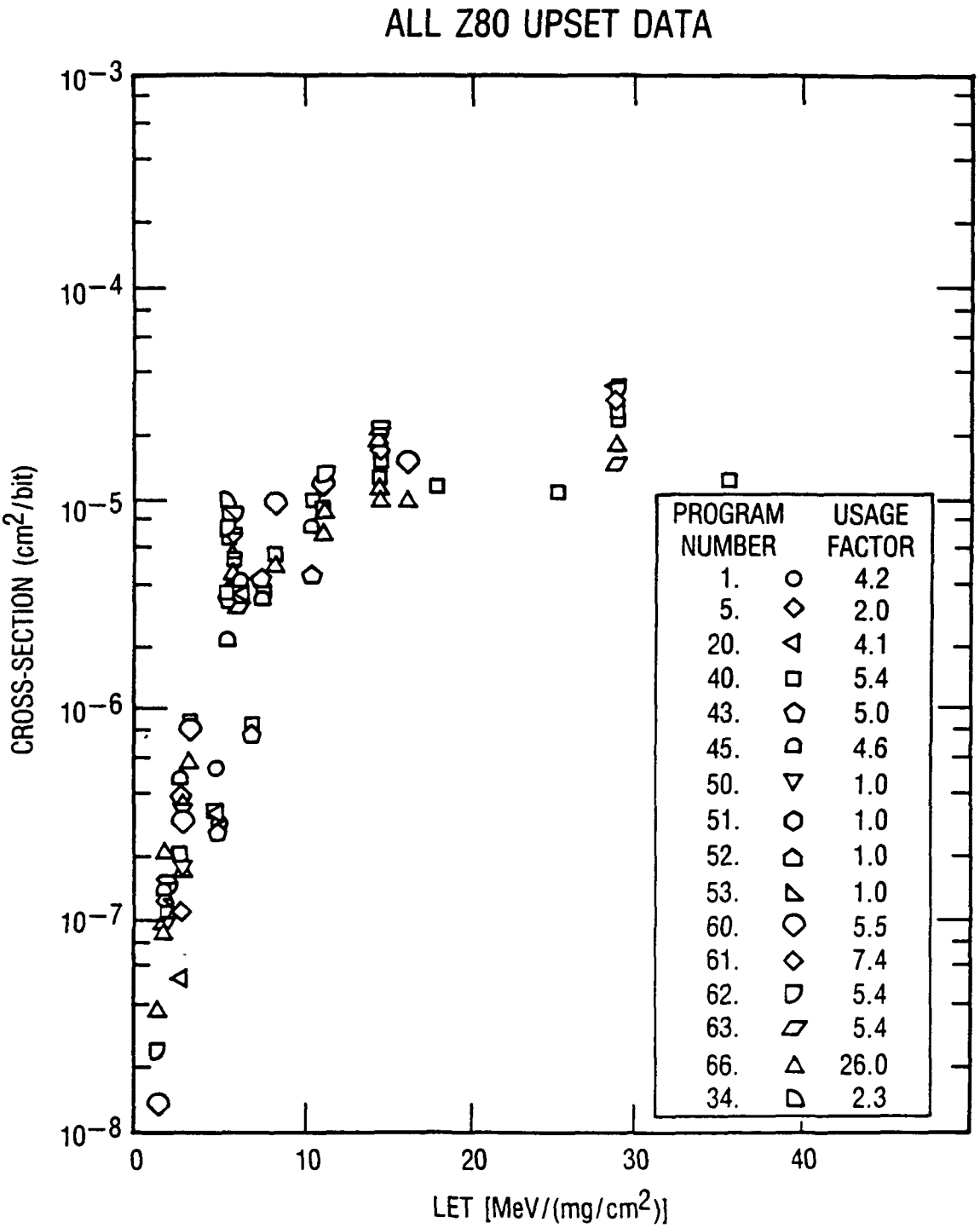

Fig. 19. Z-80 results.

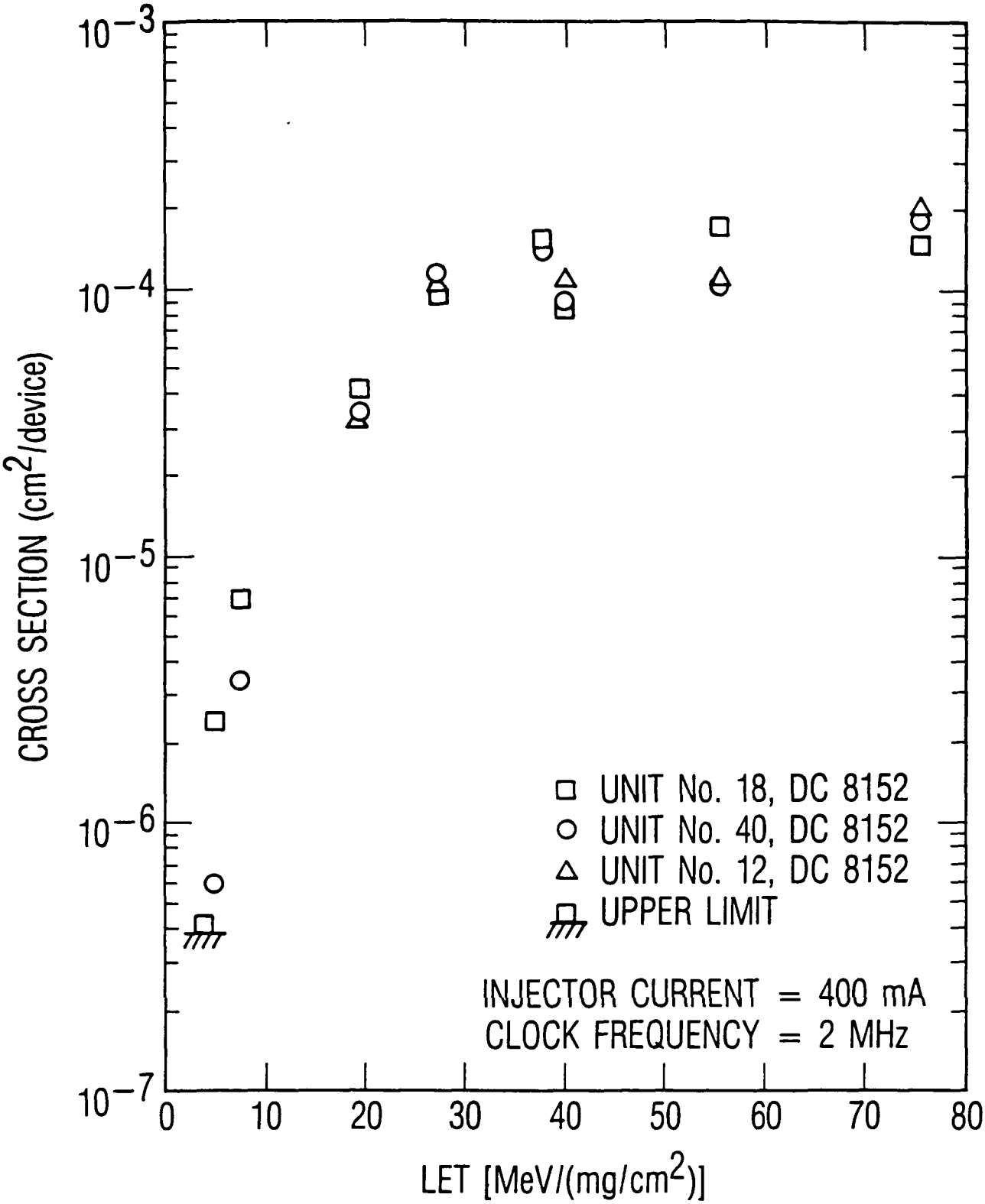

Fig. 20. SBP9989 microprocessor results.

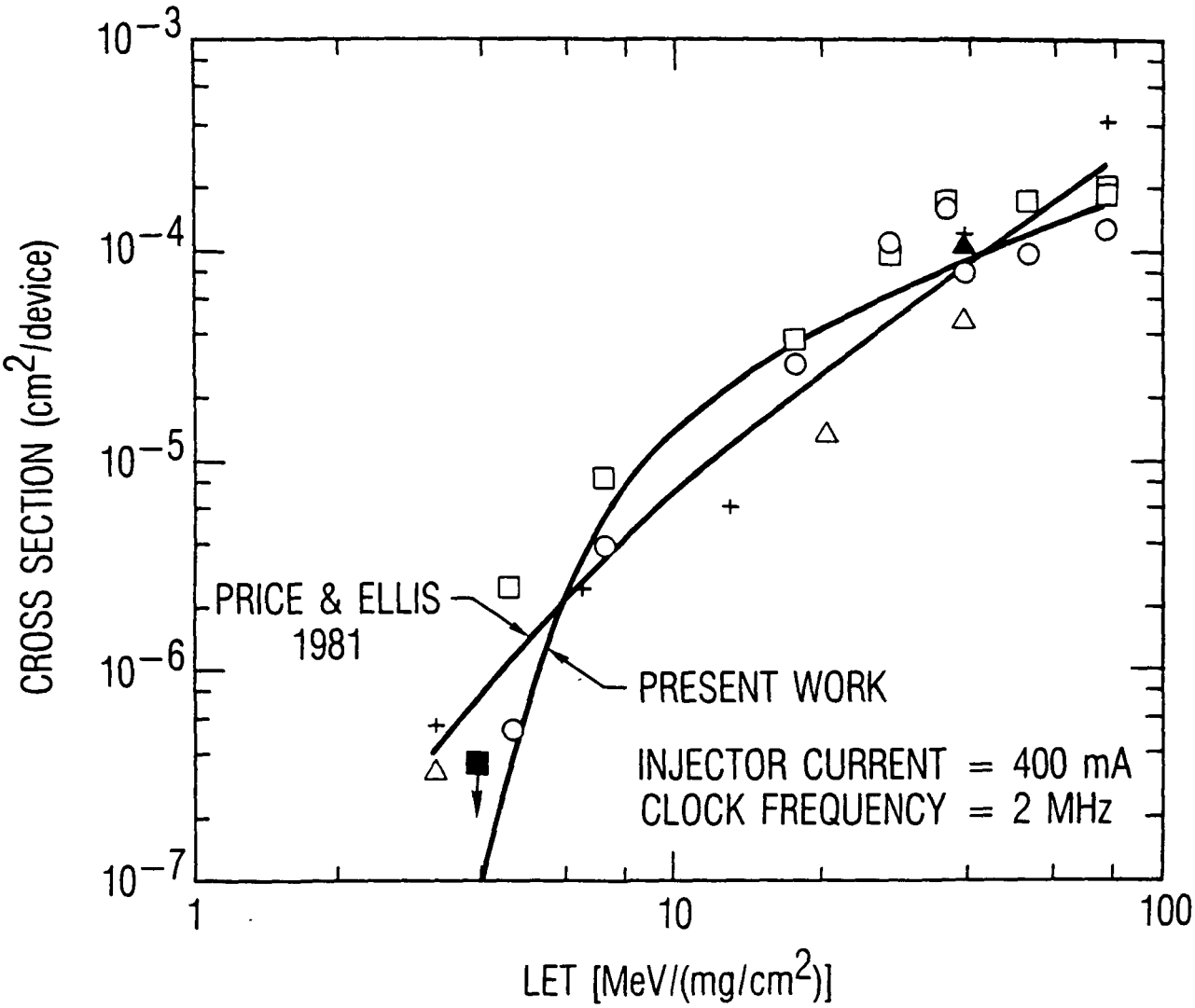

Fig. 21. Comparison of current SB9989 test results with previous test data.

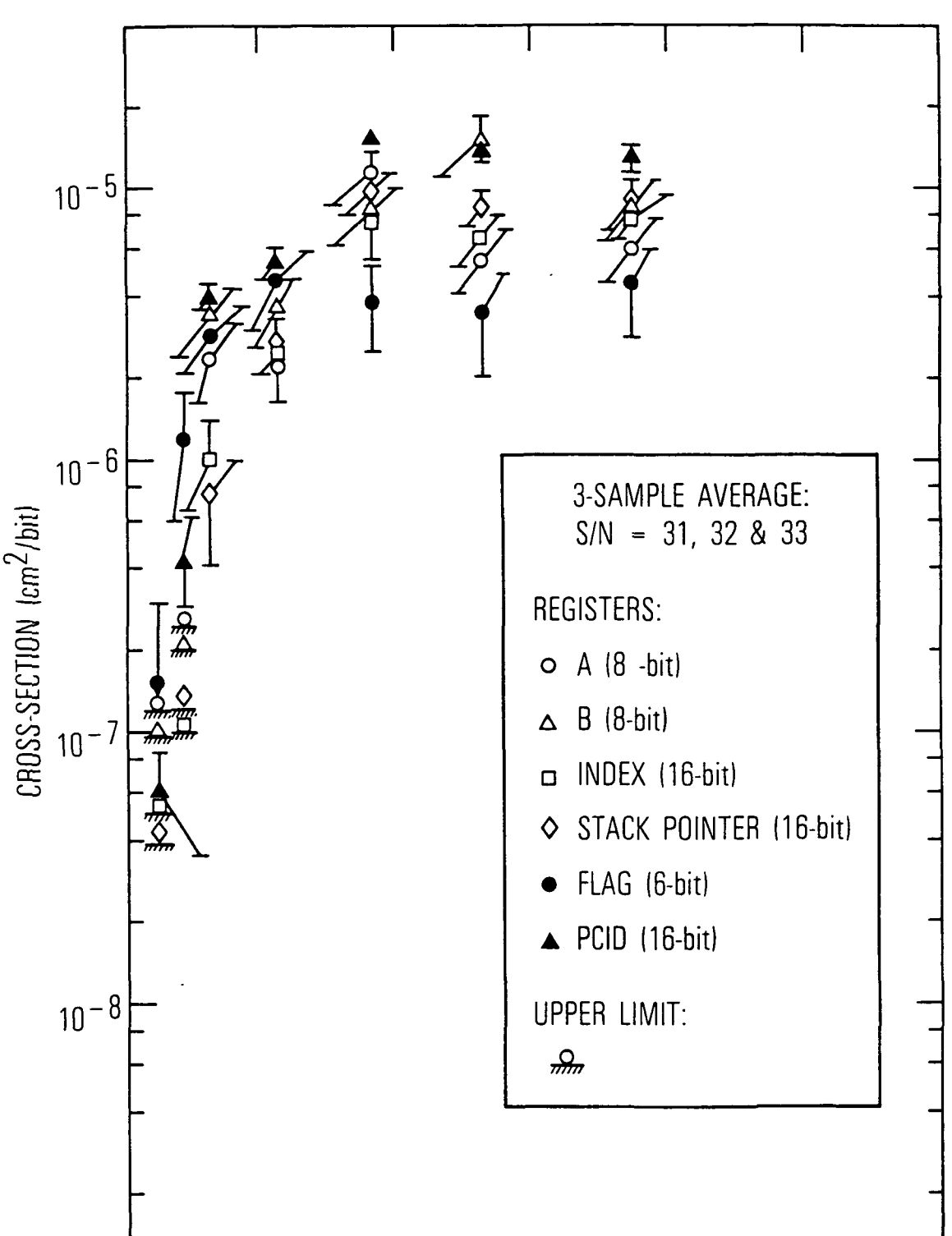

Fig. 22. 6800 results: semi-static register tests.

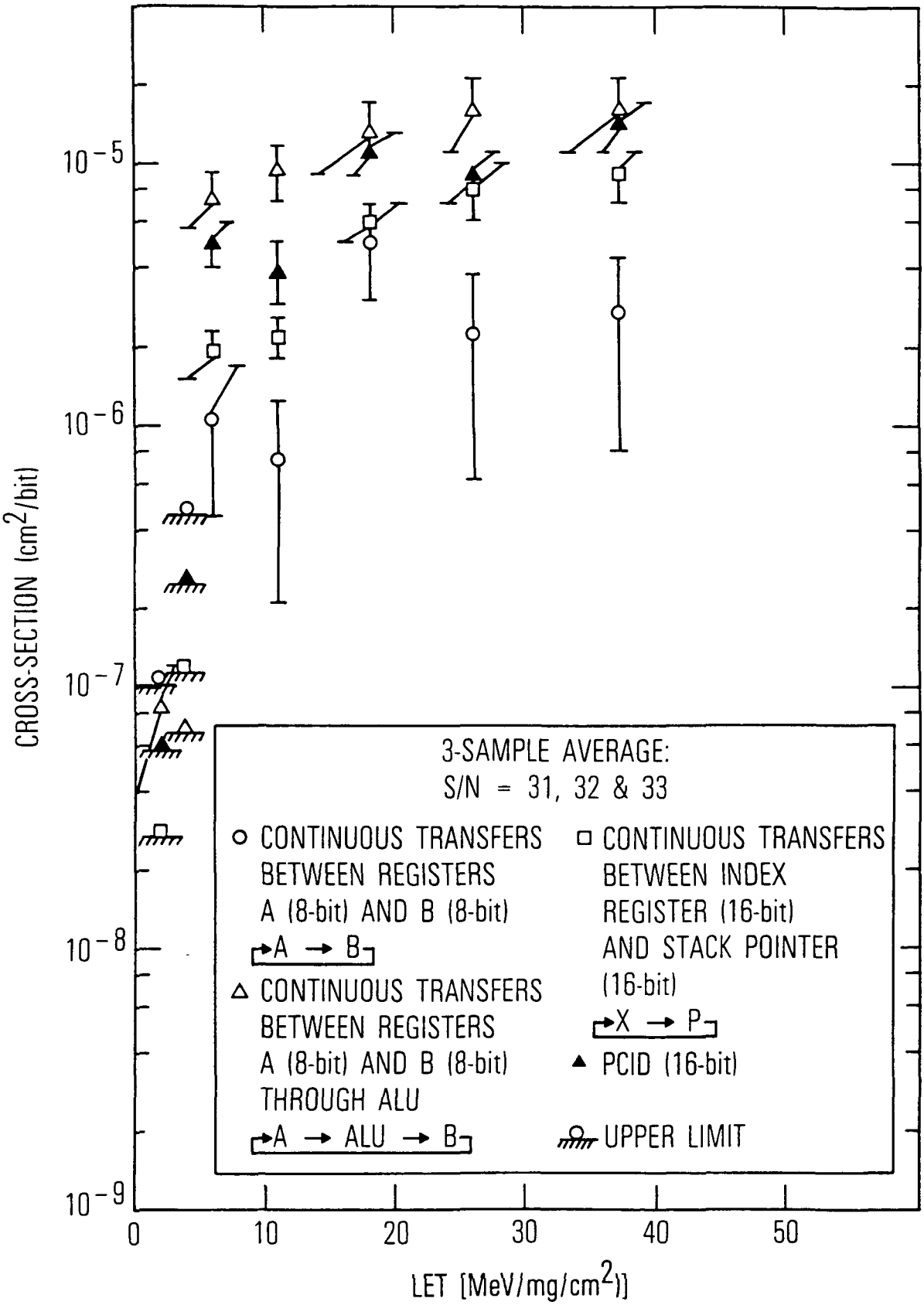

Fig. 23. 6800 results: semi-dynamic register tests.

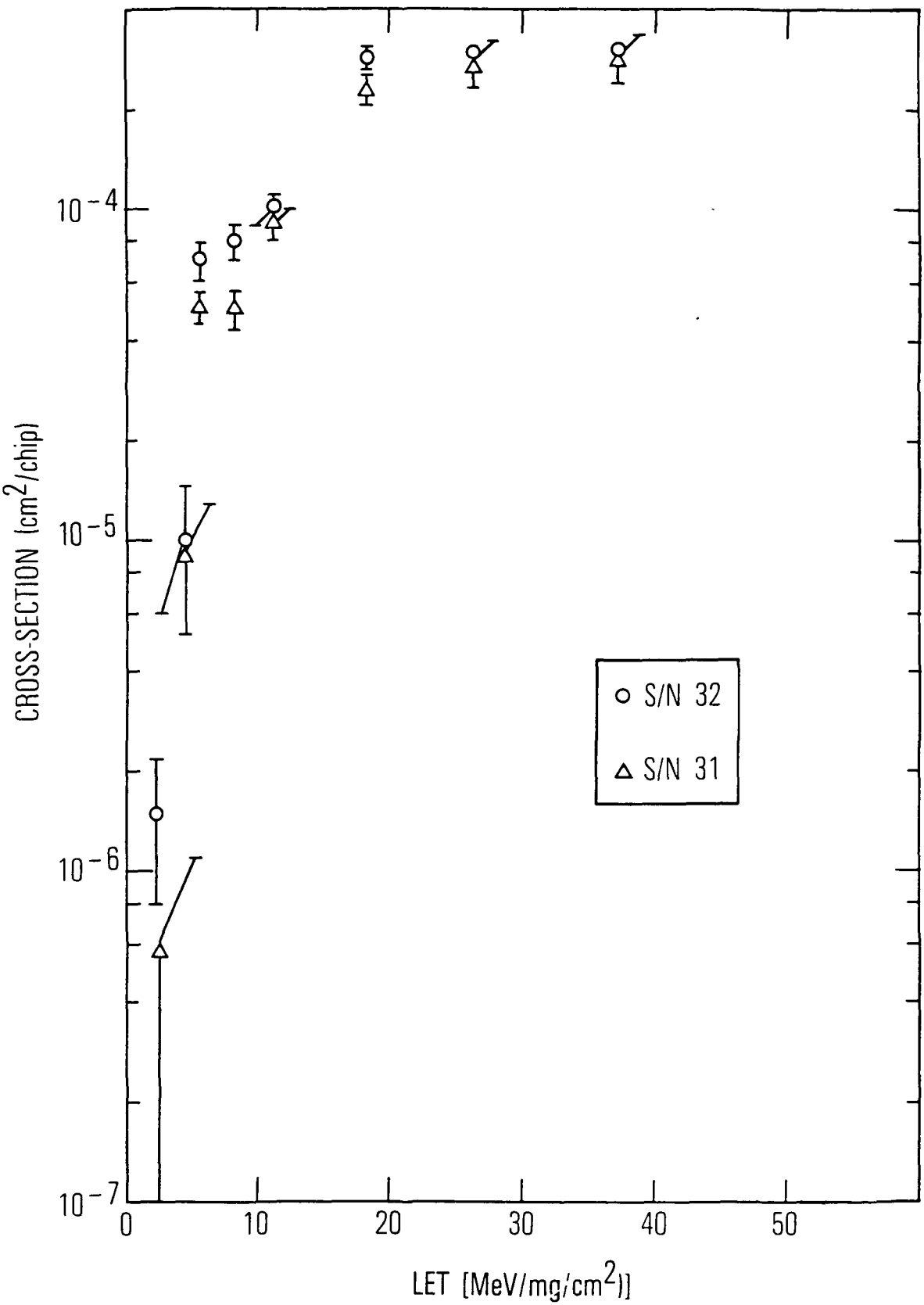

Fig. 24. 6800 results: NASA program results.

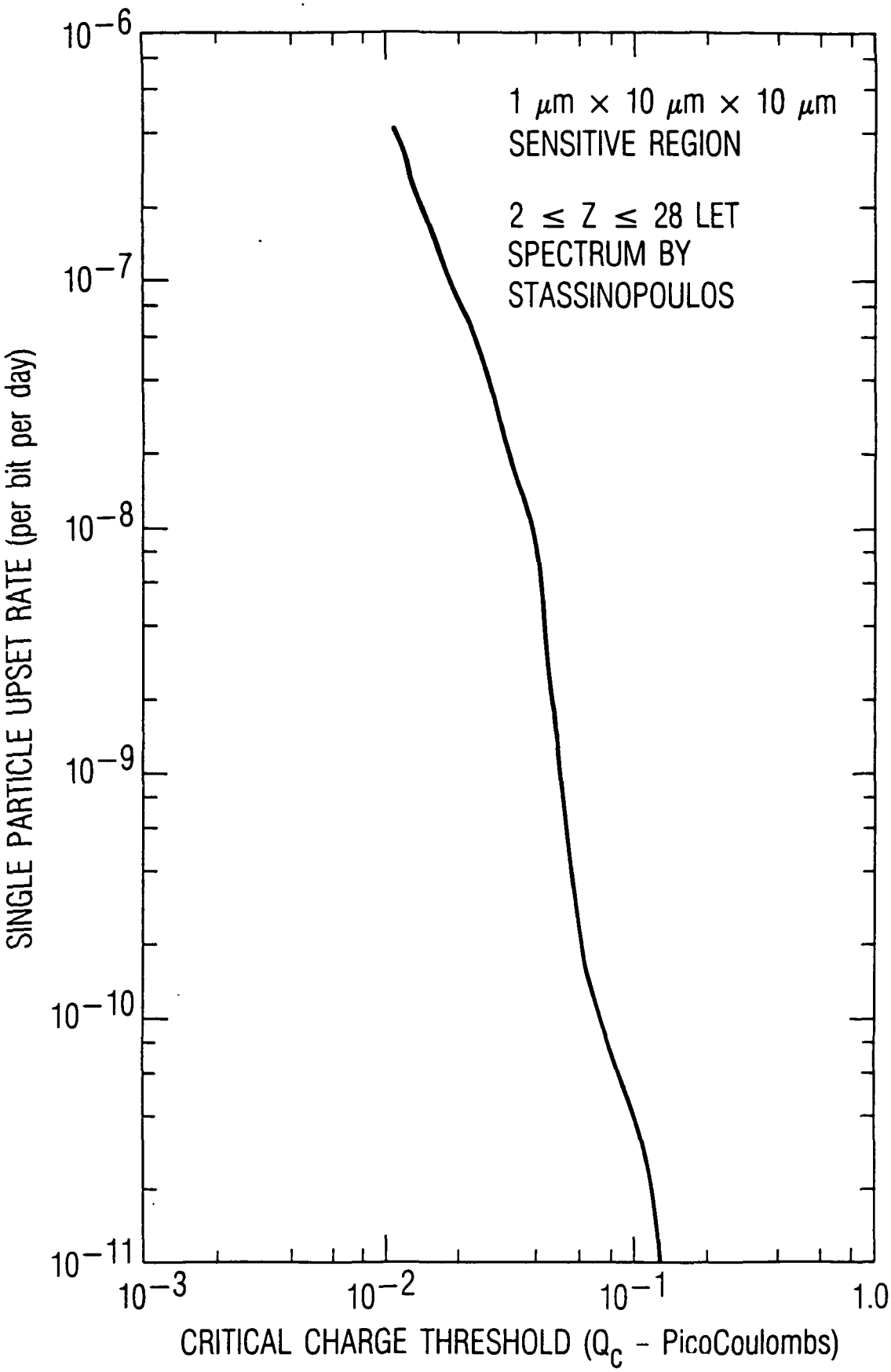

Fig. 25. Upset rate predictions as a function of critical charge for "standard" 10 μm x 10 μm x 1 μm transistor cell.