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Development of Substrate Structure CdTe Photovoltaic Devices with Performance Exceeding 10%

Ramesh G. Dhere, Joel N. Duenow, Clay M. DeHart, Jian V. Li, Darius Kuciauskas, and Timothy A. Gessert

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***Abstract* — Most work on CdTe-based solar cells has focused on devices with a superstrate structure. This focus is due to the early success of the superstrate structure in producing high-efficiency cells, problems of suitable ohmic contacts for lightly doped CdTe, and the simplicity of the structure for manufacturing. The development of the $CdCl_2$ heat treatment boosted CdTe technology and perpetuated the use of the superstrate structure. However, despite the beneficial attributes of the superstrate structure, devices with a substrate structure are attractive both commercially and scientifically. The substrate structure eliminates the need for transparent superstrates and thus allows the use of flexible metal and possibly plastic substrates. From a scientific perspective, it allows better control in forming the junction and direct access to the junction for detailed analysis. Research on such devices has been limited. The efficiency of these devices has been limited to around 8% due to low open-circuit voltage (V_{oc}) and fill factor. In this paper, we present our recent device development efforts at NREL on substrate-structure CdTe devices. We have found that processing parameters required to fabricate high-efficiency substrate CdTe PV devices differ from those necessary for traditional superstrate CdTe devices. We have worked on a variety of contact materials including Cu-doped ZnTe and Cu_xTe. We will present a comparative analysis of the performance of these contacts. In addition, we have studied the influence of fabrication parameters on junction properties. We will present an overview of our development work, which has led to CdTe devices with V_{oc} values of more than 860 mV and NREL-confirmed efficiencies approaching 11%.**

***Index Terms* — CdTe, substrate structure, devices, contacts, open-circuit voltage, efficiency.**

I. Introduction

Most work on CdTe-based solar cells has focused on devices with a superstrate structure. This focus is due to the early success of the superstrate structure in producing high-efficiency cells, problems of suitable ohmic contacts for lightly doped CdTe, and the simplicity of the structure for manufacturing. The development of the $CdCl_2$ heat treatment boosted CdTe technology and perpetuated the use of the superstrate structure. The substrate structure eliminates the need for transparent superstrates and thus allows the use of flexible metal and possibly plastic substrates. From a scientific perspective, it allows better control in forming the junction and direct access to the junction for detailed analysis. Research on such devices has been limited. The efficiency of these devices has been limited to around 8% due to low open-circuit voltage (V_{oc}) and fill factor (FF). Recently, however, CdTe photovoltaic (PV) devices fabricated in the nonstandard substrate configuration have attracted increasing interest. In addition to the manufacturing and deployment benefits, optical losses can be reduced further in substrate CdTe devices than in traditional superstrate devices because the light is incident on the film side of the stack, potentially leading to higher short-circuit current. Presently, however, the efficiencies of substrate CdTe devices reported in the literature are significantly lower (~6%–8%) [1-3] than those of high-performance superstrate devices (~17%) [4] due to significantly lower V_{oc} and FF. In this paper, we report on our recent development effort on substrate-structure CdTe devices. We have looked at a variety of back-contact layers, in addition to the variation in CdS fabrication parameters. We found the effect of heat treatments in different ambients on the device properties to be significant. The development effort has led to devices with V_{oc} values of more than 860 mV and NREL-verified efficiencies approaching 11%.

II. Experimental Details

Substrate CdTe devices used in this study were fabricated in the following manner (Fig. **1**). Substrates were prepared by depositing a thin layer (≤10 nm) of Cr and 800 nm of Mo by direct-current sputtering onto cleaned 0.8-mm-thick Corning 7059 glass. Next, interfacial layers of Cu-doped ZnTe, Sb_2Te_3, MoO_3, or Cu_xTe were deposited by radio-frequency (RF) magnetron sputtering. CdTe films were deposited by close-spaced sublimation (CSS) from a CdTe source plate [5] to a thickness of ~4–5 μm at a substrate temperature of 450°–600°C. The oxygen-free ambient used in this study for the CdTe deposition was 16 torr of He, and the oxygen-containing ambient consisted of 1 torr of O_2 plus 15 torr of He. Following the CdTe deposition, a $CdCl_2$ vapor heat treatment was performed at 400°C by CSS. The oxygen-free ambient used was 400 torr of He, and the oxygen-containing ambient was 80 torr of O_2 plus 320 torr of He. The CdS layer was deposited by chemical-bath deposition (CBD) [5] or by RF sputtering with thicknesses in the range of 80–125 nm in an ambient containing Ar and O_2 [6].

The front contact consisted of a bilayer of 100 nm of intrinsic ZnO and 120 nm of Al-doped ZnO (from a target containing 2 wt.% Al_2O_3 in ZnO) deposited by RF magnetron sputtering. A grid consisting of 50-nm Ni and 3-μm Al completed the devices.

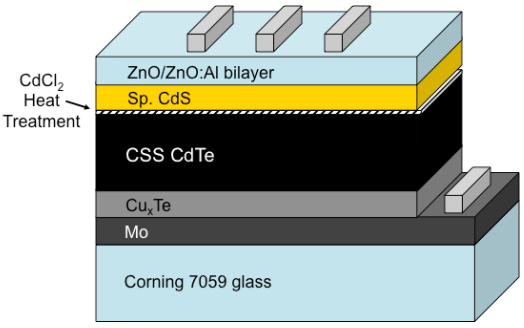

Fig. 1. Structure of the substrate CdTe devices used in this study.

Preliminary device characterization was done using current density-voltage (J-V) and quantum efficiency measurements.

Results and Discussion

Our initial work on substrate-configuration CdTe PV devices used the fabrication processes used for fabricating high-efficiency superstrate CdTe devices [5] and structural components from substrate-structure Cu(In,Ga)Se_2 (CIGS) devices. We used Mo-coated glass substrates and deposited CdTe in a He/O_2 ambient. A CdS layer 80 nm thick was deposited by CBD and the devices were finished as shown in Fig. 1. These devices were typically in the efficiency range of 5% to 6%. J-V characteristics of one of these devices are presented in Fig. 2. These devices were affected by low V_{oc} values (between 500 and 600 mV), FFs below 50%, and efficiencies below 6%.

During our initial phase of device development, we used CBD CdS layers to fabricate the devices. The resulting devices were affected by varying degrees of adhesion problems at the Mo/CdTe interface. With the use of sputtered CdS, we were able to improve the consistency of our results. Further development implemented sputtered CdS layers.

The device characteristics of Mo-contact devices were affected significantly by rollover in the first quadrant of the J-V measurements, indicating a non-ohmic contact. Hence, we decided to investigate a variety of interfacial layers (IFLs) between the Mo and CdTe layer as a contact material. Initial work concentrated on Cu-doped ZnTe as the contact layer. For the first set of devices, we used identical processing conditions mentioned above for the Mo devices without IFLs. The device performance for these devices with Cu-doped ZnTe deteriorated significantly (not shown). We attributed the performance degradation to possible oxidation of the Cu-doped ZnTe IFL during the CSS CdTe deposition in an ambient containing oxygen. Therefore, we eliminated oxygen from the CSS CdTe deposition ambient. During the development of O_2-free processing for the CdTe deposition, we experimented with various processing parameters. The device results for two types of sources used for the deposition of the CdTe layer are presented in Figs. 3 and 4. For the device in Fig. 3, we used a CdTe source that was previously used for CdTe depositions in an ambient containing O_2 partial pressure, whereas the CdTe source used for the device in Fig. 4 was never exposed to an oxygen-containing ambient at elevated temperature. The sensitivity of the ZnTe layer to trace levels of oxygen is evident from the poorer performance of the device shown in Fig. 3, with only a trace amount of oxygen introduced from an oxidized CdTe source. Results for a device fabricated using a 25-nm-thin layer of ZnTe doped with 0.3 wt.% Cu, CdTe deposited at 600°C in a He ambient, and a $CdCl_2$ heat treatment (HT) at 400°C in an O_2/He ambient are presented in Fig. 4. With these devices, we saw significant improvement in the V_{oc} to over 750 mV; however, these devices were affected by voltage-dependent collection and low FFs, reducing the efficiency significantly.

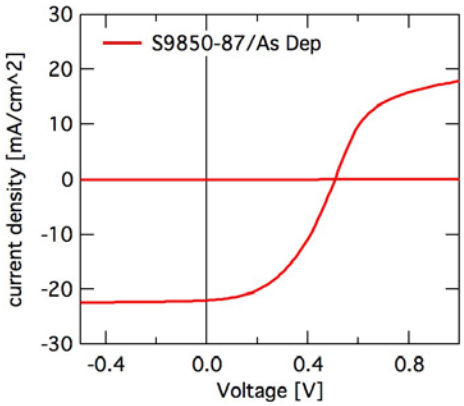

Fig. 2. J-V characteristics of baseline device without IFL. V_{oc} = 507 mV, J_{sc} = 21.9 mA/cm^2, FF = 45.8%, efficiency = 5.10%.

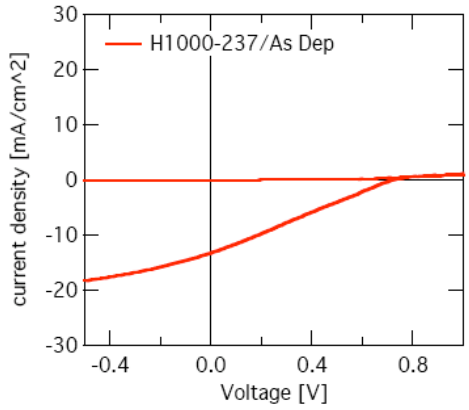

Fig. 3. J-V characteristics of a baseline device with a Cu-doped ZnTe IFL and a CdTe film deposited from an oxidized CdTe source. V_{oc} = 735 mV, J_{sc} = 13.3 mA/cm^2, FF = 24.5%, efficiency = 2.39%.

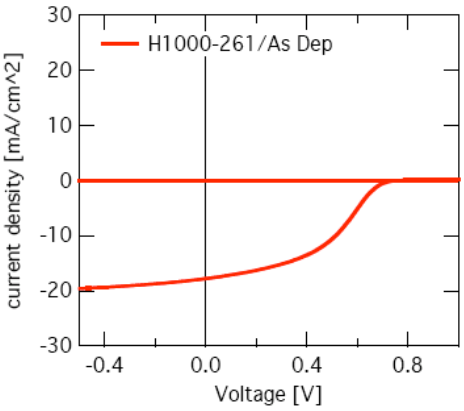

Fig. 4. J-V characteristics of a baseline device with a Cu-doped ZnTe IFL and a CdTe film deposited from an oxygen-free source. V_{oc} = 776 mV, J_{sc} = 17.8 mA/cm^2, FF = 40.2%, efficiency = 5.54%.

We have investigated the effects of HTs before and after the deposition of the CdS layer on device properties. We found that a HT of the CdTe absorber layer in a $CdCl_2$ ambient improved device performance. However, a $CdCl_2$ HT after the deposition of the CdS layer was excessive and resulted in deterioration of device performance. We investigated the use of a HT on the structures after the CdS deposition at considerably lower temperatures (175°–300°C) and without $CdCl_2$ in the ambient. The post-CdS HT had opposite effects for devices with and without a Cu-containing IFL. Results for the device with only a Mo contact (without IFL) are presented in Fig. 5. The device performance deteriorates progressively with the post-contact HT temperature. J-V characteristics for a device fabricated with 100-nm-thick ZnTe doped with 4 wt.% Cu, CdTe deposited at 450°C, and a post-contact HT at different temperatures are presented in Fig. 6. In this case, the device performance improved with an increase in treatment temperature to a maximum efficiency of 7.4% after the 225°C HT [8]. We have performed the HT of structures after the CdS deposition or after the ZnO front contact deposition and found the results to be similar. Results were also similar for the HT in either He or O_2/He ambient. The effect of the heat treatment showed the same trend for devices containing a Cu_xTe IFL. The effects of the HT on one of these devices are indicated in Fig. 7. The best efficiency of 8.45% for this device was obtained after a HT at 250°C. The highest V_{oc} for this device, 862 mV, was observed after the HT at 225°C. The opposite trend for the devices with and without a Cu-containing IFL indicates that the defect structure of these two types of devices is influenced by the presence of Cu.

In addition to Cu-containing IFLs, we also experimented with Sb_2Te_3 and MoO_3 as contact layers. Our results with Sb_2Te_3 and MoO_3 are not promising so far.

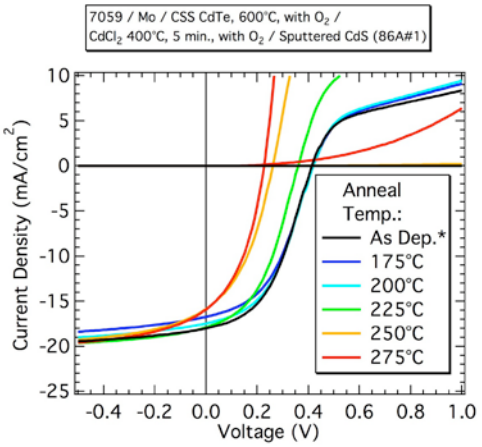

Fig. 5. J-V characteristics of device without IFL heat-treated at various temperatures, measured after each HT.

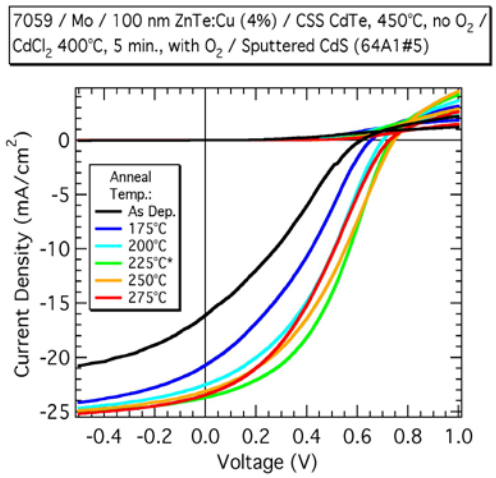

Fig. 6. J-V characteristics of a device with a Cu-doped ZnTe IFL. The best device result was obtained after the 225°C HT. After the 225°C HT, V_{oc} = 742 mV, J_{sc} = 23.6 mA/cm^2, FF = 42.2%, and efficiency = 7.4%.

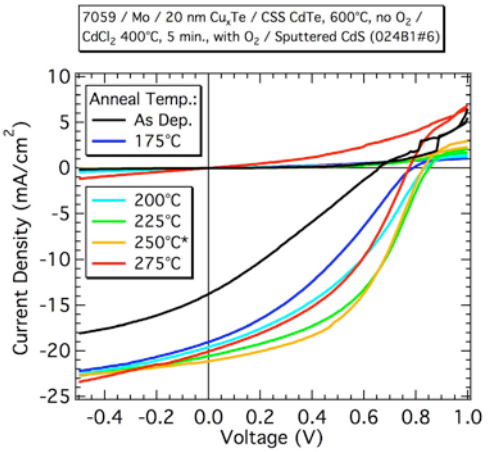

Fig. 7. J-V characteristics of device with a Cu_xTe IFL. The best device result was obtained after the 250°C HT. After the 250°C HT, V_{oc} = 841 mV, J_{sc} = 20.55 mA/cm^2, FF = 45.54%, and efficiency = 8.45%.

By refining our processing with Cu-containing IFLs, we have obtained devices with V_{oc} values of more than 860 mV and FFs up to 64%. Figure 8 presents the J-V characteristics of an NREL-verified device (without antireflection coating) with an efficiency of 10.97% for a device with a 10-nm-thick Cu_xTe IFL. In addition to the effect of the medium-temperature anneal, the presence of oxygen during different stages of processing had a profound effect on device performance [7].

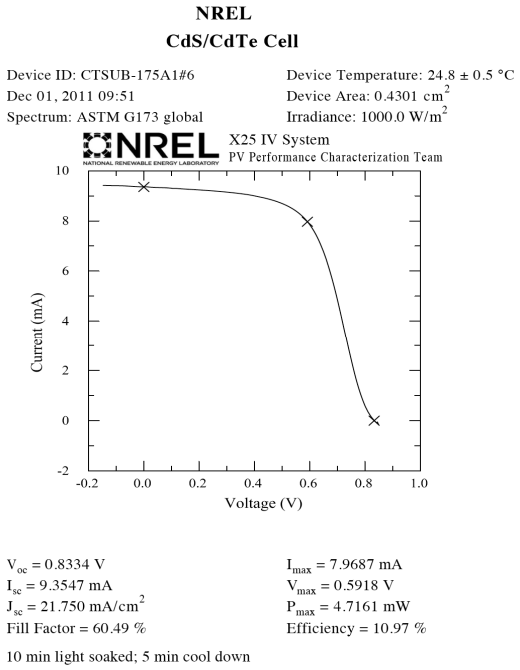

Fig. 8. J-V characteristics of NREL-verified device with Cu_xTe IFL.

III. CONCLUSIONS

We have carried out substrate CdTe device development over the past two years and found that the fabrication process used for conventional superstrate CdTe devices does not readily translate to substrate devices. The contact layer, use of oxygen during different fabrication steps, and heat treatments affect the device performance significantly. By refining our processing with Cu-containing IFLs, we have obtained devices with Voc values of more than 860 mV and FFs up to 64%. We have achieved an NREL-verified device (without antireflection coating) with an efficiency of 10.97%, which we believe is the highest verified efficiency for a substrate configuration CdTe device.

We will carry out more thorough characterization of these devices using techniques such as capacitance-voltage (C-V) and temperature-dependent current density-voltage measurements to gain further understanding of the function of these devices. We will use low-temperature photoluminescence techniques to study the effect of various fabrication parameters on the electronic defects in these devices. Results will be published in a future publication.

ACKNOWLEDGEMENTS

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