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An Advanced Platform for Development and Evaluation of Grid Interconnection Systems Using Hardware-in-the-Loop: Part III—Grid Interconnection System Evaluator

B. Lundstrom, M. Shirazi, M. Coddington, and B. Kroposki
National Renewable Energy Laboratory

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National Renewable Energy Laboratory
15013 Denver West Parkway
Golden, Colorado 80401
303-275-3000 • www.nrel.gov

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Acronyms

CAN	Controller Area Network
CHIL	Controller Hardware-in-the-Loop
CPU	Central Processing Unit
DR	Distributed Resource
EPS	Electric Power System
FRT	Frequency Ride-through
GISE	Grid Interconnection System Evaluator
GUI	Graphical User Interface
HIL	Hardware-in-the-Loop
ICS	Interconnection System
OF	Overfrequency
OV	Overvoltage
PCC	Point of Common Coupling
PHIL	Power Hardware-in-the-Loop
PV	Photovoltaic
RMS	Root Mean Square
RTS	Real-Time Simulator
UF	Underfrequency
UI	Unintentional Islanding
UV	Undervoltage
VRT	Voltage Ride-through

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Executive Summary

The world's energy paradigm continues to undergo a rapid shift, fueled by legislative mandates and quotas, towards an increased use of renewable energy sources. To support this shift, an advanced electric power system (EPS) architecture, including increasing amounts of distributed resources, load control, bi-directional power flow, advanced metering, and improved communications is gaining attention and being implemented by many electric utilities. As new distributed energy resources are interconnected with the EPS, it is essential to verify not only that their grid interconnection systems (ICS) conform to the relevant U.S. grid interconnection standards (IEEE Std 1547™ and UL 1741), but also that they perform satisfactorily under a variety of variable resource input and grid output conditions.

To this end, the National Renewable Energy Laboratory (NREL) has been developing a platform for evaluation of ICSs using hardware-in-the-loop (HIL). This report describes an important addition to that platform—a grid interconnection system evaluator (GISE). The GISE is a combined hardware and software solution that leverages HIL simulation techniques to automate portions of the often time-consuming grid interconnection conformance test procedures of IEEE Std 1547.1™. Beyond just automating grid interconnection conformance test procedures for standard equipment, the GISE provides a platform to test the capability of an ICS with respect to advanced grid functions such as voltage and/or frequency ride-through, volt/var control, or other ancillary services.

Testing an ICS using the GISE is completed through a graphical user interface (GUI) from which a user can configure, run, monitor, and view results of a set of grid interconnection conformance tests from a single window. Throughout a test, this GUI communicates with a real-time simulator (RTS) that executes a software control model of each conformance test in the loop with the ICS under test and the related electrical test equipment. High-speed data is acquired by the RTS throughout the test and then analyzed and plotted after a test is completed to provide the user with a single-page summary test report. This test report provides not only an at-a-glance summary for determination of whether the ICS passed the particular test, but also detailed waveform information of key parameters for a complete picture of the ICS's response.

This report provides a comprehensive set of test results demonstrating the GISE's accuracy, repeatability, and versatility in executing IEEE Std 1547 over/undervoltage and frequency and unintentional islanding tests. This testing regime employed three different commercial residential photovoltaic inverters to also show the applicability of the GISE to a variety of ICS topologies.

The GISE adds further capability to NREL's advanced platform for development and evaluation of grid interconnection systems. This platform now allows for rapid development of ICS control algorithms using controller hardware-in-the-loop (CHIL) techniques, the ability to test the dc input characteristics of photovoltaic (PV)-based ICS through the use of a PV simulator capable of simulating real-world dynamics using power hardware-in-the-loop (PHIL), and evaluation of the grid interconnection conformance of an ICS. This platform offers a unique set of capabilities that will help develop and evaluate the next generation of ICSs that will be prevalent in future advanced EPS architectures.

1 Introduction

1.1 Background

The world's energy paradigm continues to undergo a rapid shift towards an increased use of renewable energy sources. Worldwide, 71 countries have renewable portfolio standards or other quotas mandating that their electric utilities produce a portion of their total energy from renewable sources [1]. The effect of these quotas is evident; investments in new renewable capacity and renewable power capacity worldwide have increased over 150% from 2009 to 2011 alone [1]. The U.S. Department of Energy's Energy Information Administration predicts that this trend of growing renewable power capacity will continue at least through 2035 [2]. At the same time, an EPS architecture including increasing amounts of distributed resources, load control, bi-directional power flow, advanced metering, and improved communications is gaining attention and being implemented by many electric utilities. This new EPS architecture further enables consumer participation and assists utilities in efficiently accommodating various distributed resources (DR) such as PV, wind, fuel cell, micro turbine, and energy storage technologies.

In support of this shifting energy paradigm and new EPS architecture, a swiftly-increasing number of renewable energy-based DR installations are occurring—the majority at the EPS distribution system level. As these installations occur, it is essential to ensure that these systems, each of which interface to the EPS using a grid ICS, are properly interconnected with the EPS according to the relevant U.S. standards, which are UL 1741 [3] and IEEE Std 1547 [4]. However, grid interconnection conformance is not the only essential aspect of determining the performance of an ICS; the device's performance under variable resource input and grid output conditions is also important.

To this end, NREL has been developing a platform for ICS evaluation using hardware-in-the-loop (HIL). The first portion of this platform has been introduced in a separate publication [5]. This report describes an addition to this platform—a grid interconnection system evaluator (GISE). The ground work for this concept was established in a previous NREL effort [6][7] and an initial version was described as a Grid Interconnection Evaluator [5]. This initial version was then renamed and improved upon to create the GISE, a fully-integrated tool with a unified user interface for grid interconnection evaluation tests.

1.2 IEEE Std 1547 and EPS Interconnection Conformance Testing

IEEE Std 1547, which was harmonized with UL 1741, was developed in order to provide a standard set of requirements for issues such as voltage regulation, synchronization and isolation, response to abnormal grid conditions, power quality, and islanding for interconnecting ICSs with the EPS. IEEE Std 1547.1 [8], *IEEE Standard Conformance Test Procedures for Equipment Interconnecting Distributed Resources with Electric Power Systems*, provides a comprehensive set of test procedures for use in determining if a particular ICS meets the requirements of IEEE Std 1547. When following the step-by-step procedures in IEEE 1547.1, it becomes clear that the process of testing an ICS against IEEE Std 1547 is quite comprehensive and can become very time-consuming. For example, when verifying that an ICS disconnects properly in grid over- or undervoltage conditions, the test must be repeated five times [8]. If the ICS is a multi-phase device, the test must be repeated five times for each phase and then five times for all phases simultaneously. Furthermore, if the device has adjustable limits, the test must be repeated five

more times at the maximum, minimum, and mid-point limit settings. Thus, there is significant potential to greatly reduce the amount of time required for running these conformance tests by automating portions of the test procedures using HIL simulation techniques.

1.3 HIL and Automated EPS Interconnection Conformance Testing

HIL simulation is a technique by which hardware systems and software models can be placed together into a single closed-loop simulation. This is accomplished by using an RTS that runs the software model and communication interface between software and hardware deterministically and in actual time (see Figure 1). In doing so, outputs from the hardware system (e.g., output current in the case of an ICS) can be measured and converted to a digital value. These digital values are used as inputs to a software model and outputs calculated, and these digital outputs are converted to analog outputs (e.g., inverter gate drive signals, breaker control, grid simulator control signal, etc. depending on the application) that are sent to the hardware system, all in one time step. The period of this simulation time step is adjustable, but must be long enough that the computation required for the process detailed above can complete and short enough that the software model can respond faster than any output dynamics of the hardware system, and so that the software model accurately reflects the dynamics of the physical system it is simulating.

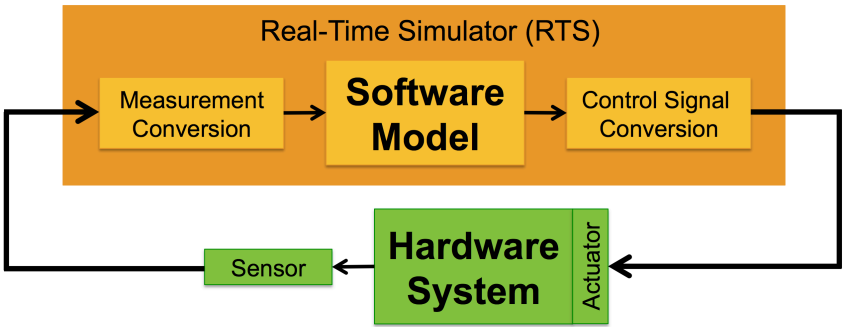

Figure 1: Typical HIL Simulation Setup

HIL simulation allows for rapid development of any portion of a closed-loop control system, whether it is based in hardware, software, or both. For example, earlier work on the NREL ICS development and evaluation platform [5] included both a CHIL-based methodology, by which ICS controllers can be tested against simulated inverter hardware prior to at power testing, and a power HIL (PHIL)-based PV simulator that can be used to test a PV ICS's response to the truly dynamic output of a PV array. Many other projects have leveraged CHIL and PHIL techniques for use with motor drives [9], generator excitation systems [10], and renewable energy applications [11] [12]. The use of HIL for grid conformance testing is mentioned in [13] and [14], however both of these works simply mention concepts and methodologies for testing different grid conformance aspects and lack implementation and results. In the case of the GISE described in this report, HIL simulation techniques are used to considerably shorten the amount of time required to complete a full set of grid interconnection conformance tests by placing a software control model of each conformance test in the loop with the ICS under test and the related electrical test equipment.

1.4 HIL and Advanced ICS Development and Evaluation

The existing standards for interconnection with the EPS in the United States, as detailed in IEEE Std 1547, were first collaborated on in 1999 and then published in 2003. Since that time, significant advancement of ICS grid support capabilities, especially power electronics-based ICS, has occurred. These new devices can be particularly valuable to the power system in providing advanced grid functions such as voltage ride-through (VRT) and/or frequency (FRT) ride-through, volt/var control, or other ancillary services. However, because of these new grid support capabilities, advanced ICS don't necessarily comply with the recommended limits indicated in IEEE Std 1547 and thus some electric utilities are hesitant to allow their installation. An amendment to IEEE Std 1547 (P1547a), which is tasked with addressing some of these discrepancies, is underway, but until that time it is particularly useful to perform PHIL-based tests that evaluate how a particular advanced ICS will operate in a particular local EPS. Such simulations are accomplished by using a software model of the local Area EPS, which is then coupled to a simulated EPS point of common coupling, where the actual ICS hardware is connected. This capability was demonstrated in a related DOE/NREL project [15] and provides an excellent addition to the platform described in this paper, allowing for evaluation of a range of ICS that may or may not have advanced grid support functions or conform to the recommended limits of IEEE Std 1547.

2 Interconnection Testing

2.1 IEEE Std 1547.1 and Interconnection Conformance Testing

2.1.1 Overview

IEEE Std 1547.1 "specifies the type, production, and commissioning tests that shall be performed to demonstrate that the interconnection functions and equipment of the distributed resources (DR) conform to IEEE Std 1547"[8]. To do so, it provides procedures for a set of tests that, when complete, verify that the ICS in question conforms to IEEE Std 1547. Of this large set of tests, the GISE focuses on the series of abnormal voltage, abnormal frequency, and unintentional islanding tests as these are the most complex and most repeated tests that would gain the most from some level of automation using HIL. To understand the approach that must be taken from an HIL software control model, these tests are briefly reviewed below.

2.1.2 Abnormal Voltage Tests

The purpose of these tests is to verify that the ICS ceases to energize the Area EPS when the voltage magnitude at the point of common coupling (PCC) between the ICS and the EPS deviates outside of a nominal range. The specific limits that constitute an overvoltage or undervoltage condition are specified in IEEE Std 1547. For both of these conditions, the exact voltage magnitude at which the ICS disconnects ("magnitude test") and the amount of time between when the abnormal voltage is first observed and when the ICS actually disconnects ("time test") must be measured and evaluated against the specifications in section 4.2.3 of IEEE Std 1547 [4].

The process of determining the voltage magnitude at which the ICS disconnects is described in section 5.2 of IEEE Std 1547.1 [8] and is shown in the generic parameter trip magnitude test function representation in Figure 2. The process begins by holding the voltage at the terminals of the ICS at nominal magnitude (P_n) and frequency until the ICS begins normal operation. Next,

the voltage magnitude is stepped to the starting voltage (P_b), which is within 10% of but not exceeding the trip point magnitude, and held at this point for T_h, at least two times the trip time setting. Finally, a slow ramp of the voltage magnitude at slope M_{ramp} occurs until the ICS disconnects, at which point the voltage magnitude is recorded. IEEE Std 1547.1 defines M_{ramp} based on the time-delay setting and stated accuracy of the ICS [8]. This procedure is then repeated for a total of five tests. If the ICS is a multiphase device or if the trip magnitude is adjustable, additional repetitions are necessary.

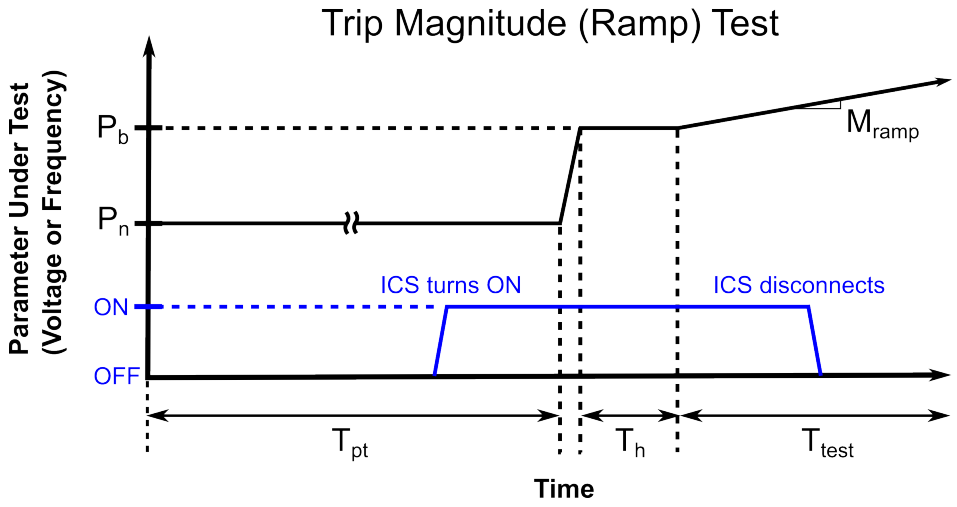

Figure 2: Representation of Trip Magnitude Test Function
(Based on Figure A.2 of IEEE Std 1547.1)

To identify the amount of time from when the ICS observes an abnormal voltage to when the ICS actually disconnects, the procedure in section 5.2 of IEEE Std 1547.1 [8] and the generic parameter trip time test function represented in Figure 3 is used. As with the trip magnitude test, the trip time test begins by holding the voltage at the terminals of the ICS at nominal magnitude and frequency until the ICS begins normal operation. Next, the voltage magnitude is stepped to the starting voltage (or starting parameter, P_b), which is within 10% of but not exceeding the trip point magnitude, and held at this point for T_h, at least two times the trip time setting. Finally, the voltage magnitude is again stepped, this time to P_t (a point well beyond the trip setting) and held until the ICS disconnects. The amount of time between when the step to P_t was finished and when the ICS disconnected is then recorded. This procedure is repeated for a total of five tests. If the ICS is a multiphase device or if the trip magnitude is adjustable, additional repetitions are necessary [8].

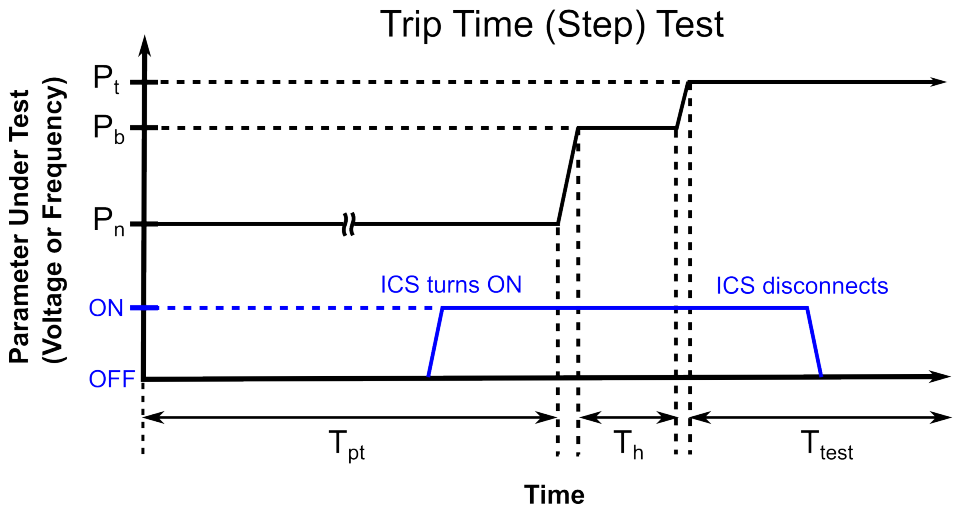

Figure 3: Graphical Representation of Trip Time Test Function (Based on Figure A.3 of IEEE Std 1547.1)

2.1.3 Abnormal Frequency Tests

The purpose of these tests is to verify that the ICS ceases to energize the Area EPS when the frequency of the voltage at the PCC between the ICS and the EPS deviates outside of a nominal range. The specific limits that constitute an overfrequency or underfrequency condition are specified in IEEE Std 1547. For both of these conditions, the exact frequency at which the ICS disconnects ("magnitude test") and the amount of time between when the abnormal frequency is first observed and when the ICS actually disconnects ("time test") must be measured and evaluated against the specifications in section 4.2.4 of IEEE Std 1547 [4].

The procedures for conducting abnormal frequency tests, which are given in section 5.3 of IEEE Std 1547.1 [8], are essentially identical to those described for the abnormal voltage tests, except that the parameter being modified is the frequency of the voltage rather than the magnitude of the voltage. Also, the starting frequency (P_b) is to be within 1% of the trip magnitude. Thus, for both the trip magnitude and trip time tests, the same procedures and generic parameter test functions (shown in Figure 2 and Figure 3) are followed except that the parameter under test is the frequency of the voltage.

2.1.4 Unintentional Islanding Tests

The purpose of this test is to verify that the ICS ceases to energize the Area EPS when an unintentional island condition is present. Such a condition occurs when "a portion of the an Area EPS is energized solely by one or more local EPSs through the associated PCCs while that portion of the Area EPS is electrically separated from the rest of the Area EPS" [8]. In other words, the portion of the EPS to which the ICS is connected becomes isolated, or islanded, from the rest of the Area EPS such that the voltage magnitude and frequency are no longer being regulated by the Area EPS. Per IEEE Std 1547 [4], an ICS should detect such a condition and disconnect itself within two seconds.

To verify this, IEEE Std 1547.1 prescribes a test (section 5.7 of IEEE Std 1547.1 [8]) in which the ICS is placed in parallel with a resonant RLC load and then disconnected from the Area EPS. This is done to replicate a worst-case condition in which an ICS could be found to be energizing a local EPS that has resonant properties and thus might appear to be energized by the Area EPS, when in reality it is not.

The procedure for this test begins with connecting the ICS in parallel with a resonant RLC load through a breaker or other electrical disconnection device (S3) to the simulated Area EPS as shown in Figure 4. The simulated Area EPS is then set to output voltage of nominal magnitude and frequency until the ICS begins normal operation. Once the ICS is online, the resonant RLC load is tuned until it absorbs all real power provided by the ICS, is operating at a quality factor of 1 ± 0.5, and the fundamental frequency current through S3 is less than 2% of the rated current of the ICS on a steady-state basis. Switch S3 is then opened and the time between the opening of the switch and when the ICS ceases to energize the RLC load is recorded. This procedure is then repeated multiple times for varying reactive power settings of the load (in 1% increments), with various output power settings of the ICS [8].

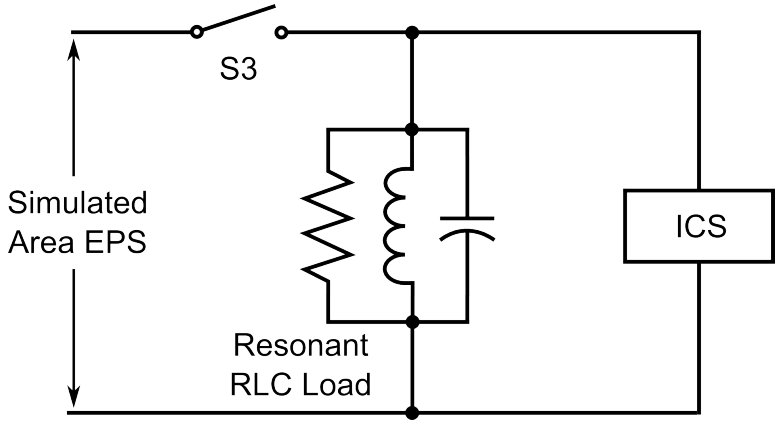

Figure 4: Unintentional Islanding Test Circuit
(Simplified version of Figure 2 of IEEE Std 1547.1 [8])

3 GISE Realization

3.1 Overview

The complete architecture of the GISE is shown in Figure 5.

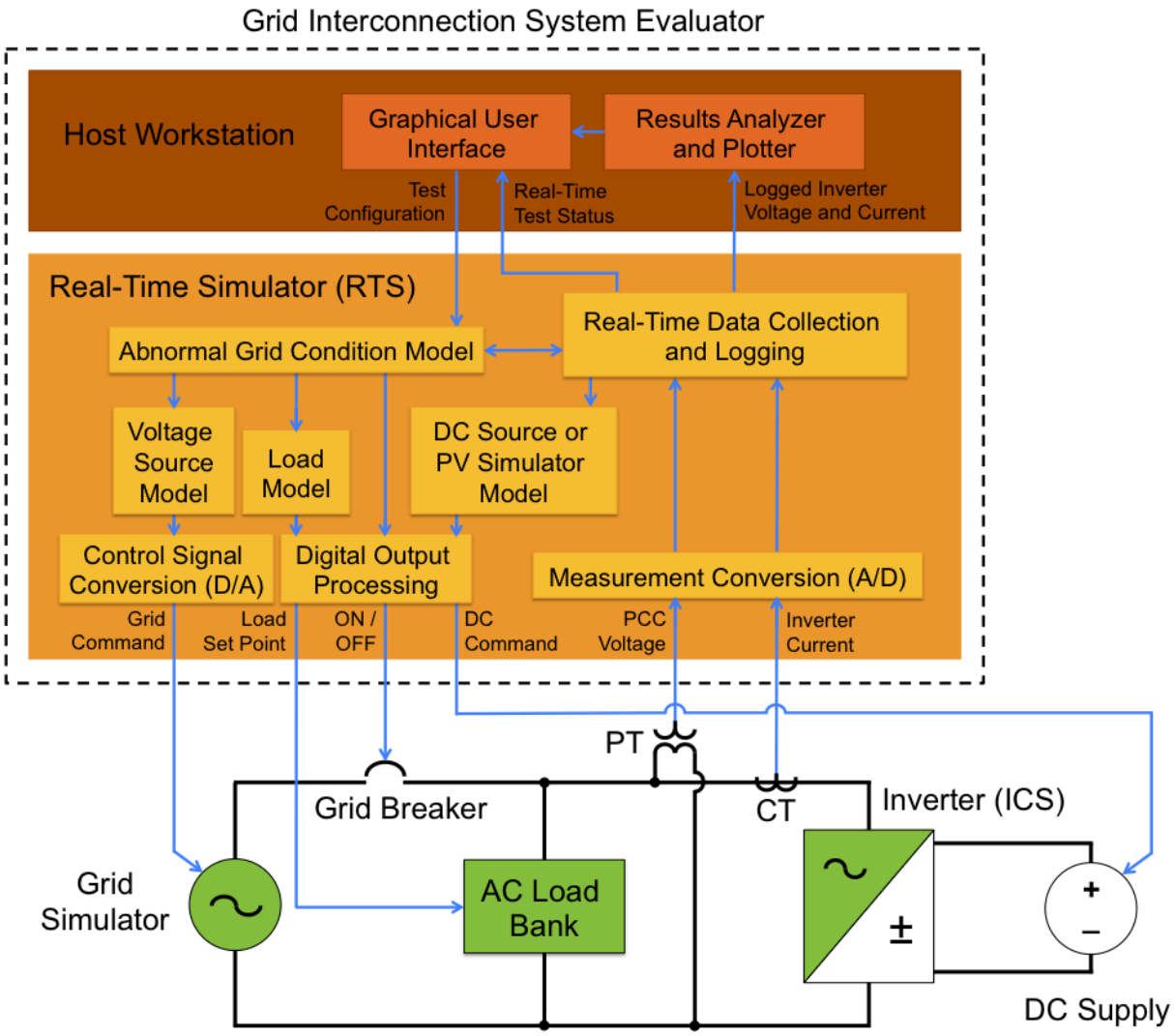

Figure 5: Grid Interconnection System Evaluator Architecture

It can be seen that the GISE is comprised of four major sections:

1. Electrical hardware setup
2. RTS and models
3. Results analyzer and plotter
4. Graphical user interface.

This section provides further detail on these four components.

3.2 Electrical Hardware Setup

The GISE's electrical hardware setup is shown in the test circuit at the bottom of Figure 5. In this test circuit, the grid simulator and grid breaker function as the simulated EPS point of common coupling, the ac load bank as the constant resistive or resonant RLC load (depending on test), and the dc supply as the DR being interconnected through the inverter ICS.

Specifically, the following electrical equipment was used for the tests described in this report:

- **Grid simulator**: 62.5 kVA (four units for up to 250 kVA available) voltage source configured for output in a 240 V_{rms} nominal, split-phase configuration in response to a line voltage waveform command. This unit will maintain output frequency within 0.01% and will regulate individual phase voltages within 0.5%. It has a frequency range of 47 to 500 Hz, a voltage range of 0 to 132 VL-N (before a step-up output transformer), and a slew rate of 1 V/µs. The analog control of this grid simulator, which is operated from the voltage source model running on the RTS, is very fast with response times of 300 µs for 100% load changes.
- **Grid breaker**: LSI molded case circuit breaker, 400A frame, electronic trip, with shunt trip and auxiliary contacts for status
- **AC load bank**: 436 kVA @ +/- 0.37 pf with 125 W and 312.5 VAR steps
- **DC supply**: 250 kW, 0-900 VDC
- **Inverter (ICS)**: A variety of commercial maximum power point tracking (MPPT) PV inverters rated for approximately 3 kW of power transfer capacity.
- **Potential transformer (PT)**: 40:1 turns ratio
- **Current transducer (CT)**: 10 mV/A, 10 kHz bandwidth

3.3 RTS and Models

3.3.1 Real-Time Simulator

The real-time simulator provides the key interface between the physical electrical components and the software models that control them. An example of this interaction for just the PV simulator is shown in Figure 7. The physical simulator used for the testing described in this report is an eMegaSim Wanda 4U model [16] from Opal-RT Technologies. The complete RTS model is developed using MATLAB Simulink, compiled into executable code using Mathworks' Real-Time Workshop, and deployed onto the RTS using Opal-RT's RT-LAB. Each of the individual key software models is described in the following sections.

3.3.2 Voltage Source Model

The voltage source model is shown in Figure 6.

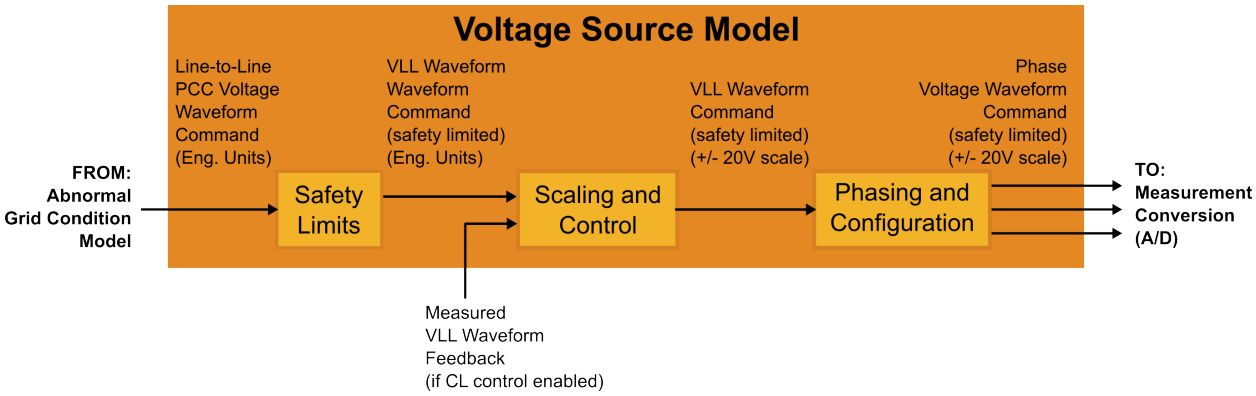

Figure 6: Voltage Source Model

This model is simple with only three key parts:

1. **Safety Limits** – limits the magnitude of the commanded waveform to ensure it is within the specified operating limits of the physical hardware.

2. **Scaling and Control** – scales the voltage command given in engineering units to an analog voltage range understood by the grid simulator's internal controller, and performs open-loop proportional or closed-loop proportional integral control on this scaled control signal depending on which method is enabled. By default, open-loop proportional control is used.

3. **Phasing and Configuration** – depending on how the ICS is electrically connected to the grid simulator, different phase voltage waveform commands are generated. By default, a split-phase configuration is used and the ICS under test is connected across phase A and phase B of a three-phase power system bus. Thus, phase A and phase B are enabled and 180 degrees out of phase with one another, and phase C is disabled.

3.3.3 Load Model

The ac load bank used for this testing is governed by an on-board controller, which opens and closes relays and switches to connect or disconnect the various R, L, and C elements to or from the physical power connections. The onboard controller must be commanded as to which relays to open or close by the RTS load model. Thus, the RTS load model interprets a user set point that includes the nominal voltage range (240 V or 480 V), the desired apparent power value in kVA, and the desired power factor, and, using knowledge of the available element combinations in the load bank, translates this set point into discrete on or off signals for all of the element relays and switches in the load bank.

For example, when a set point of 22 kVA at pf = 0.707 lagging (this is equivalent to a resistive load of 15.554 kW and an inductively reactive load of 15.554 kVAR) and 240 V is commanded, the relays corresponding to 240 V operation, a 15 kW resistor, a 500 W resistor, a 15 kVAR inductor, and a 312.5 VAR inductor would be commanded to be turned on and all other relays turned off. This set of relays is selected because, given the discrete resistive and inductive steps available, 15.5 kW and 15.3125 kVAR are the closest values that are less than or equal to the

commanded values of 15.554 kW and 15.554 kVAR. The relay states are then digitally communicated to the load bank's onboard controller for execution.

3.3.4 DC Source or PV Simulator Model

The dc power source used for this testing (shown in Figure 7 below) is governed via an on-board controller that manages the source's internal ac inverter unit and dc converter unit to affect the desired power transfer and voltage characteristics on both channels of the source. This controller accepts set points for the source's limits and commanded operating conditions, and communicates measured power transfer and voltage information for each channel via controller area network (CAN) digital communication. The RTS communicates via CAN with the dc power source controller to transfer these set points and measurements back and forth.

Within the RTS, a software model of either a dc source or a PV simulator is used to interpret measurements and provide set points. The dc source model takes a set point command input and then issues set points to the dc source in order to control the source's output to this commanded set point. The dc source model also reports measurements of the actual source's reported power transfer characteristics.

The PV simulator, the architecture of which is shown in Figure 7, leverages this simple dc source model by using its reported measurements, an internal model of a PV array, and a basic control system to provide the dc source model commands so that the dc source behaves as an actual photovoltaic array would. This PV model includes both response to varying environmental—solar irradiance and cell temperature—input conditions and dc output power transfer characteristics (e.g., appropriate voltage, current, and power output corresponding to each loading scenario). Further detail on the PV simulator is given in [5].

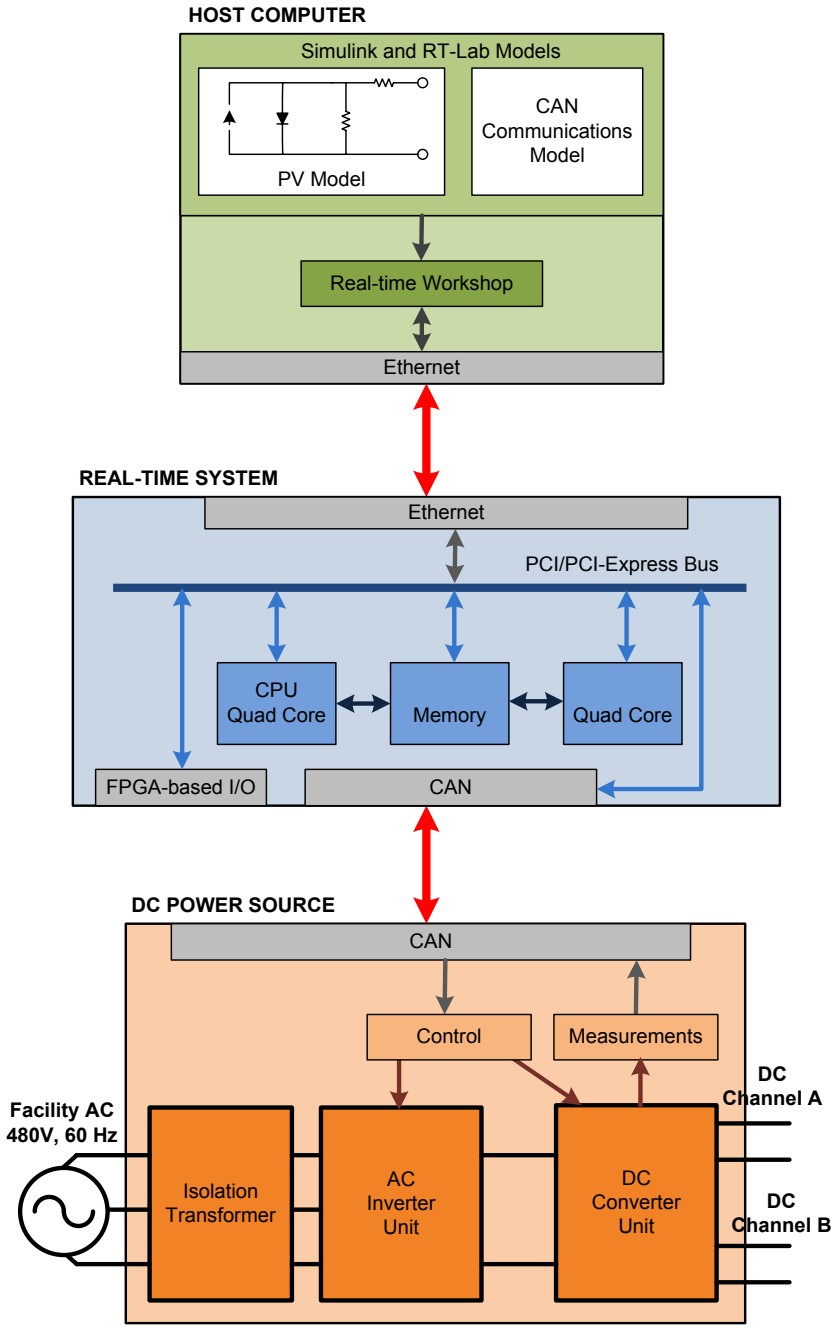

Figure 7: PV Simulator Architecture

3.3.5 Abnormal Grid Condition Model

The abnormal grid condition model, a block diagram of which is shown in Figure 8 below, is the core model of the GISE. This model contains two key subsystems:

1. **Test Waveform Generation** – generates the test waveforms for each of the three test intervals and a trigger signal depending on the user's test selection and configuration

2. **Test Sequencing and Control** – controls the overall timing of the test, ramps up and ramps down the overall test waveform, and sequences the three interval test waveforms so that they are executed at the correct times and there are no discontinuities between intervals. It sends the reference command to the voltage source model, load model, and grid breaker.

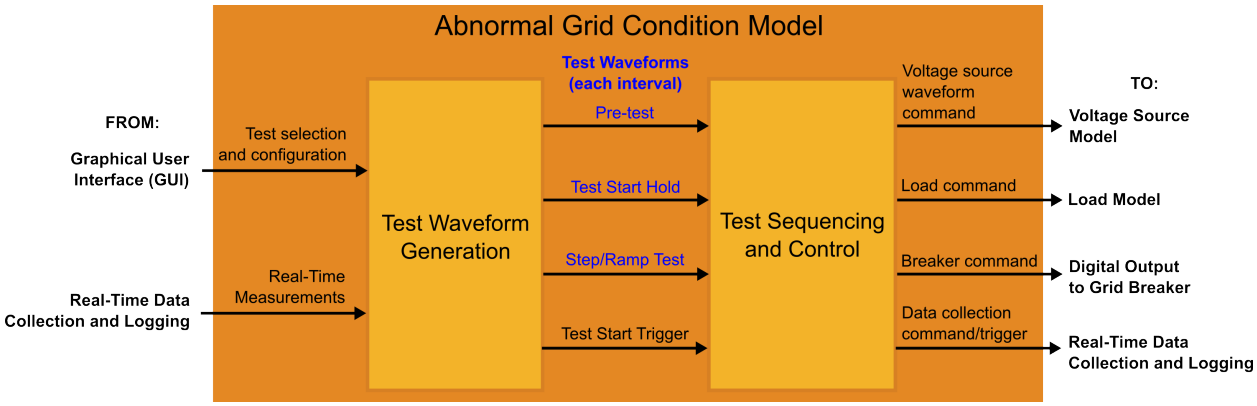

Figure 8: Abnormal Grid Condition Model

3.4 Results Analyzer and Plotter

The Results Analyzer and Plotter is a set of scripts implemented in MATLAB that analyze the raw data collected by the RTS and calculate a number of key parameters or waveforms:

1. **Time series of voltage magnitude (RMS) values over the test duration** – calculated on a full-cycle basis based on zero crossings

2. **Time series of current magnitude (RMS) values over the test duration** – calculated using the last full cycle of the current waveform data, as determined by zero crossing detection

3. **Time series of voltage frequency (Hz) values over the test duration** – calculated using the immediately previous two zero crossings (one full cycle)

4. **Voltage and frequency magnitudes immediately prior to the start of the three test intervals** (test intervals are described in section 4) – useful for verifying that the values specified in the test configuration are being properly commanded and in determining the actual step or ramp value that was commanded for a particular test

5. **Exact time and magnitude at which the ICS disconnected during the ramp/step test interval** (test intervals are described in section 4) – the key parameter being measured for all tests. The time at which the ICS disconnected is calculated based on when the current waveform first deviates from its periodic waveform towards zero (a complex algorithm examining first and second derivatives of the current is employed to determine this). This value and the point in time at which the ramp/step test interval began are then used to

calculate the ICS's trip time. The magnitude at which the ICS disconnected is calculated based on the full cycle immediately previous to disconnection.

These key parameters are then used to generate a summary test report. An example summary test report from an undervoltage time interconnection conformance test is shown in Figure 9. There are four key sections to this report:

1. **Report Header** – shows a tabular summary of the user's specified parameters (left) and the relevant results (right) for the test. The results table varies slightly depending on the test being run; the results table includes the measured ramp slope for magnitude/ramp tests and the measured step magnitude for time/step tests. This section is useful in quickly determining whether the ICS passed the test in question.

2. **Top Plot** – shows RMS values of the ICS's current and voltage magnitude, in addition to the frequency of the voltage waveform, as a function of time over the course of the entire test. The three test intervals (pre-test, test start hold, and ramp/step test) are delineated by the vertical lines.

3. **Middle Plot** – shows the ICS current and voltage waveforms over the course of the entire test. This plot adds additional detail to the top plot, in that one can better spot any periodic abnormalities in current output from the waveform.

4. **Bottom Plot** – shows the ICS current and voltage waveforms just before and after the inverter tripped. This plot is most useful for determining what the ICS's current waveform looked like right as it tripped.

For every test that is run, a summary test report of this same format is generated. The raw data for each test is also saved and available for further examination offline.

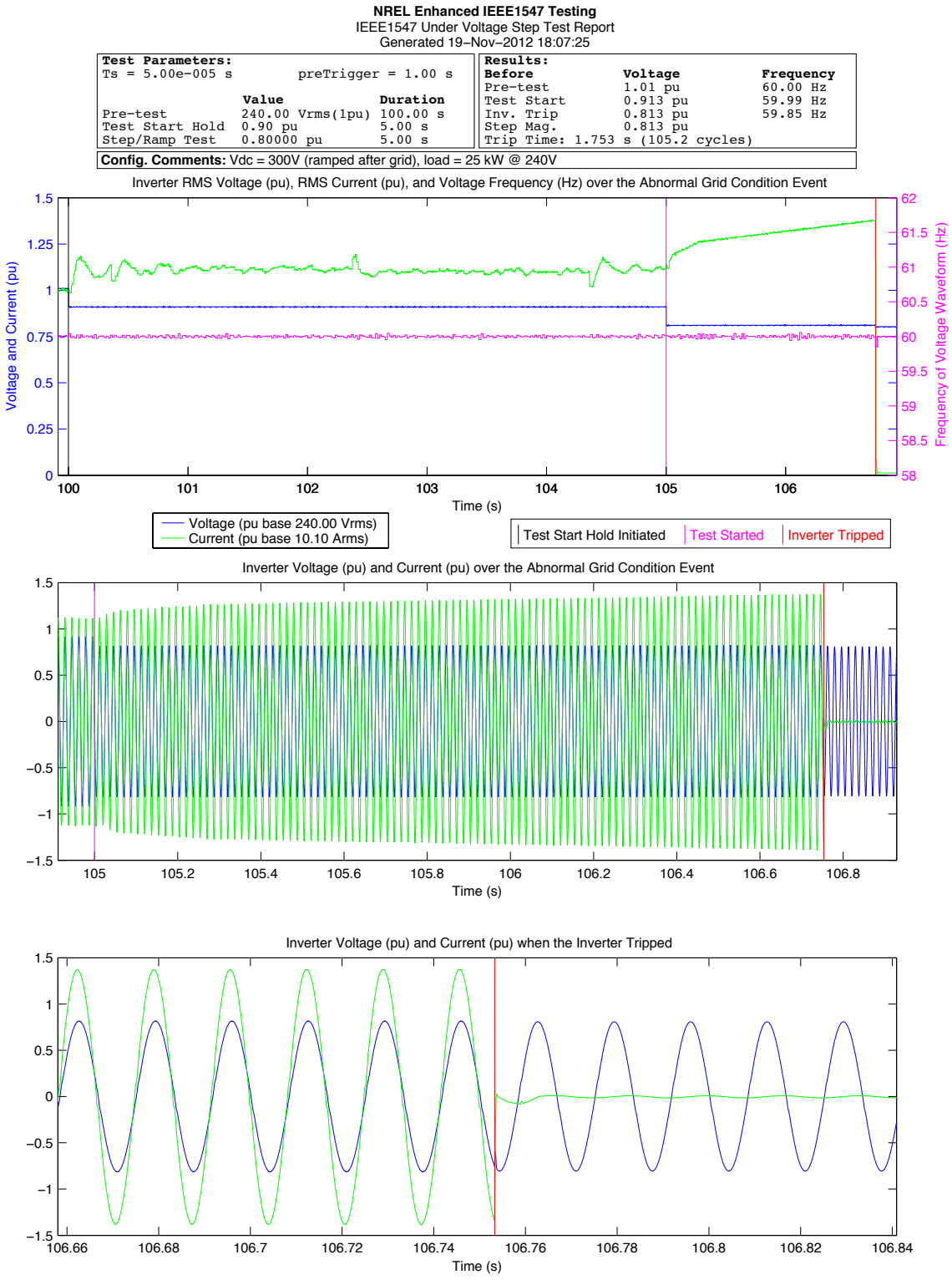

Figure 9: Example Summary Test Report for an Undervoltage Time/Step Test

3.5 Graphical User Interface

Figure 10 shows a screenshot of the GUI from which a user can configure, run, monitor, and view results of grid interconnection conformance tests. Configuration takes place at the top of the screen where the user selects the desired tests, enters the relevant parameters, and enters a comment if desired. A graphic at right assists the user with understanding the parameters being entered as they relate to the selected test. Once configured, the user presses "Start Test," which will verify that the entered parameters are valid and then execute the test using the RTS.

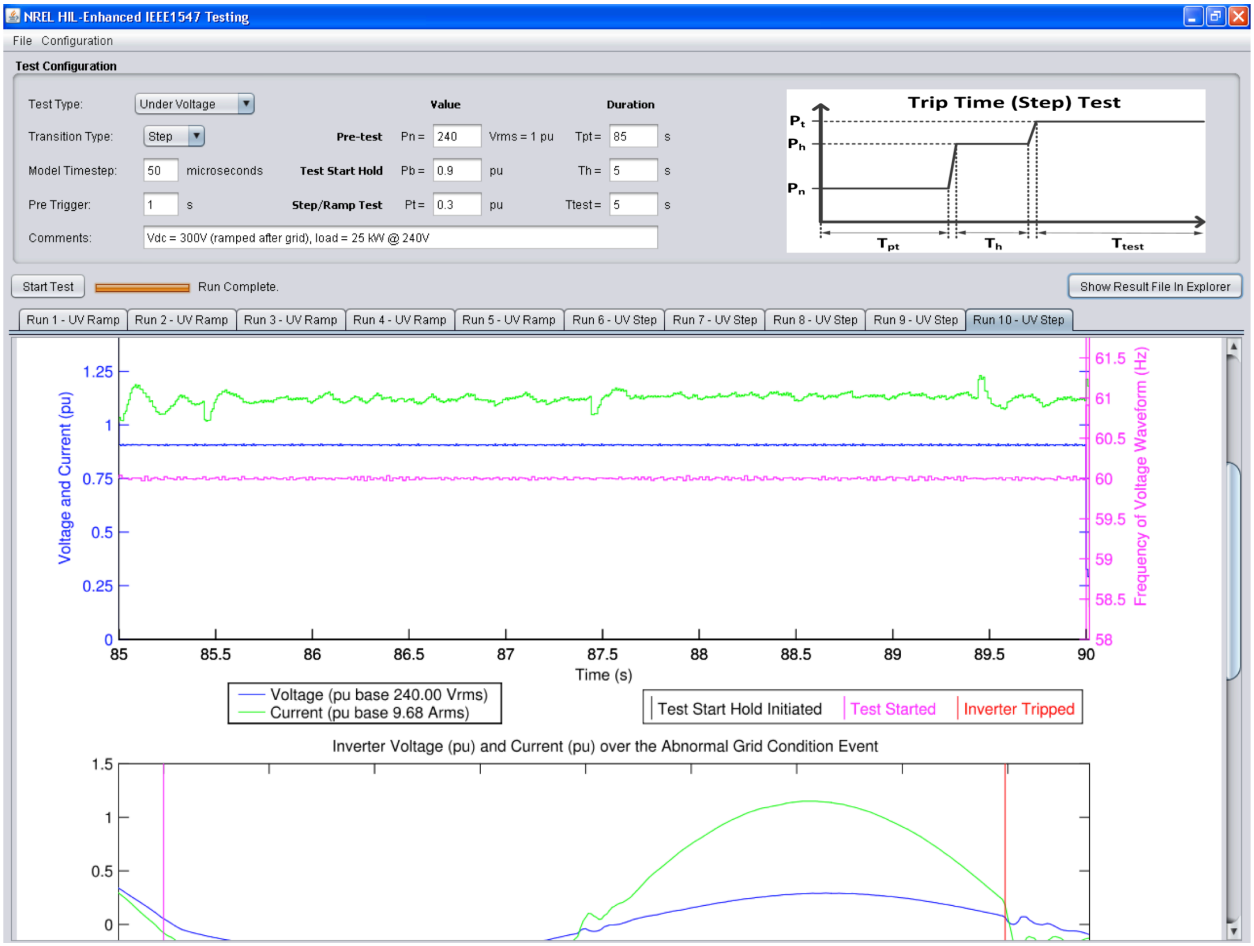

Figure 10: Graphical User Interface

Upon test completion, the GUI collects the test data logged by the RTS over the entire test and sends that to the results analyzer and plotter. Once analysis is finished, a new results tab with the generated report (see Figure 9 for an example) is opened at the bottom of the screen. All results of the test are available in this PDF report, and raw data is also saved. More detail about the configuration and sequence of specific tests is given in section 4 below.

4 GISE Test Configuration and Sequence

Successfully executing a grid interconnection conformance test using the GISE consists of the following steps:

1. **Equipment Setup** – the user connects and configures the ICS under test and the relevant electrical equipment, as shown in Figure 5, while following the relevant manufacturer guidance and taking proper safety precautions.

2. **Test Configuration** – using the Test Configuration portion of the GUI, a zoomed-in view of which is shown in Figure 11, the user specifies:

    - **Test Type**:
        - Overvoltage (OV)
        - Undervoltage (UV)
        - Overfrequency (OF)
        - Underfrequency (UF)
        - Unintentional Islanding (UI)

    - **Transition Type** (only applicable for OV, UV, OF, or UF tests):
        - Step/Time - measures the amount of time required by the ICS to respond to and disconnect after an abnormal grid condition is detected
        - Ramp/Magnitude - measures the voltage or frequency magnitude at which the ICS disconnected

    - **Model Timestep** – defines how fast the model runs and thus how fast data collection occurs. The default value of 50 microseconds is generally sufficient. The user is allowed to enter values between 10 and 100 microseconds.

    - **Pre Trigger** – amount of time in seconds before the Test Start Hold interval begins (at T_{pt} of Figure 3) to log test data. Data is logged from T_{pt} – Pre Trigger until the end of the test. The user is allowed to enter values between 0.01 and 10 seconds, though the default of 1 second is recommended.

    - **Nominal parameter (voltage or frequency) magnitude and interval duration for the three intervals during testing**:

        - **Pre-test** – used to allow the inverter to wake-up, synchronize, etc. Shown as the duration T_{pt} in Figure 3, which is also displayed to the user when entering this value into the GUI (see Figure 10). Value is specified in units of V_{rms} and the duration is specified in seconds.

        - **Test Start Hold** – temporary period immediately before test occurs during which the starting parameter value (P_b) is held (explained in section 2.1). Shown as the duration T_h in Figure 3, which is also displayed to the user when entering this value into the GUI (see Figure 10). Value is specified in per unit (pu) for voltage tests and Hertz (Hz) for frequency tests. Duration is specified in seconds.

- **Step/Ramp Test** – period during which the specified test occurs. Shown as the duration T_{test} in Figure 3, which is also displayed to the user when entering this value into the GUI (see Figure 10). Value P_t, either the desired value to step to for time tests or the desired ramp rate for magnitude tests, is specified in pu or pu/s for voltage tests and Hz or Hz/s for frequency tests. Duration is specified in seconds.

- **Comments** – useful for noting any details about the test configuration of the particular ICS under test

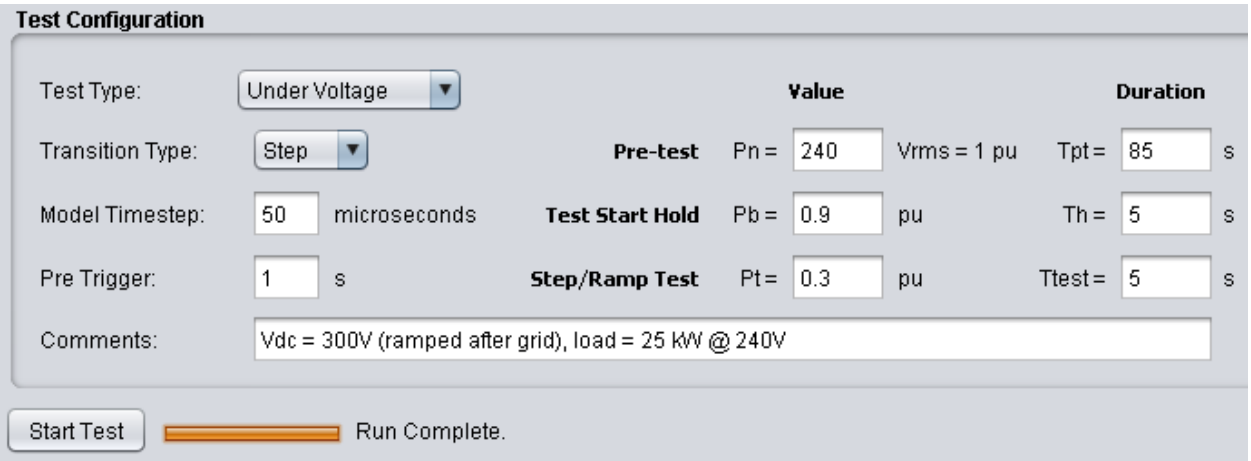

Figure 11: Test Configuration and Status Portion of the GUI

3. **Parameter Verification and Test Execution** – once the user sets the configuration parameters above, the "Start Test" button is pushed. Upon this action, the specified parameters are then verified to ensure that they make sense given the selected test and transition type, are within the allowable ranges for each of the parameters, and won't cause any equipment to be commanded to an unsafe condition (e.g., too high a voltage or frequency commanded on the grid simulator). Next, the configuration is communicated to the RTS, which then builds its model and executes the test in three intervals. The user is apprised of real-time test status throughout the test via the GUI status progress bar and message shown at the bottom of the Test Configuration section. Figure 11 shows the progress bar and message configuration that are displayed when a test is complete. In the middle of a test, varying status messages and progress bar completions are shown that tell the user when the RTS model is being built, being loaded, what interval of testing is occurring, if analysis after the test is being completed, or when the test is complete.

4. **Results** – upon test completion, data collected throughout the test is passed from the RTS to the Results Analyzer and Plotter, where the result parameters are calculated and plots created. This information is then organized into a report, described in the next section, and displayed to user in the same GUI. The results from each test run are displayed in a new tab, as shown for the 10 tests of Figure 10, so that many test runs can be completed in a short succession and the results easily compared. The reports are automatically saved as a PDF

document that can be located in the workstation's operating system by the Show Result File in Explorer button.

5. **Repeat Steps 2-4** – these steps are repeated for each additional test run. If the test configuration specified in step 2 doesn't change between test runs, the RTS model is not compiled and the testing period begins immediately.

5 GISE Test Results

5.1 Test Setup and Methodology

For demonstration of the GISE, three different commercial PV inverters were tested as the ICSs under test. These three inverters all had power transfer capability ratings of around 3 kW and were connected to the simulated Area EPS in a split-phase 240 V configuration. The grid simulator was operated using analog waveform control from the RTS voltage source model as described in section 3.2. The ac load bank was given a constant load set point of 10 kW by the RTS load model for over and undervoltage and frequency tests. For unintentional islanding tests, the load bank was manually tuned to resonant conditions via user interaction with the load model. For these tests, the dc power source was commanded by the RTS dc source model to operate in voltage control mode with a constant voltage appropriate for each inverter.

Selected results for each of the nine IEEE 1547.1 interconnection conformance tests that were performed (overvoltage time, overvoltage magnitude, undervoltage time, undervoltage magnitude, overfrequency time, overfrequency magnitude, underfrequency time, underfrequency magnitude, and unintentional islanding) are shown and described in the following sections. The results presented were selected in order to present the GISE's functionality to perform these nine interconnection tests across a variety of ICSs with varying topologies; they are not intended to be a complete (e.g., the appropriate number of repetitions, etc.) set of tests according to the procedures of 1547.1. Complete results, including the summary report shown in section 3.4 and a raw data file, were collected for each individual test run. However, instead of showing the summary report for every test, each set of tests is summarized using a table of results that describes the overall strategy and purpose of individual test runs, and a plot of multiple repeated identical test runs, that demonstrates the repeatability and accuracy of the GISE's execution of the test set and the slight variability in ICS output response for each test run. This plot has a very similar format to the example test report of Figure 9 in that it shows the RMS voltage, the RMS current, and the calculated (on a full-cycle basis) frequency over the course of the test run's three intervals (delineated with vertical lines).

5.2 OV Tests

5.2.1 Time

A selection of the overvoltage time test results is given in Table 1. The first five test runs were for identical configuration parameters, and results from these specific runs are shown in Figure 12 to demonstrate the repeatability and accuracy of the GISE's execution of the test set and the slight variability in ICS output response for each test run. In examining Figure 12, one will notice that the RMS voltages for the set of tests are all very similar, as demonstrated by very low standard deviations. The standard deviation does increase slightly around step events as

sometimes one test run made the step change one time step before another test run, resulting in a larger instantaneous standard deviation. This plot also shows that there are some fairly significant frequency deviations associated with these overvoltage time test runs. In general, these frequency deviations, the largest of which reached 61.8 Hz (cyan color, after the first step transition, off the chart), occur after step transitions and thus are expected. This particular plot did have one excursion between step transitions that appears to be an anomaly.

Table 1: Summary of Selected Overvoltage Time Tests

Test Run #	PT Hold Magnitude P_b (pu)	PT Hold Duration T_h (s)	Test Magnitude P_t (pu)	Test Duration T_{test} (s)	Trip Time (s)	Comments
OVS-1	1.15	0.32	1.21	1	0.141	
OVS-2	1.15	0.32	1.21	1	0.125	Demonstrates the fast overvoltage trip timing of the ICS. Shown in Figure 12.
OVS-3	1.15	0.32	1.21	1	0.124	
OVS-4	1.15	0.32	1.21	1	0.125	
OVS-5	1.15	0.32	1.21	1	0.141	
OVS-6	1.08	5	1.15	5	0.736	
OVS-7	1.08	5	1.15	5	0.722	Demonstrates the slow overvoltage trip timing of the ICS at two different magnitudes.
OVS-8	1.08	5	1.15	5	0.738	
OVS-9	1.08	5	1.15	5	0.753	
OVS-10	1.08	5	1.15	5	0.976	
OVS-11	1.08	5	1.11	5	0.736	
OVS-12	1.08	5	1.20	5	0.128	Demonstrates fast overvoltage trip timing at various magnitudes in the fast trip range. (Note that OVS-12 through OVS-14 weren't conducted completely according to IEEE 1547.1 (PT hold value and duration), but were preliminary tests that demonstrated various magnitudes in the fast trip range).
OVS-13	1.08	5	1.21	5	0.144	
OVS-14	1.08	5	1.23	5	0.025	

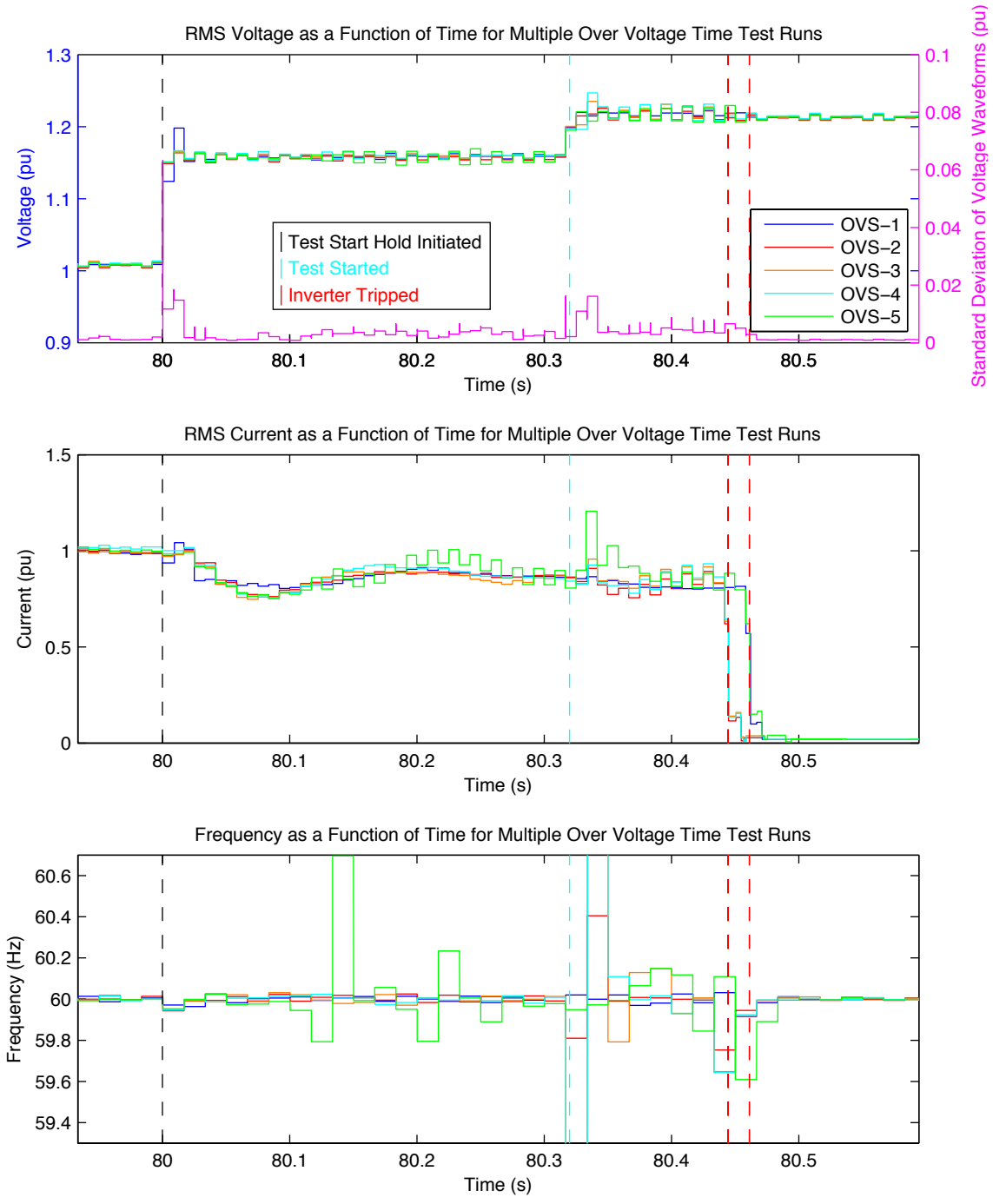

Figure 12: Multiple Overvoltage Time Test Runs

5.2.2 Magnitude

A selection of the overvoltage magnitude test results is given in Table 2. The first three test runs were for identical configuration parameters, and results from these specific runs are shown in Figure 13 to demonstrate the repeatability and accuracy of the GISE's execution of the test set and the slight variability in ICS output response for each test run. In examining Figure 13, one will notice that the RMS voltages for the set of tests are all very similar, as demonstrated by very low standard deviations.

Table 2: Summary of Selected Overvoltage Magnitude Tests

Test Run #	PT Hold Magnitude P_b (pu)	PT Hold Duration T_h (s)	Ramp Rate M_{ramp} (pu/s)	Trip Magnitude (pu)	Comments
OVR-1	1.08	5	0.001	1.096	Demonstrates the slow overvoltage trip magnitude of the ICS. OVR-1 through OVR-3 are shown in Figure 13.
OVR-2	1.08	5	0.001	1.097	
OVR-3	1.08	5	0.001	1.097	
OVR-4	1.08	5	0.00272	1.1	
OVR-5	1.08	5	0.001	1.098	
OVR-6	1.08	5	0.001	1.099	
OVR-7	1.08	5	0.001	1.097	
OVR-8	1.08	5	0.001	1.092	
OVR-9	1.18	0.32	0.00545	1.193	Demonstrates the fast overvoltage trip magnitude of the ICS.
OVR-10	1.18	0.32	0.00545	1.192	
OVR-11	1.175	0.32	0.00545	1.187	
OVR-12	1.175	0.32	0.00545	1.19	
OVR-13	1.175	0.32	0.00545	1.191	

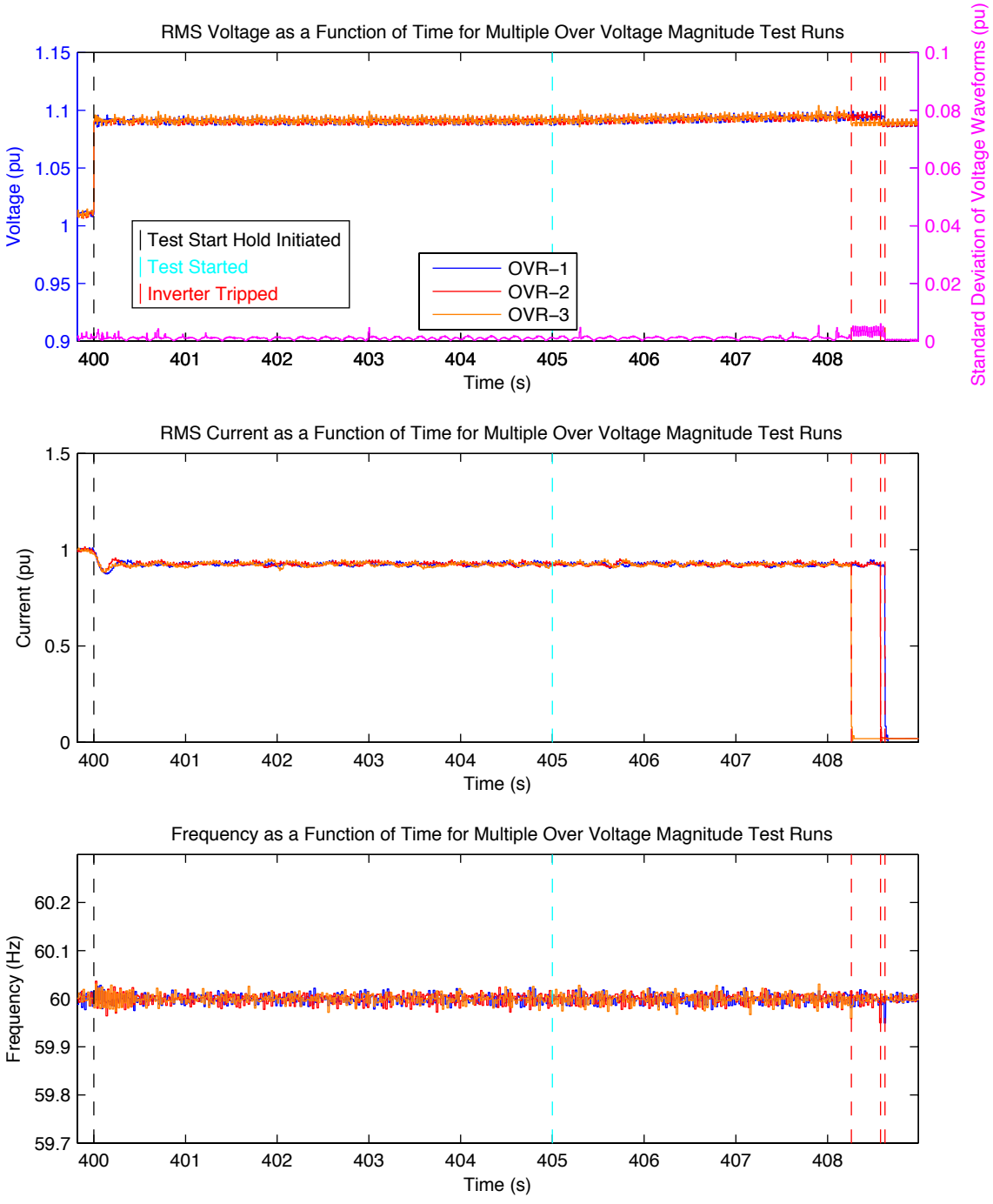

Figure 13: Multiple Overvoltage Magnitude Test Runs

5.3 UV Tests

5.3.1 Time

A selection of the overvoltage time test results is given in Table 3. The first five test runs were for identical configuration parameters, and results from these specific runs are shown in Figure 14 to demonstrate the repeatability and accuracy of the GISE's execution of the test set and the slight variability in ICS output response for each test run. In examining Figure 14, one will notice that the RMS voltages for the set of tests are all very similar, as demonstrated by very low standard deviations. The standard deviation does increase slightly around step events as sometimes one test run made the step change one time step before another test run, resulting in a larger instantaneous standard deviation. This plot also shows that there are some frequency deviations associated with these undervoltage magnitude test runs. These frequency deviations occur after step transitions and thus are expected.

Table 3: Summary of Selected Undervoltage Time Tests

Test Run #	PT Hold Magnitude P_b (pu)	PT Hold Duration T_h (s)	Test Magnitude P_t (pu)	Test Duration T_{test} (s)	Trip Time (s)	Comments
UVS-1	0.51	0.32	0.47	5	0.119	
UVS-2	0.51	0.32	0.47	5	0.136	Demonstrates the fast undervoltage trip timing of the ICS. Shown in Figure 14.
UVS-3	0.51	0.32	0.47	5	0.136	
UVS-4	0.51	0.32	0.47	5	0.119	
UVS-5	0.51	0.32	0.47	5	0.136	
UVS-6	0.93	5	0.85	5	1.787	
UVS-7	0.93	5	0.85	5	1.803	Demonstrates the slow undervoltage trip timing of the ICS.
UVS-8	0.93	5	0.85	5	1.803	
UVS-9	0.93	5	0.85	5	1.787	
UVS-10	0.93	5	0.85	5	1.803	
UVS-11	0.9	5	0.85	5	1.993	Demonstrates slow undervoltage trip timing at various magnitudes in the slow trip range.
UVS-12	0.9	5	0.8	5	1.753	
UVS-13	0.9	5	0.7	5	1.753	
UVS-14	0.9	5	0.55	5	1.736	
UVS-15	0.9	5	0.4	5	0.144	Demonstrates fast undervoltage trip timing at various magnitudes in the fast trip range. (Note that UVS-15 and -16 weren't conducted completely according to IEEE 1547.1 (PT hold value and duration), but were preliminary tests that demonstrated various magnitudes in the fast trip range).
UVS-16	0.9	5	0.3	5	0.016	
UVS-17	0.51	0.32	0.47	0.5	0.134	

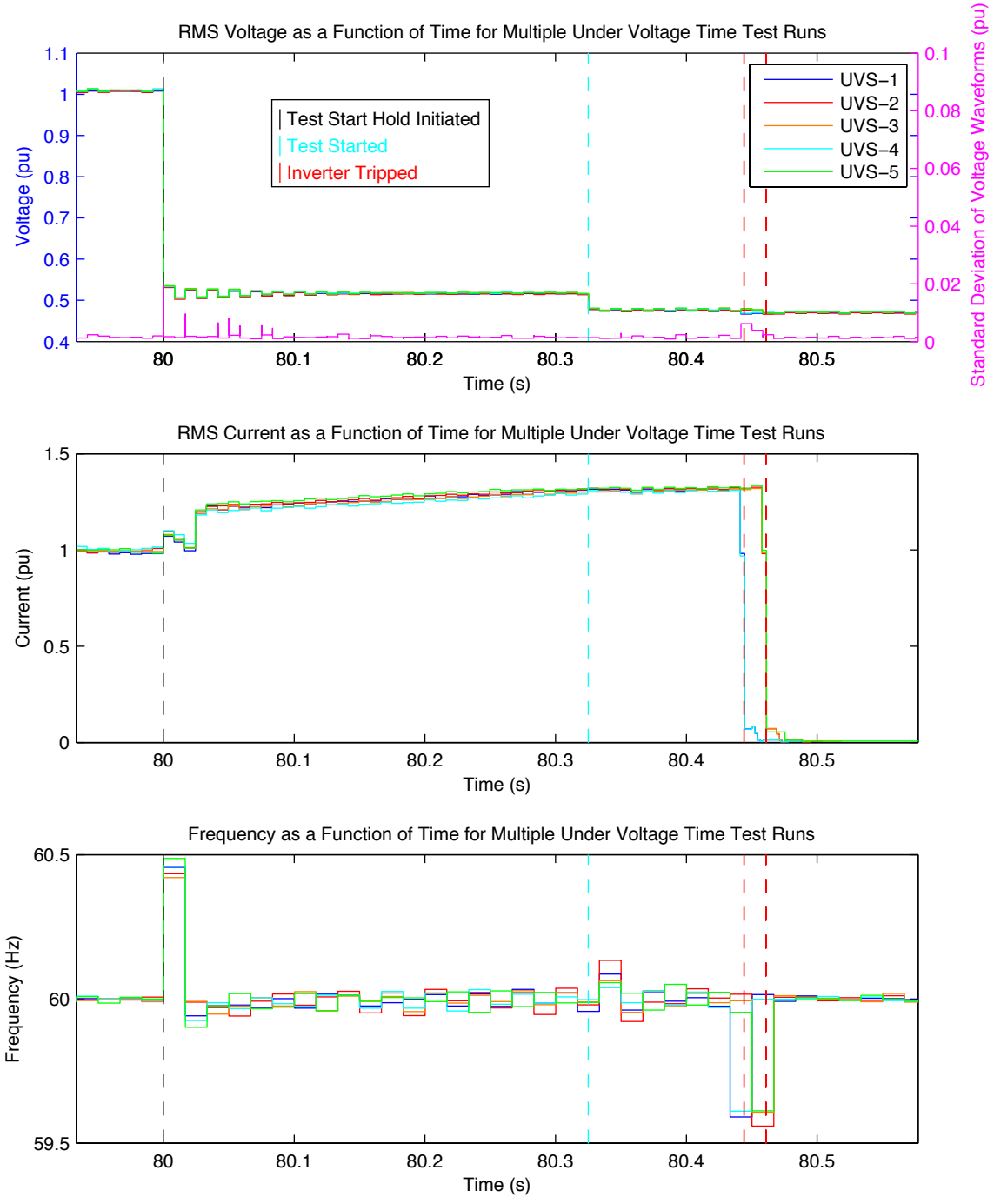

Figure 14: Multiple Undervoltage Time Test Runs

5.3.2 Magnitude

A selection of the undervoltage magnitude test results is given in Table 4. The last five test runs were for very similar configuration parameters, and results from these specific runs are shown in Figure 15 to demonstrate the repeatability and accuracy of the GISE's execution of the test set and the slight variability in ICS output response for each test run. In examining Figure 15, one will notice that the RMS voltages for the set of tests are all very similar, as demonstrated by very low standard deviations. The standard deviation does increase slightly around step events as sometimes one test run made the step change one time step before another test run, resulting in a larger instantaneous standard deviation. The RMS voltages and RMS currents of each test run are just slightly offset from one another as compared to other test sets where they are right on top of one another. This is because the pre-test hold magnitudes for the five tests included three very close, but not identical, values as shown in Table 4.

Table 4: Summary of Selected Undervoltage Magnitude Tests

Test Run #	PT Hold Magnitude P_b (pu)	PT Hold Duration T_h (s)	Ramp Rate M_{ramp} (pu/s)	Trip Magnitude (pu)	Comments
UVR-1	0.9	5	-0.001	0.884	Demonstrates the slow undervoltage trip magnitude of the ICS for various ramp rates.
UVR-2	0.9	5	-0.001	0.887	
UVR-3	0.9	5	-0.001	0.887	
UVR-4	0.9	5	-0.001	0.887	
UVR-5	0.9	5	-0.001	0.885	
UVR-6	0.9	5	-0.00272	0.884	
UVR-7	0.9	5	-0.0005	0.877	
UVR-8	0.502	0.32	-0.00272	0.509	Demonstrates the fast undervoltage trip magnitude of the ICS.
UVR-9	0.5	0.32	-0.00272	0.508	
UVR-10	0.495	0.32	-0.00272	0.503	
UVR-11	0.495	0.32	-0.00272	0.501	
UVR-12	0.495	0.32	-0.00272	0.5	

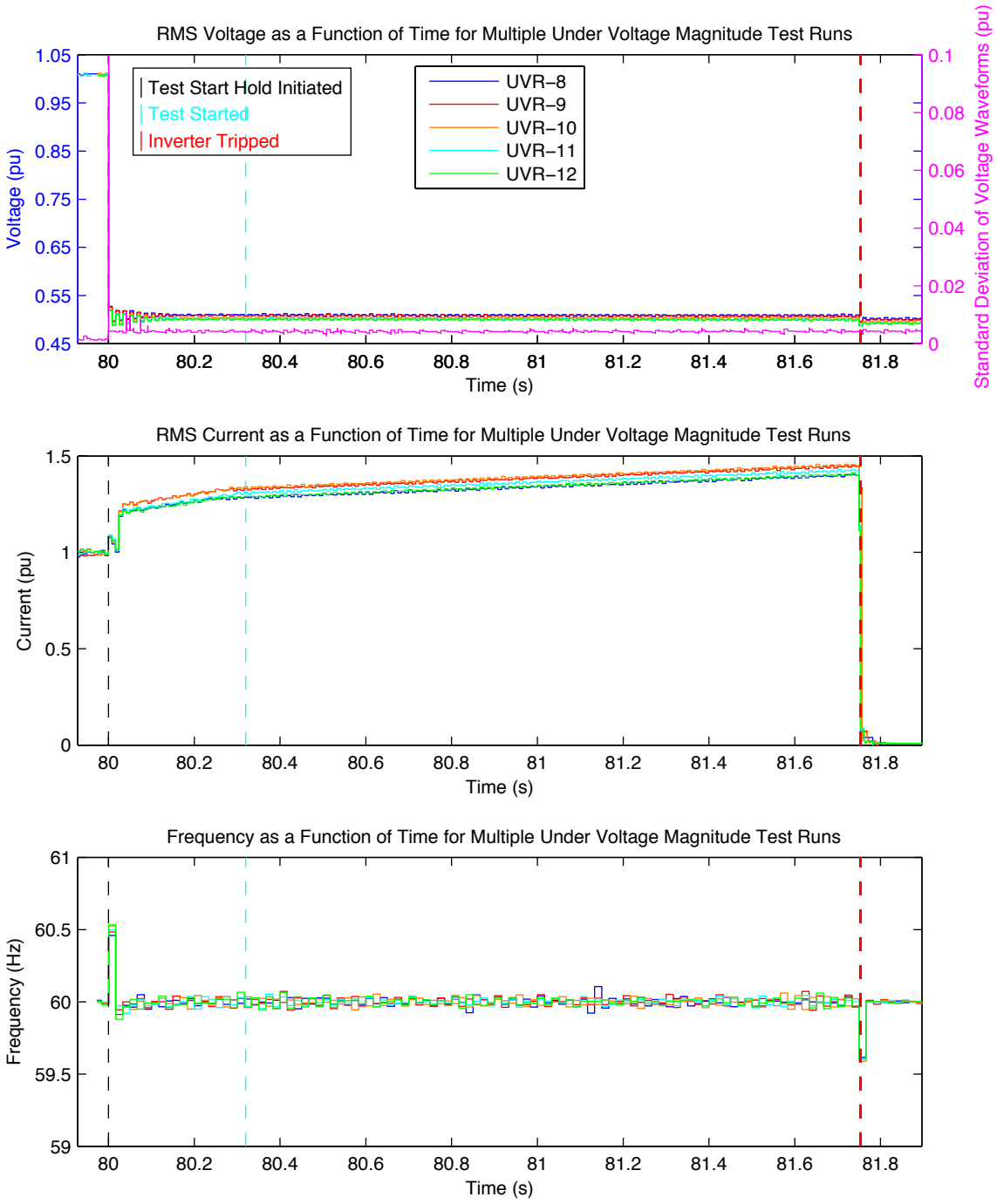

Figure 15: Multiple Undervoltage Magnitude Test Runs

5.4 OF Tests

5.4.1 Time

A selection of the overfrequency time test results is given in Table 5. Figure 16 shows a plot of the first four of the test runs listed in Table 5 in order to demonstrate the repeatability and accuracy of the GISE's execution of the test set and the slight variability in ICS output response for each test run. In examining Figure 16, one will notice that the frequencies for the two sets of tests are nearly identical. This plot also shows that there are some oscillatory deviations in the currents for each run. These deviations are due to the fact that the inverters under test had MPPT control enabled, but were drawing power from the fixed dc source, and the output current tended to hunt. This behavior was observed as normal for all inverters tested.

Table 5: Summary of Selected Over Frequency Time Tests

Test Run #	PT Hold Magnitude P_b (Hz)	PT Hold Duration T_h (s)	Test Magnitude P_t (Hz)	Test Duration T_{test} (s)	Trip Time (s)	Comments
OFS-1	60.2	5	61	2	0.109	Demonstrates the overfrequency trip timing of the ICS. Shown in Figure 16.
OFS-2	60.2	5	61	2	0.109	
OFS-3	60.2	5	62	2	0.116	
OFS-4	60.2	5	62	2	0.102	
OFS-5	60.2	5	63	2	0.117	Further demonstrates the overfrequency trip timing of the ICS at other PT hold and test magnitudes.
OFS-6	60.3	2	61	2	0.141	

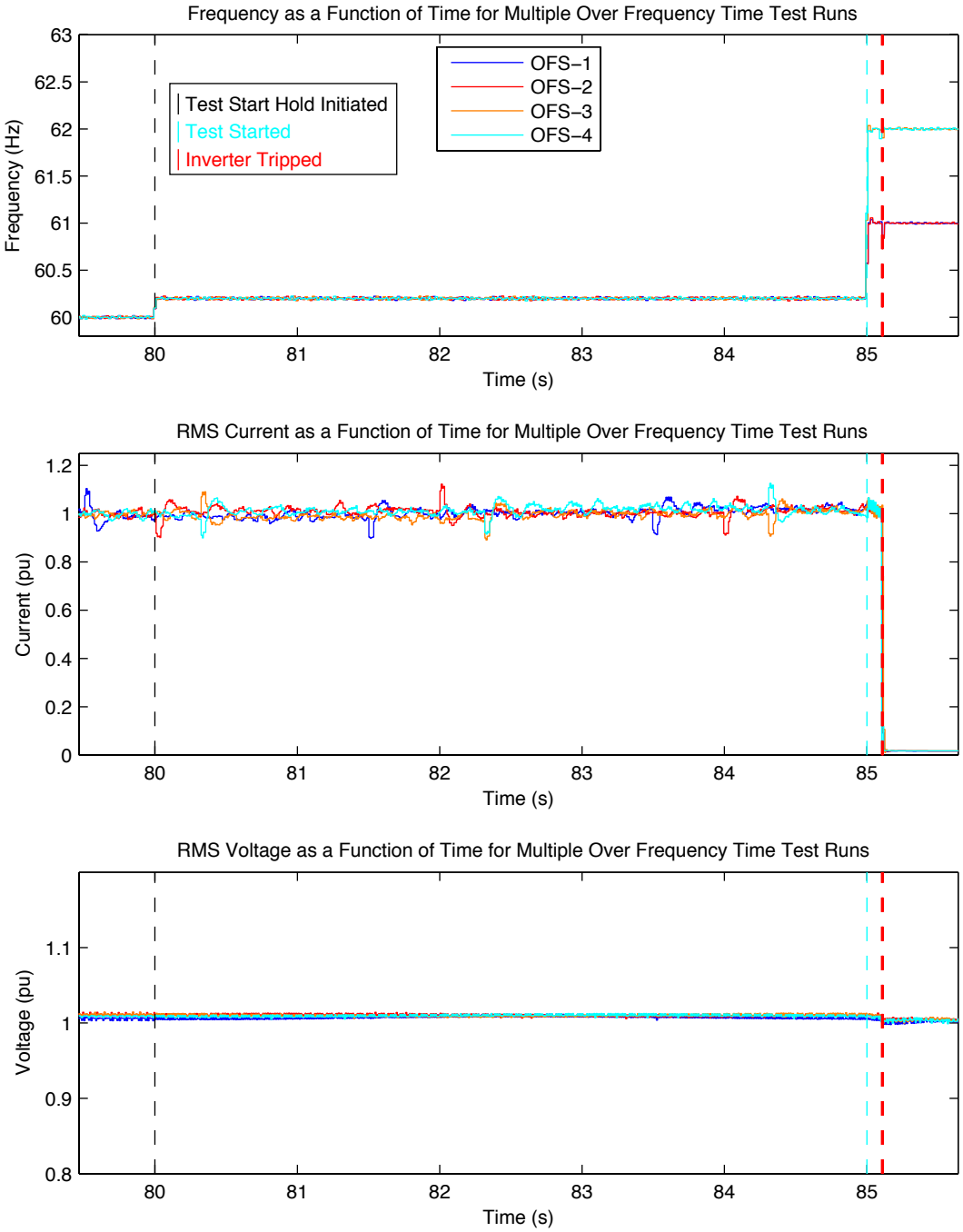

Figure 16: Multiple Over Frequency Time Test Runs

5.4.2 Magnitude

A selection of the overfrequency magnitude test results is given in Table 6. Figure 17 shows a plot of the first five of the test runs listed in Table 6 to demonstrate the ability of the GISE to execute tests over a range of different ramp rates and the variability in ICS output response for each test run. In examining Figure 17, one will notice there are some oscillatory deviations in the currents for each run. These deviations are due to the fact that the inverters under test had MPPT control enabled, but were drawing power from the fixed dc source, and the output current tended to hunt. This behavior was observed as normal for all inverters tested.

Table 6: Summary of Selected Over Frequency Magnitude Tests

Test Run #	PT Hold Magnitude P_b (Hz)	PT Hold Duration T_h (s)	Ramp Rate M_{ramp} (Hz/s)	Trip Magnitude (Hz)	Comments
OFR-1	60.2	5	0.093	60.38	
OFR-2	60.2	5	0.045	60.4	Demonstrates the overfrequency trip magnitude of the ICS for various ramp rates. Shown in Figure 17.
OFR-3	60.2	5	0.045	60.4	
OFR-4	60.2	5	0.02	60.4	
OFR-5	60.2	5	0.015	60.4	
OFR-6	60.3	2	0.015	60.41	Further demonstrates the overfrequency trip magnitude of the ICS for various ramp rates from a different starting value.
OFR-7	60.3	2	0.025	60.44	

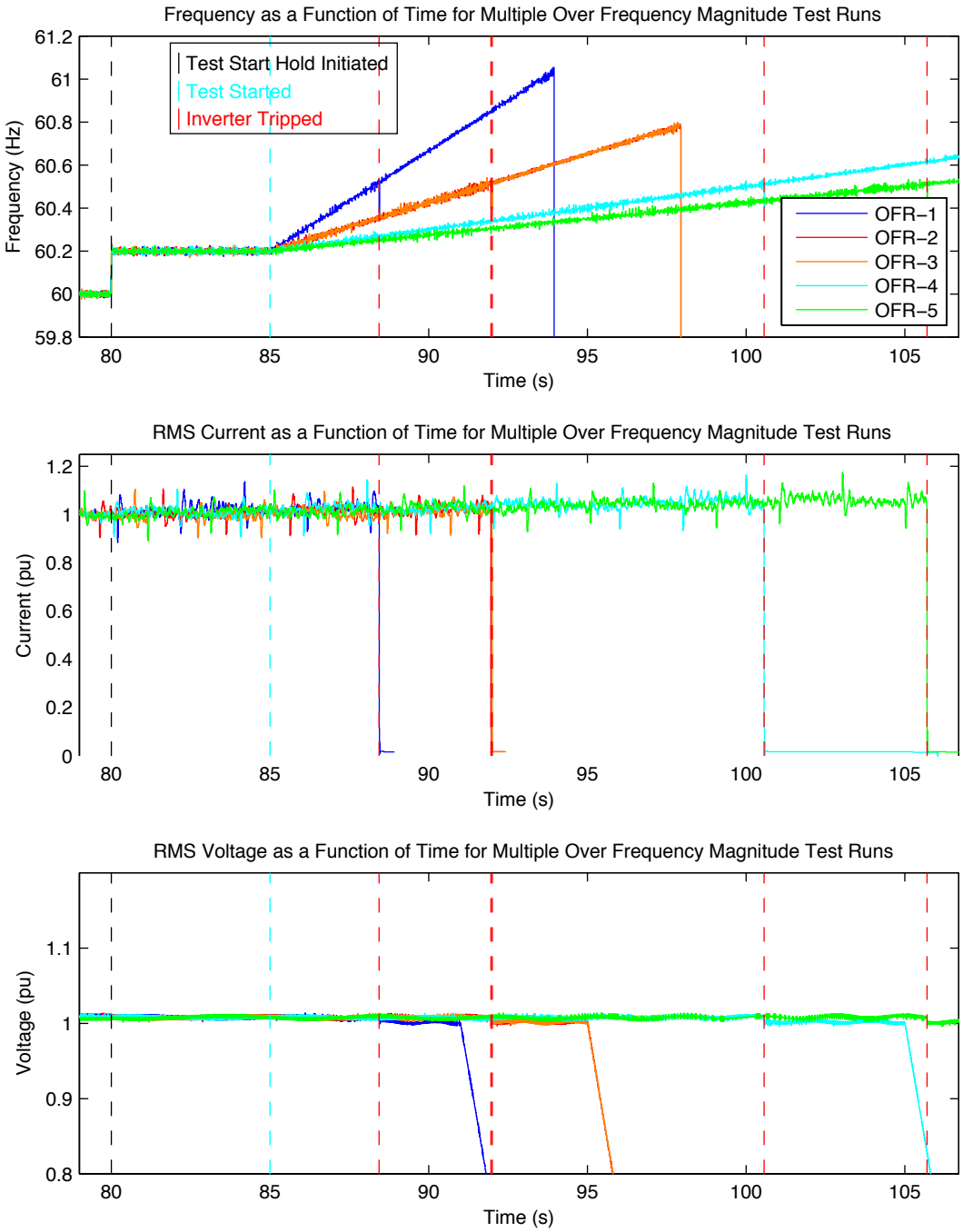

Figure 17: Multiple Over Frequency Magnitude Test Runs

5.5 UF Tests

5.5.1 Time

A selection of the underfrequency time test results is given in Table 7. Figure 18 shows a plot of the first three of the test runs listed in Table 7 to demonstrate the repeatability and accuracy of the GISE's execution of the test set and the slight variability in ICS output response for each test run. In examining Figure 18, one will notice that the frequencies for the two sets of tests are nearly identical. This plot also shows that there are some oscillatory deviations in the currents for each run. These deviations are due to the fact that the inverters under test had MPPT control enabled, but were drawing power from the fixed dc source, and the output current tended to hunt. This behavior was observed as normal for all inverters tested.

Table 7: Summary of Selected Underfrequency Time Tests

Test Run #	PT Hold Magnitude P_b (Hz)	PT Hold Duration T_h (s)	Test Magnitude P_t (Hz)	Test Duration T_{test} (s)	Trip Time (s)	Comments
UFS-1	59.6	5	59	2	0.123	Demonstrates the underfrequency trip timing of the ICS. Shown in Figure 18.
UFS-2	59.6	5	59	2	0.106	
UFS-3	59.6	5	59	2	0.102	
UFS-4	59.6	2	59	2	0.159	Further demonstrates the underfrequency trip timing of the ICS at other test magnitudes.
UFS-5	59.6	2	59	2	0.159	
UFS-6	59.6	5	58	2	0.106	
UFS-7	59.6	5	57	2	0.115	
UFS-8	59.6	5	57	2	0.107	

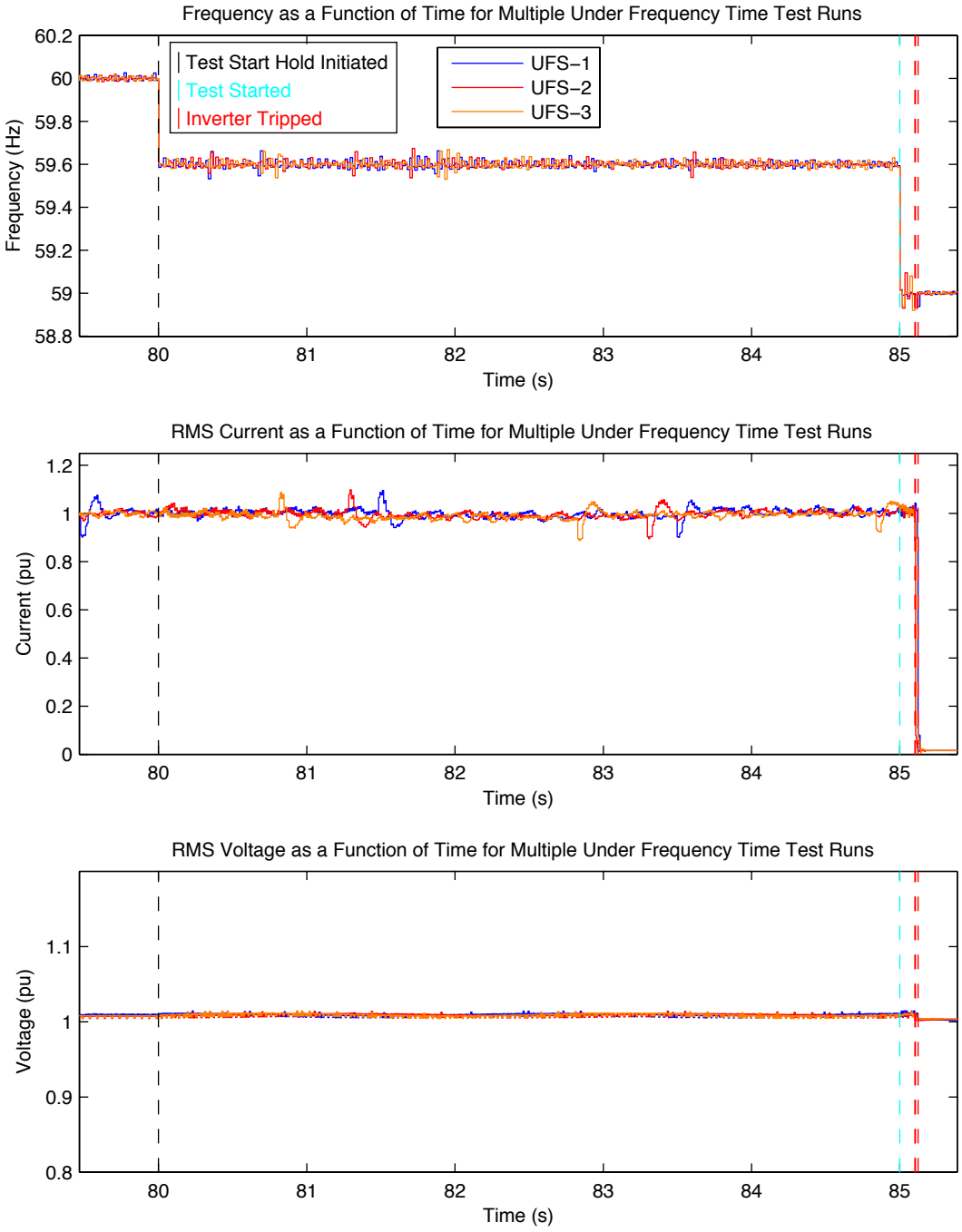

Figure 18: Multiple Underfrequency Time Test Runs

5.5.2 Magnitude

A selection of the underfrequency magnitude test results is given in Table 8. Figure 19 shows a plot of the first five of the test runs listed in Table 8 to demonstrate the ability of the GISE to execute tests over a range of different ramp rates and the variability in ICS output response for each test run. In examining Figure 19, one will notice that are some oscillatory deviations in the currents for each run. These deviations are due to the fact that the inverters under test had MPPT control enabled, but were drawing power from the fixed dc source, and the output current tended to hunt. This behavior was observed as normal for all inverters tested.

Table 8: Summary of Selected Underfrequency Magnitude Tests

Test Run #	PT Hold Magnitude P_b (Hz)	PT Hold Duration T_h (s)	Ramp Rate M_{ramp} (Hz/s)	Trip Magnitude (Hz)	Comments
UFR-1	59.6	5	-0.093	59.22	Demonstrates the underfrequency trip magnitude of the ICS for various ramp rates. Shown in Figure 19.
UFR-2	60.2	5	-0.045	59.23	
UFR-3	60.2	5	-0.045	59.24	
UFR-4	60.2	5	-0.02	59.22	
UFR-5	60.2	5	-0.015	59.25	
UFR-6	60.3	5	-0.015	59.24	Further demonstrates the underfrequency trip magnitude of the ICS for various ramp rates from a different starting value.
UFR-7	60.3	5	-0.025	59.24	

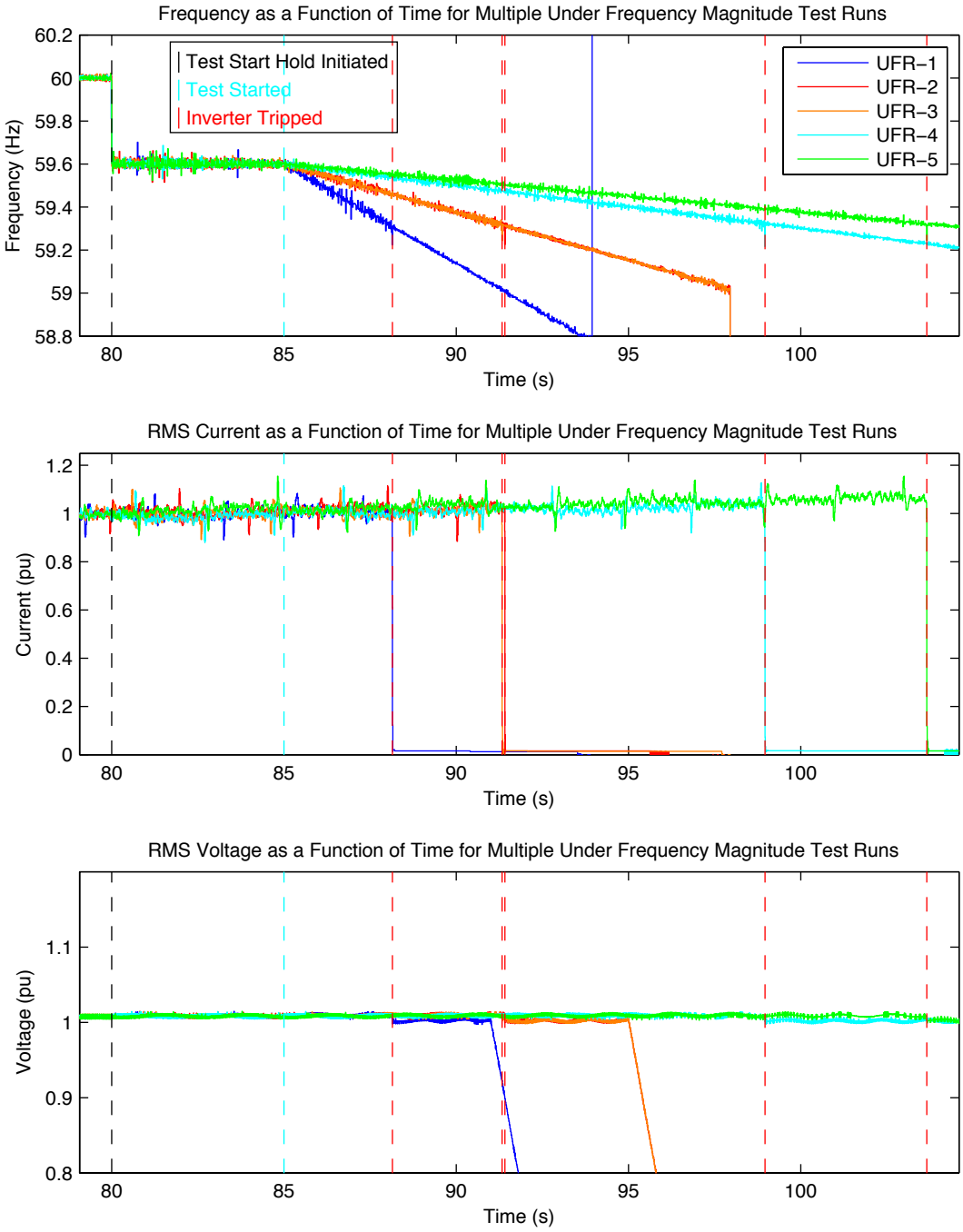

Figure 19: Multiple Underfrequency Magnitude Test Runs

5.6 Unintentional Islanding

As described in section 2.1.4 unintentional islanding testing is much different than the previous eight tests that were described. The test involves one more circuit element—the grid breaker—and requires more user intervention to precisely tune the resonant RLC load needed to complete the test. The test is also configured with a different strategy than the other over/undervoltage and frequency tests.

For the unintentional islanding test, the user only enters durations (values are automatically entered as nominal) for each of the three test intervals. In this case, the sum of the pre-test and test start hold durations becomes the amount of time before the grid breaker is automatically opened, by which time the resonant RLC load needs to have been already configured by the user. A summary of the test configurations and results for two selected unintentional islanding tests is given in Table 9.

The test report generated for test UI-1 is shown in Figure 20. This report format is identical to that used for the other over/undervoltage and frequency tests. For this particular test, the grid simulator was operated manually at 240 V nominal, the load configured, and then the RTS model run for a short duration to initiate the grid breaker opening and measurement of the ICS response. It can be observed from Figure 20 that the ICS under test employed a frequency perturbation unintentional islanding algorithm that perturbed the frequency up outside of the frequency trip limits once the simulated local EPS was no longer strongly regulating the frequency. The trip time for this test, measured as the duration between the time a breaker open condition, is communicated to the RTS by the grid breaker's auxiliary contact and the time the ICS current went to zero, was 0.189 seconds.

Table 9: Summary of Selected Unintentional Islanding Tests

Test Run #	Load Bank Configuration (set points)				Final Measured Grid Contribution (+ values indicate qty. is supplied)			
	Real Power (W)	Inductive Reactive Power (VAR)	Capacitive Reactive Power (VAR)	Effective Quality Factor	Current (A_{rms})	Real Power (W)	Reactive Power (VAR)	Trip Time (s)
UI-1	1937.5	2031.25	2187.5	1.088	0.4	9	96	0.189
UI-2	2437.5	2500	2812.5	1.088	0.45	39	97	0.169

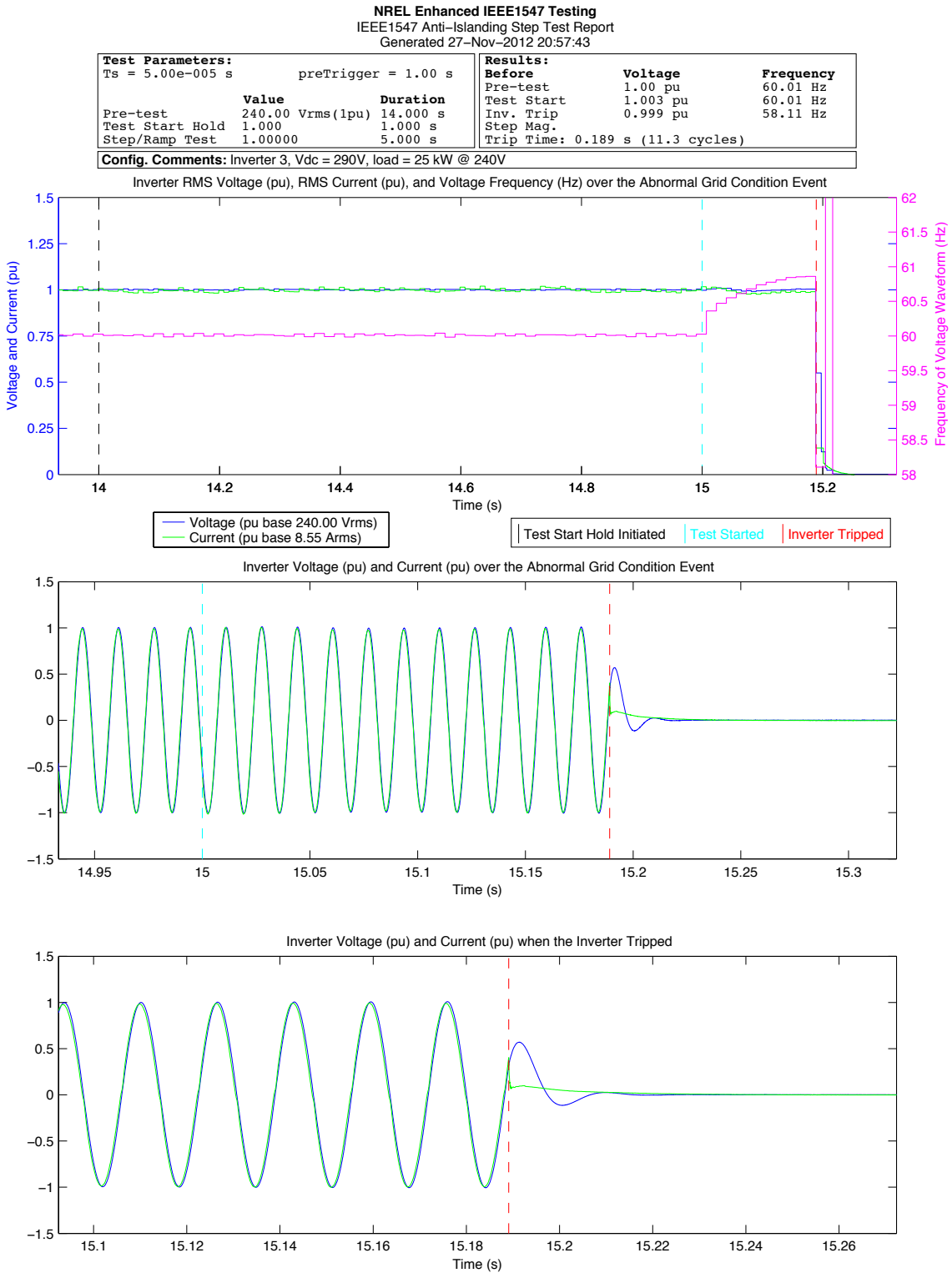

Figure 20: Summary Test Report for Unintentional Islanding Test UI-1

6 Conclusions and Continuing Work

This report describes and demonstrates a grid interconnection system evaluator that provides a method to vastly increase the efficiency of conducting IEEE Std 1547 and other grid interconnection conformance tests through the use of HIL simulation techniques, advanced analysis scripts, and a single user interface. Using the GISE's GUI, an operator can now configure, run, monitor, and view analyzed summary results for over/undervoltage and frequency and unintentional islanding IEEE Std 1547 grid conformance tests from a single interface. The accuracy, repeatability, and applicability to various ICS with different internal topologies of the GISE test execution were also demonstrated.

More than just automating a test procedure, this work adds further capability to NREL's advanced platform for development and evaluation of grid interconnection systems. This platform now allows for rapid development of ICS control algorithms using CHIL techniques, the ability to test the dc input characteristics of PV-based ICS's through the use of a PV simulator capable of simulating real-world dynamics using PHIL, and now evaluation of the ICS grid interconnection conformance. This platform offers a unique set of capabilities that will help develop and evaluate the next generation of ICS that will be prevalent in future advanced EPS architectures.

Upcoming work will involve further developing methods to leverage PHIL techniques to advance unintentional islanding, VRT, FRT, and volt/var control testing capabilities, and performing more realistic simulations of ICSs interfaced at various local EPS PCCs.

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