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20 GHz MONOLITHIC TRANSMIT MODULES

FINAL REPORT FOR THE PERIOD
November 30, 1981 through November 30, 1987

CONTRACT NO. NAS3-23247
NASA CR 182134

Prepared for

NASA-Lewis Research Center
Communications and Propulsion Section
21000 Brookpark Road
Cleveland, OH 44135

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15. Supplementary Notes

16. Abstract

The report presents the history of the development of a transmit module for the band 17.7 to 20.2 GHz. The transmit module was to monolithically combine, on one chip, five bits of phase shift, a buffer amplifier and a power amplifier to produce 200 mW to the antenna element.

The approach taken to accomplish this was to use the MESFET technology in its most fundamental version, i.e., the ion implanted device technology. The use of the MESFET both as a switch and a power amplifier device might normally call for multiple implant schedules in order to obtain the optimum pinch-off voltage in the devices for each application. In the case of this project a common pinch-off voltage was decided upon for each application thus simplifying the process.

The program was divided into four phases; the development of the individual switches and phase shifters, the power amplifiers and the first and second total integration phases. The first and second phases were accomplished without significant problems and established the fundamentals of the individual circuit components. Four mask sets, NASA-1, NASA-2, NASA-3 and NASA-3A, were eventually designed and utilized in this project.

The beginning of the total integration phases revealed the hitherto unencountered hazards of large microwave circuit integration. These problems were all surmountable and based in nature upon the processing aspects of the task rather than the design and/or test aspects of the task. The problems were solved and complete transmit modules from this program were awarded the prestigious IR-100 award for solid state design.

During the course of this program many valuable lessons were learned in the arena of transferring MMIC technology to production. That technology to produce the transmit module is now available in the Rockwell Pilot Line.

This NASA program culminated with the demonstration that the MESFET technology could meet the specifications and that the devices were producible. Yield and customer design considerations finally led to two separate chips for this project; one containing the power amplifiers and the other containing the complete five bit phase shifter. Program funding was insufficient to support the complete production, in the Pilot Line, of the final designs in the quantities originally specified. Limited quantities of the Variable Phase Shifter (VPS) and Power Amplifier (CGAP) chips, fabricated in the Rockwell R&D Laboratory (Science Center), will be delivered to the customer.

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1.0 INTRODUCTION

This report covers the period from Nov. 30, 1981 through Nov. 30, 1987 under NASA Contract No. NAS3-23247. The goal of this program was to develop a 20 GHz monolithic transmit module, which consisted of a 5-bit phase shifter, a buffer amplifier to overcome insertion loss of the phase shifter, and a power amplifier which provided 16 dB gain and 200 mW output power over the 17.7 to 20.2 GHz band. In addition, some simple control logic was included on-chip to reduce the required number of input bonding pads. The program was structured to provide the capability for a hybrid backup approach if insurmountable difficulties were encountered in fabricating a fully monolithic module.

Four mask sets were generated through the course of this program. The first was used to fabricate and test the phase shifter portion of the transmit module, while the second was dedicated to evaluation of the power amplifier. The third mask contained a complete monolithic transmit module that was somewhat larger than optimum to provide extensive diagnostic capabilities. The fourth mask was intended to contain a complete transmit module with an optimized layout.

From the program beginning to the evaluation of the early wafers from the third mask set, no major problems were perceived. But with the early measurement of the NASA-3 output, this changed and the following conditions were acknowledged.

1. Although amplifier gain was at design values, the power output level was not. A power level of 100 mW could regularly be obtained from the constant gain amplifier (CGA), but the goal of 200 mW was not attained.

2. Overall gain was low because of higher-than-designed for values of variable phase shifter (VPS) insertion loss. This insertion loss, thought to be due to the FET switches, was 1-1/2 dB higher per bit than expected.

3. The yields from the contact lithography-based process were lower than tolerable.

As a result of these facts, the plan for the fourth mask set was altered. The fourth mask set included changes in the amplifiers to boost power levels at output and

changes in the VPS circuits to lower losses. Further, the amplifier section and the VPS section were separated into two chips to alleviate the yield problem. The fourth mask set was labeled "NASA-3A" to reflect the changed nature of its goals and the postponement of the ultimate totally monolithic module. NASA-3A was procured in two formats. The first format, to be used immediately, was as a contact lithography mask set which included a "mix-and-match" provision to allow electron beam lithography (EBL) to be used for defining the submicron gate length. The second format, reflecting the ultimate processing method, was in a 10X projection system mask set which also provided for the use of EBL as the gate definition mode.

The processing accomplished with NASA-3A was done almost entirely in the contact mode. This processing was in two phases during the period of April 1984 up to December 1985. Initially, processing was performed under contract funds, but then some mask errors were discovered and were corrected. Finally, some processing development of the MMIC technology was carried out under Rockwell funding using the corrected NASA-3A mask set as an instrument, resulting in working amplifier modules and VPS modules.

The current status is influenced by the subsequent transfer of MESFET MMIC technology to Rockwell's GaAs foundry. There, the same MMIC technology has been developed to a high yield process. Rockwell has offered to conclude this contract by producing, at an overrun cost, the required deliverables in that facility. NASA declined the overrun and took the option of letting the work run to a conclusion with the production of this report and the delivery to NASA of representative samples of the amplifier chips and VPS chips from NASA-3A.

This report will provide details of the development effort over the subject period. As can be concluded from the above narrative, the period of intense activity on this contract was between January 1982 and December 1985. The intervening period to November 1987 has been a dormant period while decisions about proceeding were postponed as other options were being explored •

2.0 PHASE SHIFTERS

The first mask set developed under this contract was devoted to design and evaluation of the 5-bit phase shifter submodule, since this component was deemed most critical to the goals of the program. Each bit was fabricated as a separate circuit to evaluate phase shift accuracy and easily isolate any problems encountered. These were combined with a two-stage buffer amplifier, a single-stage test amplifier, the control logic submodule, and various test patterns to form the first mask set (NASA-1) for this program. Each of these circuits will be described in detail, followed by a description of their layouts and the entire NASA-1 mask set layout.

2.1   Design Approach

2.1.1   Phase Shifter

For each bit stage of the 5-bit phase shifter, a differential line length circuit is used. The circuit employs two single-pole, double-throw switches to switch between a short reference line and a longer line with the desired delay at the frequency of interest (see Fig. 1). The devices used for the switches are FETs biased with 0 V_{ds}. When the device gate is pinched off, the channel resistance becomes very large and the switch is effectively open. Conversely, when the gate potential is zero with respect to the other two terminals (or even slightly forward-biased), the channel resistance is low and the switch is on. At 20 GHz, there is an appreciable parasitic capacitance across the switch. This capacitance has no effect on the on state, but provides a significant leakage path in the off state. It is a well-known design technique to resonate out this capacitance by a parallel inductor realized as a high impedance transmission line; for the low or moderate power levels expected for the 20 GHz transmit module, this is not the best approach.

The electrical line length of a transmission line with an impedance of Z_0 Ω required to resonate a capacitance, C, at a frequency ω is given by:

$$\theta = \sin^{-1}(1/(wCZ_0)) \quad .$$

Therefore, for a given line impedance, only values of C greater than $1/(wZ_0)$ can be tuned out. The design rules established for the MMIC processing technology, consistent

BIT $\overline{\text{BIT}}$ BIT $\overline{\text{BIT}}$

SPDT
FET
SWITCH

L_1

L_2

SPDT
FET
SWITCH
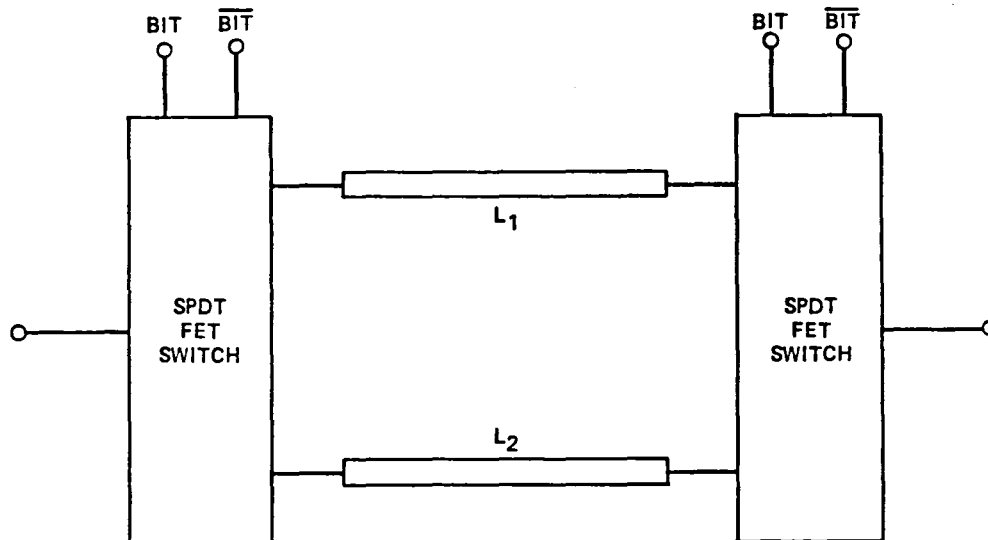
Fig. 1 One-bit phase shifter implemented with two passive transistor switches.

with high yield, produce a minimum transmission line width of 10 μm on the 125 μm thick GaAs substrate. The impedance of such a line is 93 Ω, the minimum C at 20 GHz is 0.086 pF. This translates into a minimum FET switch size, since FET capacitance is proportional to FET width for a fixed device geometry in the other dimensions. For the devices used in this program, the minimum FET width is approximately 125 μm at 20 GHz. At this limiting case, the required electrical line length is 90°, and it is as large (in terms of GaAs real estate) as the largest delay line in the 5-bit phase shifter. Note that four resonators would be required for each bit, since two FETs are required to form a single-pole, double-throw (SPDT) switch; thus, a total of 20 resonators with their large area would be required in the first bit phase shifter. Although the actual FET width used is somewhat larger than the 125 μm minimum, the resonators would still represent a chip area much larger than the switches and delay lines.

In lieu of the resonator method of controlling capacitive leakage, Rockwell has elected to short the small leakage signal with another switch to ground. This approach is reminiscent of PIN diode technology, but without the power consumption problems associated with PIN diodes. Note that the shunting switch is not placed a quarter wavelength

away as it is in conventional diode switches. Although such placement would improve performance significantly, the increased size would be unacceptable (a quarter-wave line at 20 GHz is approximately 1.26 mm long on the MMIC substrates). Even so, the improvement achieved with the second switch is substantial and allows acceptable performance over the band of interest. Size is significantly reduced since a very high gain buffer amplifier could be designed in the space that would be taken by the passive resonators or isolation lines between switches.

Figure 2 is a schematic of the SPDT switch used, and Fig. 3 is a layout plot of a switch as implemented on the NASA-1 mask set. Isolation resistors are required on all gate leads to prevent the capacitive leakage between the gate and switch terminals from degrading the isolation. This is the smallest possible circuit for providing isolation; it also has the highest yield. Although alternative structures would allow faster switching speeds, the resistor-isolated approach is adequate for this application, since the small gate capacitances can be charged with the moderate switching speeds required on this program.
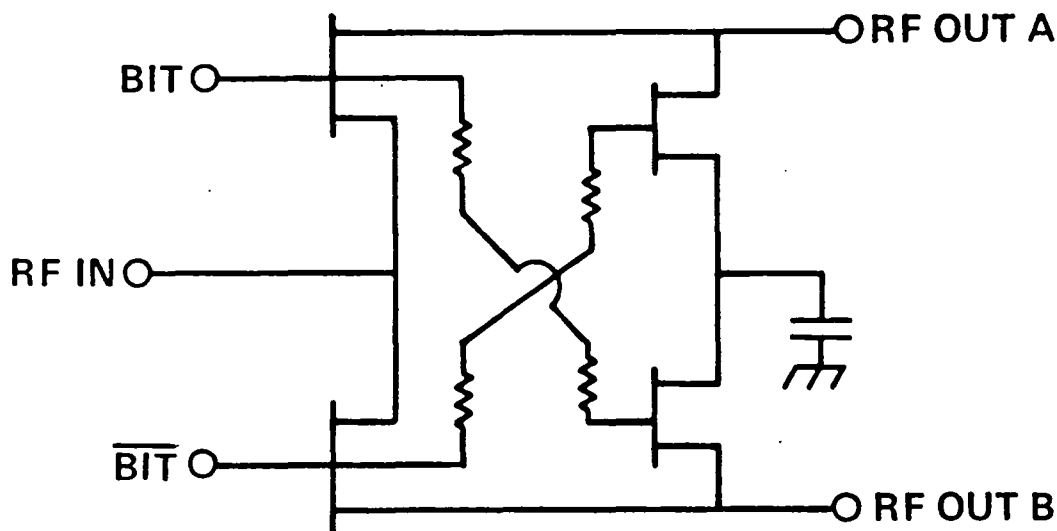
Fig. 2 Schematic of the SPDT switch used in 20 GHz phase shifters.
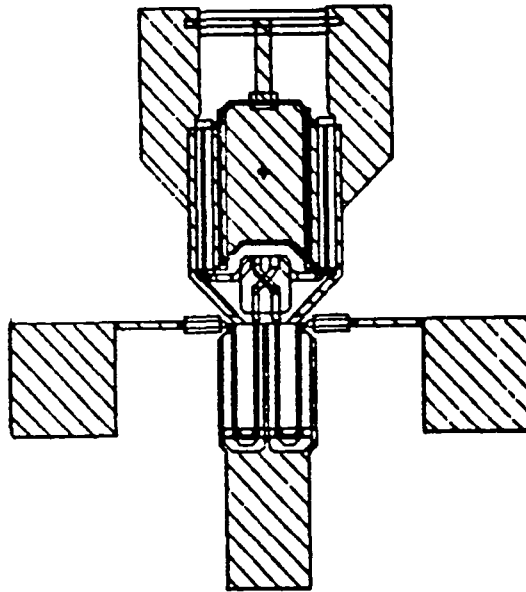
Fig. 3 Schematic of a SPDT switch as fabricated.

The phase shifter bits comprise two SPDT switches: a short reference delay line and the phase shift delay line, as shown in Fig. 1. Photographs of the five phase shifter bits implemented on the NASA-1 mask set are shown in Figs. 4a through 4e, which are the 180, 90, 45, 22.5 and 11.25° bits, respectively. Each bit is fabricated on a 1.5 x 1.5 mm chip, 125 µm thick. Input and output are 50 Ω lines which also serve as the bonding pads for the circuit. The shunting switches are internally cross-coupled to the main series switches such that they automatically turn on or off at the appropriate time. However, the four main control lines are brought to bonding pads separately to facilitate test and evaluation. In actual operation, the two lower gate bias lines are operated in parallel and the two upper bias lines are operated in parallel, resulting in two bias control lines for each bit. These two lines must run inverted from each other, i.e., when one set of switches is on, the other must be off. Because of this, it is necessary to include five inverter circuits on the final monolithic transmit module to obtain one control line per bit of phase shift.

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(a)
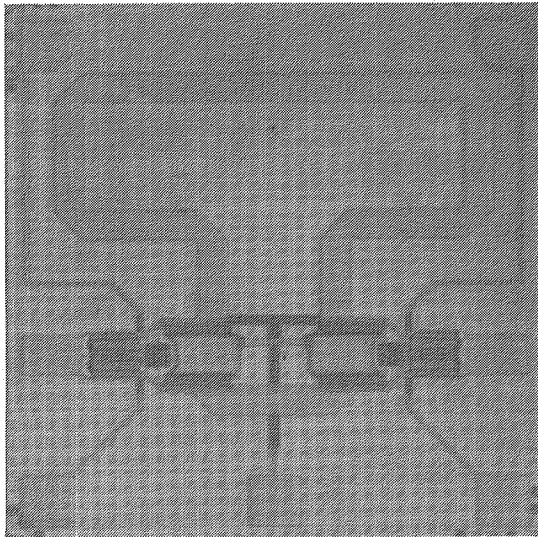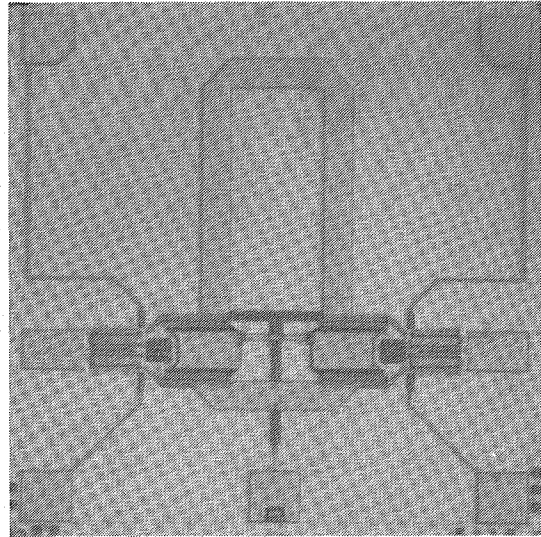
(b)

Fig. 4 Photographs of the NASA phase shifter bits: (a) 180°, (b) 90°.

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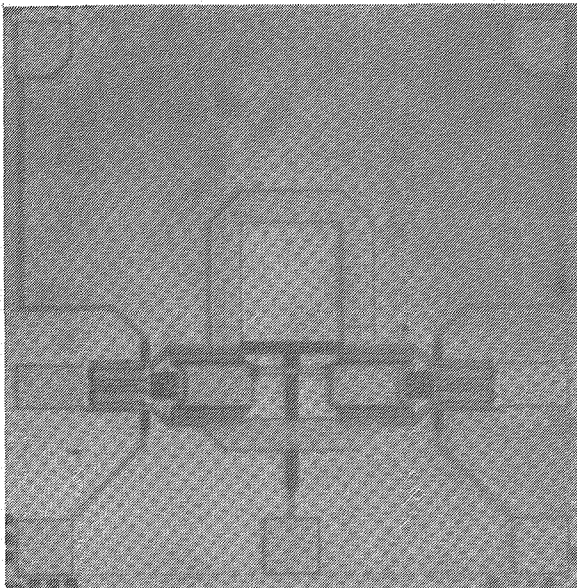
(c)
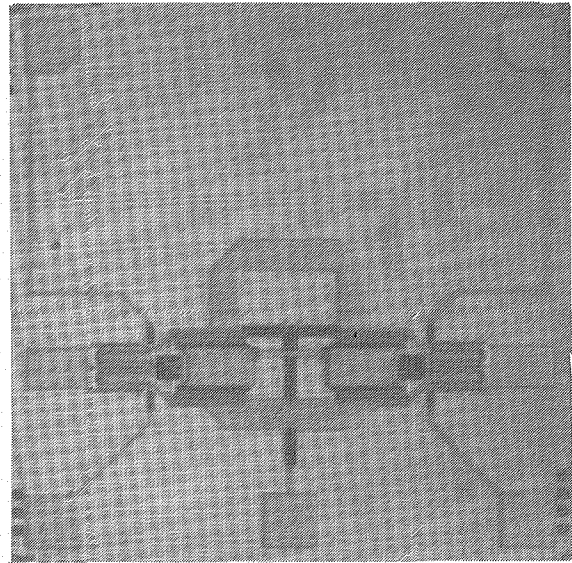
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(d)

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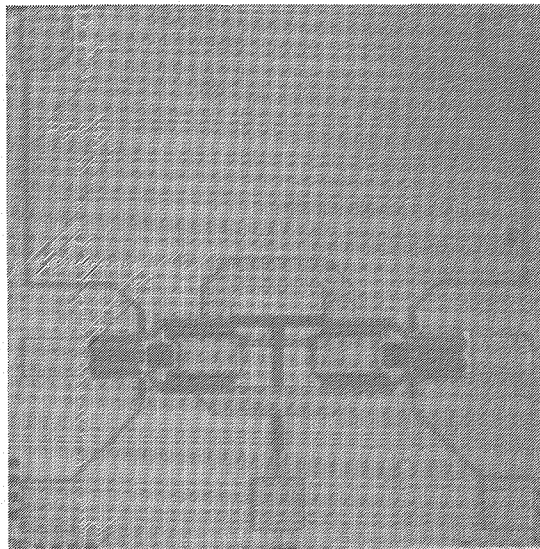
(e)

Fig. 4 (cont) , (c) 45°, (d) 22.5°, and (e) 11.5°.

2.1.2   Buffer Amplifiers

The 5-bit phase shifter was expected to have approximately 2 dB of loss per bit, or a total of 10 dB loss. A buffer amplifier was to be included to compensate this loss. Obtaining a flat gain of 10 dB across the 17.7 to 20.2 GHz band would be very difficult with a single-gain stage, but should be straightforward with a two-stage amplifier. Assuming 6 dB gain per stage was attainable, then a two-stage buffer amplifier could have 12 dB gain; the 2 dB margin could be used to compensate for unexpected extra losses in the phase shifter or lower than expected gain in the amplifier, in addition to the expected 10 dB loss in the phase shifter. Since the program represented the first attempt by Rockwell to design and fabricate 20 GHz circuits, it was determined that both a one- and a two-stage amplifier must be designed to aid in the diagnosis of any unexpected problems.

One of the technical problems in MMIC design, as well as in any IC design, was the limit of diagnostic techniques available to probe a fabricated circuit of a new design to the degree necessary for complete analysis. Computer-aided design techniques minimized these problems; however, diagnosis still relied heavily on built-in diagnostic capabilities. For this reason, the one-stage amplifier and the large test areas were extremely important in the early stages of the design effort. Later mask sets, which combined previously proven circuits, had less diagnostic capability at the circuit level while retaining process diagnostic elements.

Figure 5 is a schematic of the single-stage buffer amplifier designed for this program, and Fig. 6 is a photograph of the actual 1.5 x 1.5 mm chip. It consisted of a simple input and output matching network, on-chip bypass capacitors, and on-chip dc blocking capacitors which also served as part of the matching networks. Gate and drain bias were supplied through shorted stubs that were part of the reactive tuning rf networks. As described previously, quarter-wave lines could not be used for bias isolation, since their length would be excessive (almost as long as one edge of the amplifier chip). The source of the 200 μm wide center-fed FET was grounded by through-substrate via holes on each side; each of the 10 pF bypass capacitors was also grounded by a via hole. The discrete FET at the top of the circuit was used for test purposes only, and was not part of the single-stage amplifier circuit.

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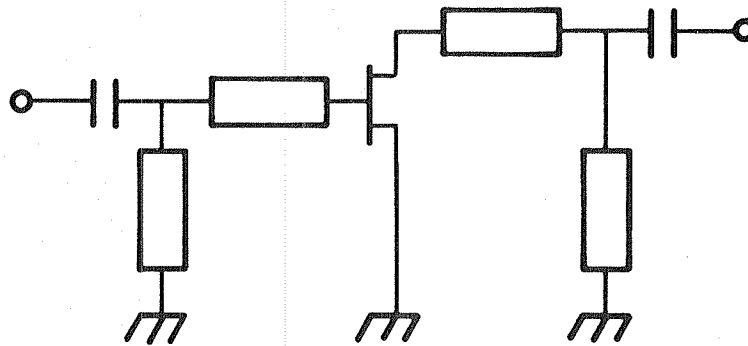
Fig. 5 Schematic of a single-stage buffer amplifier.

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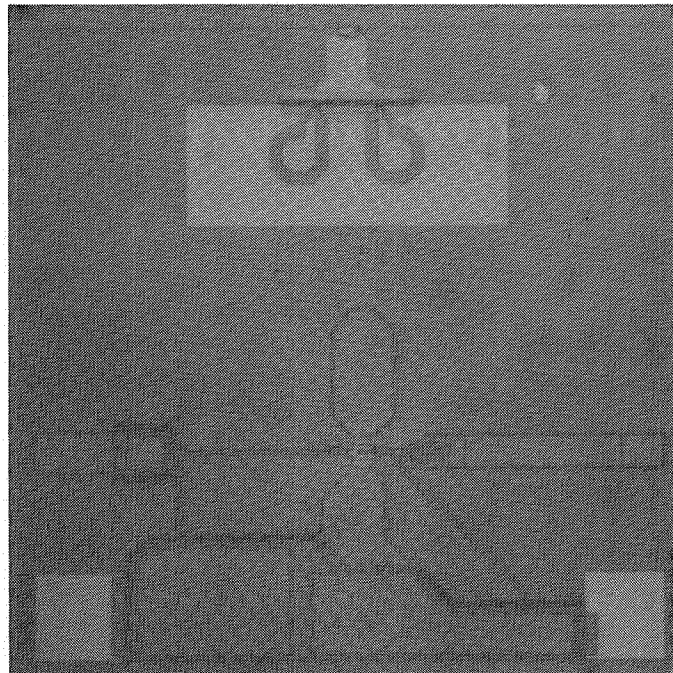
Fig. 6 Photograph of a single-stage buffer amplifier.

Predicted gain of the single-stage amplifier is shown in Fig. 7. The gain was optimized for a reasonable level at 20 GHz and no attempt was made to flatten the response across the operational band, since this amplifier was planned for diagnostics only. The layout was kept as clean as possible to minimize parasitic coupling and improve characterization of the passive components, to obtain as much information as possible about the FET and FET-circuit interactions.

More care was taken in the design of the two-stage buffer amplifier that was part of the full transmit module. Its purpose was to provide compensation for all losses in the phase shifter. Gain flatness was optimized at a level of 12 dB, and VSWRs compatible with the phase shifter were included in the optimization weighting function. Figure 8 is a schematic of the two-stage amplifier, which contains FETs identical to the one in the single-stage amplifier. The input matching network consists of a capacitive transformer (which had considerably smaller area than an inductive transformer or coupled lines), followed by a shorted stub to ground, a series-inductive line, and a shorted stub used for both tuning and bias insertion. The capacitive transformer did not provide

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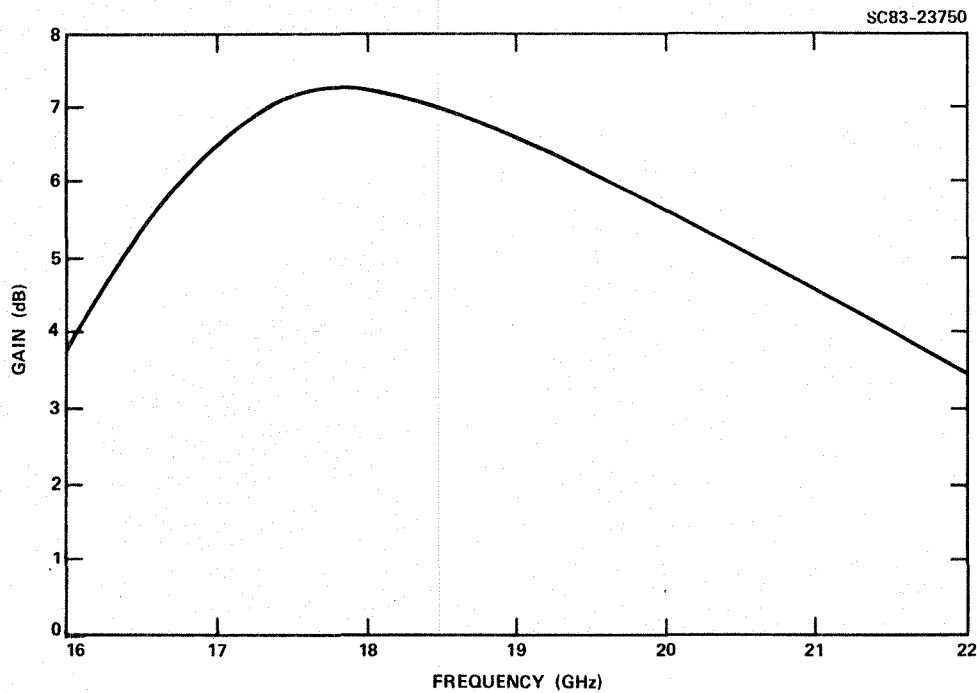
Fig. 7 Predicted gain of the single-stage buffer amplifier.

SC83-21388
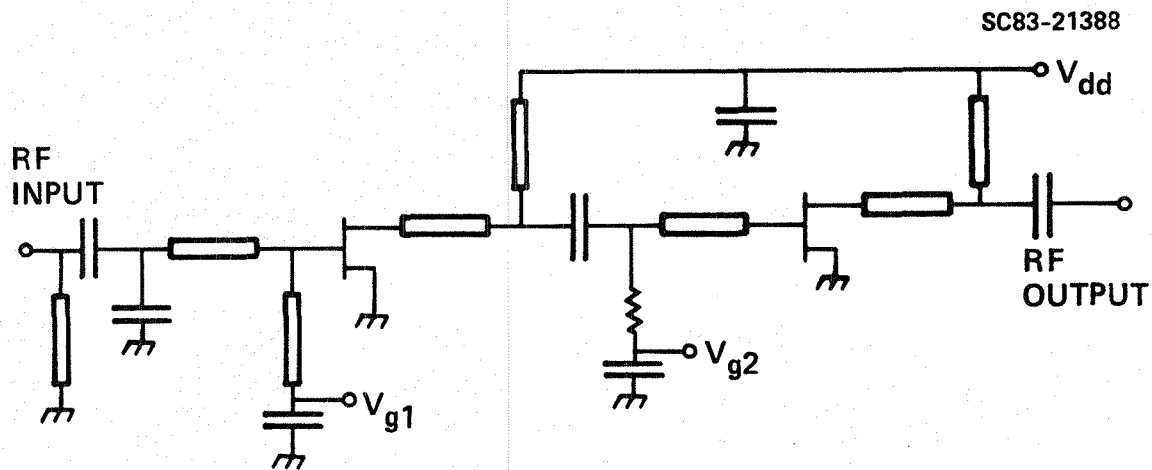
Fig. 8 Schematic of a two-stage buffer amplifier.

optimum bandwidth capability; however, the gain-bandwidth constraints were not severe
in this application and the benefit of the small GaAs area was desirable to increase
yield. The interstage matching network consisted of an inductive tuning line, a shorted
stub (which also provided drain bias to the first stage), and another inductive line. The
2 pF blocking capacitor provided a slight amount of tuning, but was primarily used to
allow the two FETs to operate from a common drain supply voltage. It was important to
minimize the number of bias points needed in the final monolithic transmit module.
Rather than use two shorted stubs for interstage biasing (which would result in a layout
area more than twice as large as the current configuration), a 10 KΩ resistor was used to
bias the gate of the second FET. This was acceptable since the FET did not operate at a
power level high enough for self-biasing to be a problem and no noise figure constraints
were placed on the design of the transmit module. Finally, the output network consisted
of a series-inductive line and a shorted stub for tuning and bias insertion to the second
FET. Again, the output capacitor provided mostly dc blocking and a small amount of rf
tuning. All inductive lines and shorted stubs were 10 μm wide, which corresponds to an
impedance of 93 Ω on the 125 μm thick GaAs substrate. The 10 μm linewidth was selected

as a compromise between wider lines with attendant higher yield and lower loss, and thinner lines with high impedance and reduced circuit size. The two drains were brought to a single bonding pad, but the gates were individually controlled in this initial design. Figure 9 shows a photograph of the two-stage amplifier chip, and Fig. 10 is a plot of the predicted gain for the two-stage amplifier. Measured performance is described in a subsequent section.

2.1.3   Control Logic

The control logic section of the monolithic transmit module consisted of five inverters which are TTL-compatible on the input. The original concept for the inverters was that they would be fully TTL-compatible at both the input and output from any signal source. That design goal was modified slightly to allow improved phase shifter performance without significantly increasing complexity of the control submodule. As a result, a constraint was imposed so that the drive signal was an open collector TTL logic.

SC44463
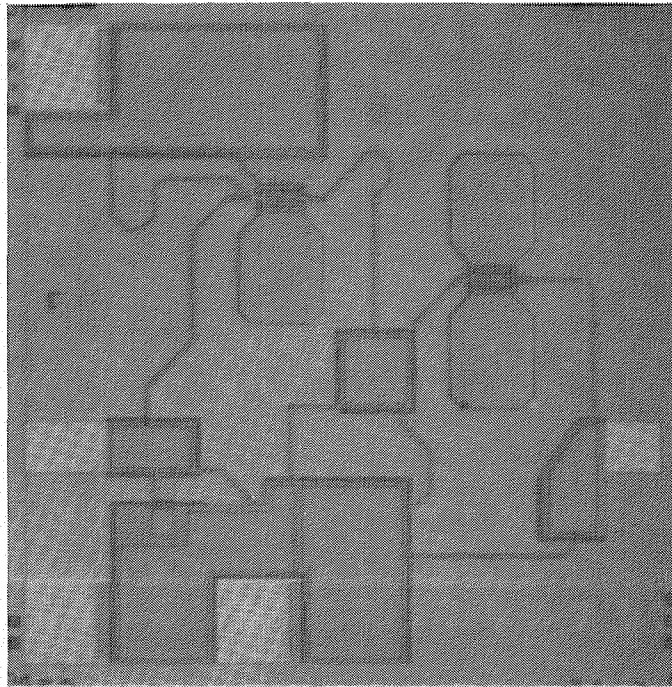
Fig. 9 Photograph of a two-stage buffer amplifier.

SC83-21384
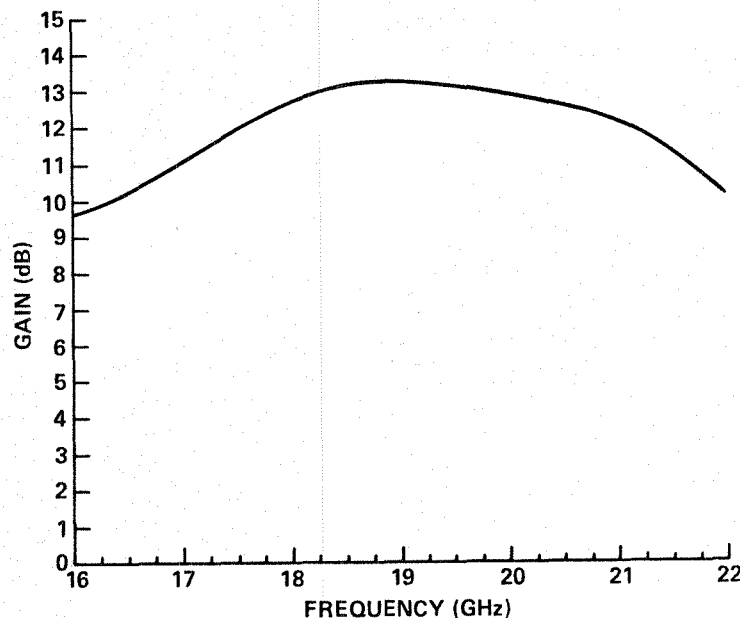
Fig. 10 Predicted gain of the two-stage buffer amplifier.

This allowed the inclusion on the GaAs chip of a pull-up to a higher than normal TTL level of 5 V, and avoided the possibility of insufficiently forward-biasing the rf switches in the phase shifter bits. This modification insured minimum rf insertion loss in the phase shifter string without other deleterious effects.

Figure 11 is a schematic of the TTL inverter as implemented on the NASA-1 mask set. A total of five inverters completed the entire control logic submodule of the transmit module. The input pull-up FET was 100 μm wide, while the pull-down at the end of the diode string was 10 μm wide, insuring that the inverting FET was slightly forward-biased when no signal was present (input voltage of 5 V). The large number of level shifting diodes was necessary since the nominal pinchoff voltage of the FETs used was 3 V. This allowed process compatibility with the other FETs on the mask set without the need for an additional ion implant step with its associated mask. (Normal digital switching FETs have a pinchoff voltage of 1.5 V or less; since the required amount of logic circuitry is small and the speed constraints are minimal, process development that would add an additional mask and process step was not considered for this program.) The relatively large number of diodes in this circuit considered were high yield, small area
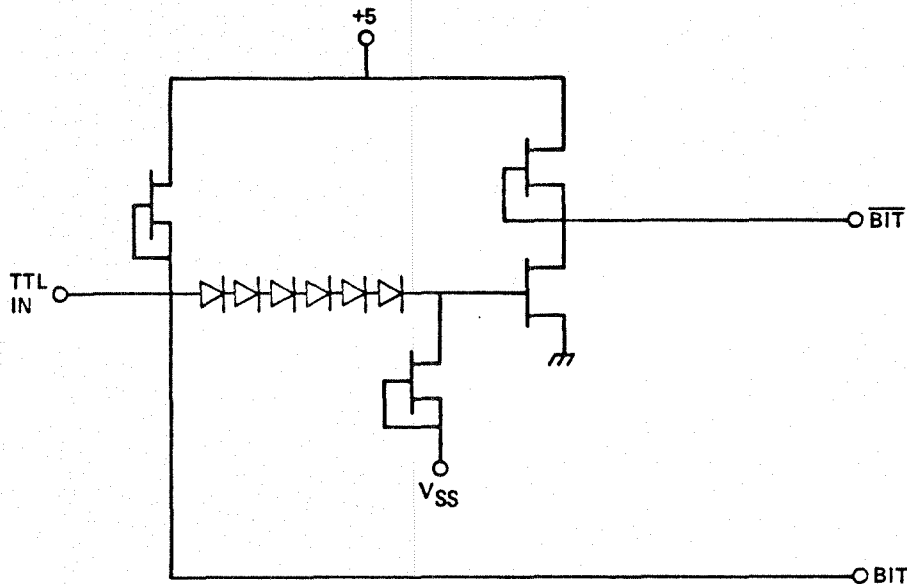
Fig. 11 Schematic of the TTL inverter as implemented on the NASA-1 mask set.

devices. At the output, a 10 μm wide pull-up and a 100 μm inverting FET completed the design. In the final design, the number of diodes were further increased and the pull-up voltage was correspondingly increased to improve phase shifter performance; however, this did not alter the design theory or performance at the input, providing open collector inputs with sufficient breakdown voltage were used.

Figure 12 is a photograph of the control logic section from the NASA-1 mask set. The structure on the right is the five inverters and some bypass capacitors on the bias line, while the two structures on the right are test structures consisting of the input and output portions of the inverter. These test structures have already proven quite valuable in diagnosing a minor problem in the fabrication of the inverters, as described in Sect. 2.3.4.

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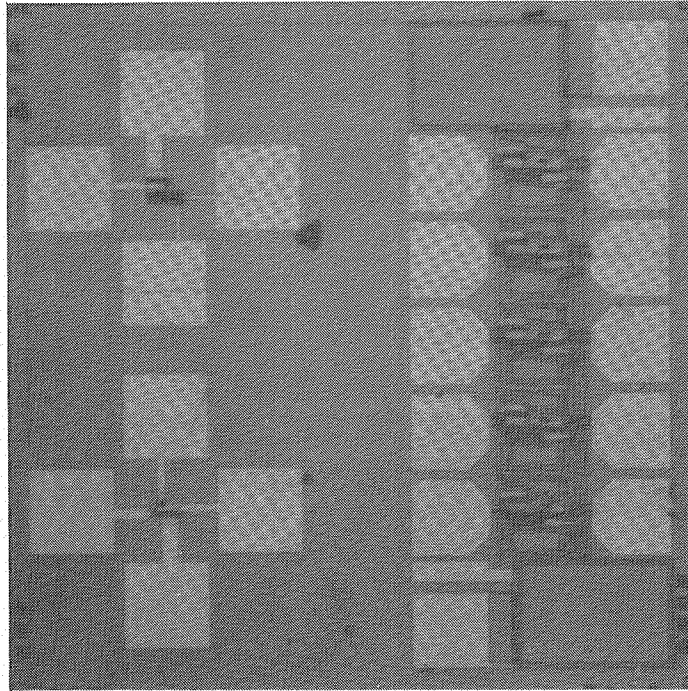
Fig. 12 Photograph of the control logic subsection and its associated test patterns.

2.1.4 Process Compatibility

Although the NASA-1 mask consisted of just the phase shifters, buffer amplifiers and control logic, it was essential that all processing steps be compatible with the power submodule as well, since they were to be totally integrated on the final monolithic transmit module. The use of high pinchoff voltage FETs in the control logic section for process compatibility was already mentioned, and resulted in the inclusion of a large number of high yield diodes to avoid process modifications. Similarly, a compromise was made in the design of the power amplifier; the standard pinchoff voltage was retained for the FETs in the power amplifier as well (power FETs usually have a pinchoff voltage of 5 V or more). The FETs were slightly wider as a result.

2.2 NASA-1 Mask Layout

The first mask set on this program (NASA-1) was fabricated as a 3 x 3 array of cells, with each cell having a size of 1.5 x 1.5 mm. Also included are 100 μm wide streets needed for saw kerfs when dicing so that the entire array was 4.8 x 4.8 mm. The array

was stepped to form the mask plates. Processing resulted in approximately 25 arrays on a 1 in. square GaAs wafer. The number increased to approximately 80 on a 2 in. round wafer. Figure 13 is a plot of the NASA-1 array.

The upper left-hand corner of the reticle contained the control logic and inverter (also shown in Fig. 12). The center of the top row is the single-stage buffer amplifier used for evaluation purposes only, and the right top corner contains the test pattern with the process monitor pattern in its lower right-hand corner. Also included in the test pattern are a SPDT switch (shown in more detail in Fig. 3), a discrete FET from the buffer amplifiers, some resistor and diode test devices, and a standard FET included on most Rockwell masks for device evaluation and further process monitoring. The left center circuit is the two-stage buffer amplifier expected to compensate for all losses in the 5-bit phase shifter (shown in more detail in Fig. 9). Finally, the remaining five circuits are the phase shifter bits previously shown in Fig. 4.
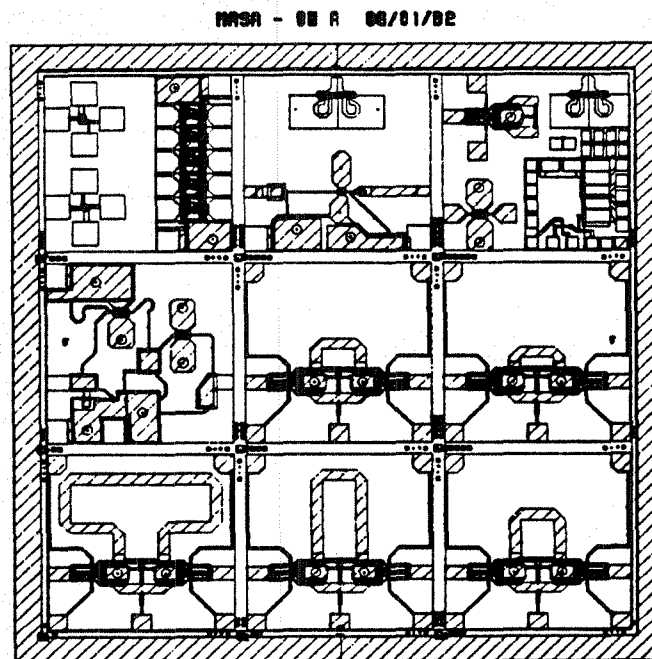
Fig. 13 Plot of a NASA-1 mask set reticle.

All alignment marks needed for both optical and electron beam alignment are included in the streets of the array, with the exception of the two "F" marks in the center left and right of the array. These were used for the in-house fabrication of the master reticle employed to make the mask set and are not part of the circuit. They are positioned so that they would have no effect on circuit performance.

2.3   Test Results

2.3.1   Measurement Techniques

The phase shifters and buffer amplifiers were measured in an rf test fixture on two different measurement setups. The first setup used was a swept power meter (from Wiltron) which can store a reference line, but cannot be used to do a full vector correction since phase information is not available. The second test set is a fully calibrated automatic network analyzer (from Hewlett-Packard) with an in-house calibration routine for the special test fixture used. A photograph of the test fixture used for all rf measurements is shown in Fig. 14. Many of the measurements presented here were made on the swept power measurement system in advance of readiness of the full vector correction test set. Making this set ready involved resolving several hardware and software malfunctions. These malfunctions were diagnosed and eliminated, so future measurements could be performed on the fully corrected test set, except for nonlinear measurements on the power amplifier stages for output power, spurious output, intermodulation and distortion.

2.3.2   Phase Shifter

The measured insertion loss of the 0°/90° section of the phase shifter in both phase states is shown in Fig. 15a, and the corresponding differential phase shift is shown in Fig. 15b. The center of the designed frequency band is at 18.9 GHz. The data shown in the figure could only be measured to 18 GHz. As the frequency is varied around that point, the circuit should have exhibited a linear change in phase shift, corresponding to the variation in delay line (electrical) length with frequency. The larger phase shift had longer delay lines, resulting in more phase slope in the phase vs frequency curves. Also note that the phase shifters worked over much larger bandwidths than required for this application, as noted in Fig. 16 as a 45° phase shifter measured at a later time, a direct
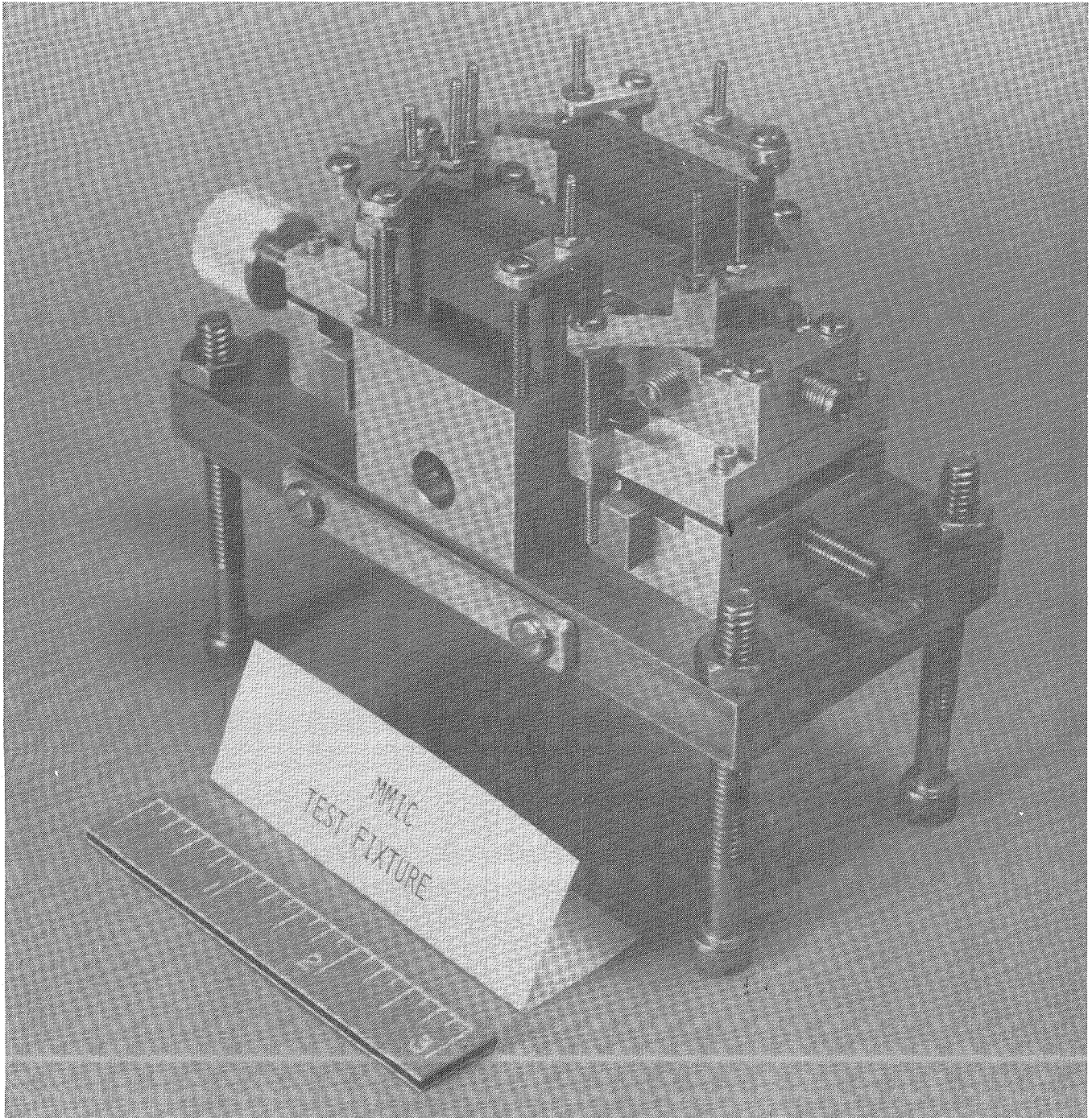
Fig. 14 Test fixturing used for test MMIC modules at frequencies up to 26 GHz.

SC5492.FR

(a)

0

+0.5000/DIV

dB

1

2

-4.000

+0.1800 10⁵

(b)

100.0

+10.00/DIV

DEGREES

0

+1000/DIV   +0.1800 10⁵

FREQUENCY (MHz)

INSERTION LOSS OF THE
90° PHASE SHIFTER,
STATE 1

DIFFERENTIAL PHASE
SHIFT OF THE
90° PHASE SHIFTER
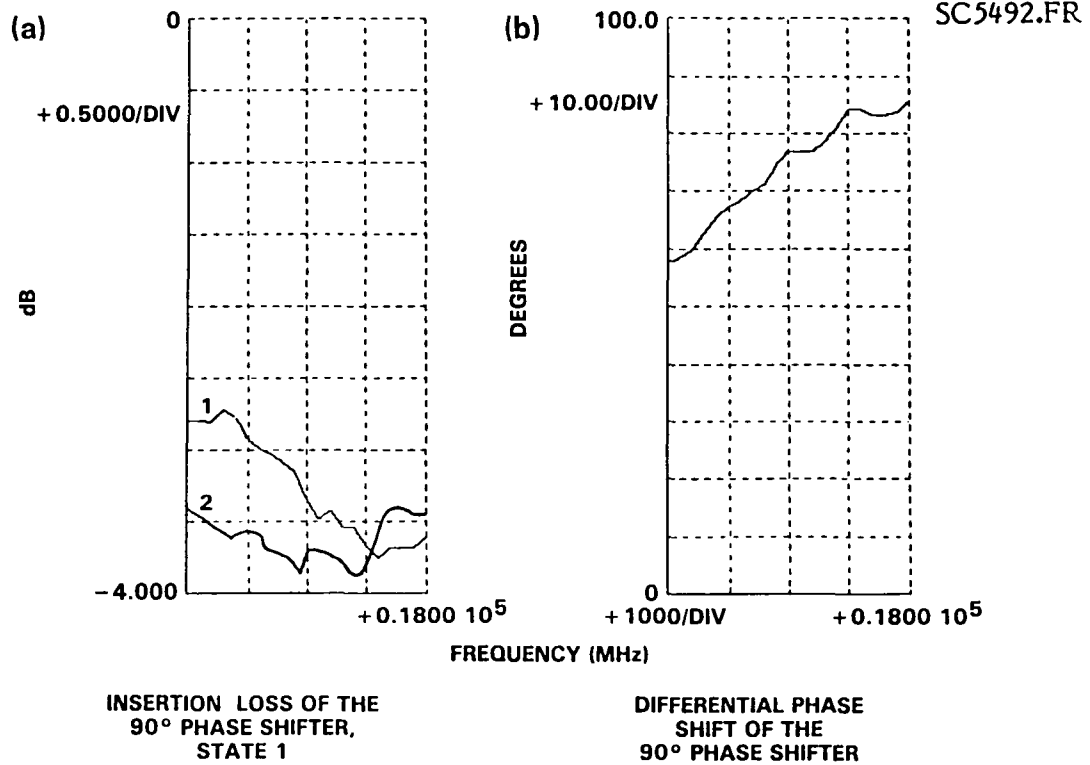
Fig. 15   (a) Insertion loss of the 90° phase shifter at frequencies 14 to 18 GHz and in
both states; (b) differential phase shift in the 90° phase shifter.

MRDC 38292

PHASE SHIFT (DEGREES) →

90°

45°

0

-45°

-90°

1
▽

△
2   (-47.13°)

14   15   16   17   18   19   20   21   22   23   24

FREQUENCY (GHz) →
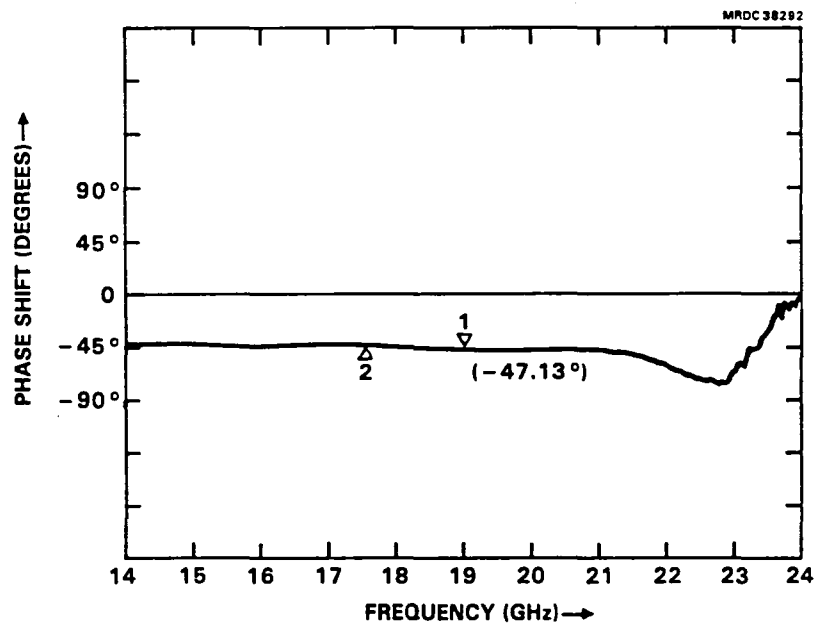
Fig. 16   Phase shift of a 45° phase shifter over 14 to 24 GHz.

result of the absence of resonant inductors in the switches. This was expected to greatly increase the rf yield, since slight variations in switch capacitance do not shift the operational frequency away from the desired frequency range as they would for a resonant structure. The only effect expected was a slight altering of the insertion loss. The insertion loss noted in Fig. 15, however, is larger than expected, a common trait in these phase shifters.

2.3.3   Buffer Amplifiers

The single- and two-stage buffer amplifiers were measured on the swept power test set, and the results are shown in Figs. 17 and 18, respectively. Both of these amplifiers, as well as the power amplifiers described in Sect. 3.0, exhibited a strong tendency to oscillate at very low frequencies (in the hundreds of megahertz range). This was caused by the high-performance FETs used, which often yielded potential instability at low frequencies and the simple matching networks used. It was further aggrevated by a waveguide interface to the test fixture, which presented an open circuit to the amplifiers at low frequencies. The oscillations were eliminated by addition of a simple feedback resistor outside the 10 pF on-chip bypass capacitors, as shown in Fig. 19. This resistor had no effect on in-band performance, since it was outside the bias circuitry; however, it
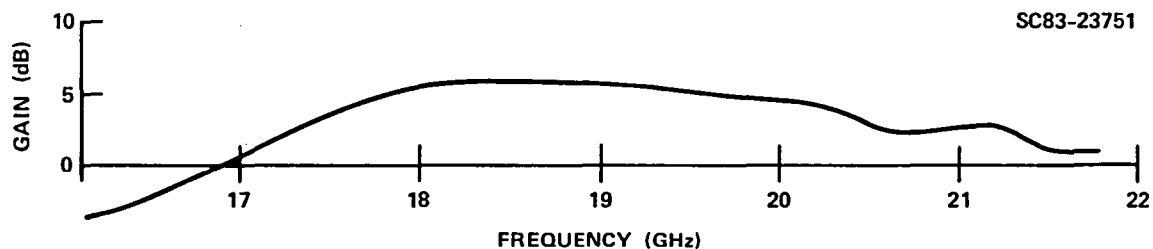
Fig. 17 Measured gain of the single-stage buffer amplifier.

21386
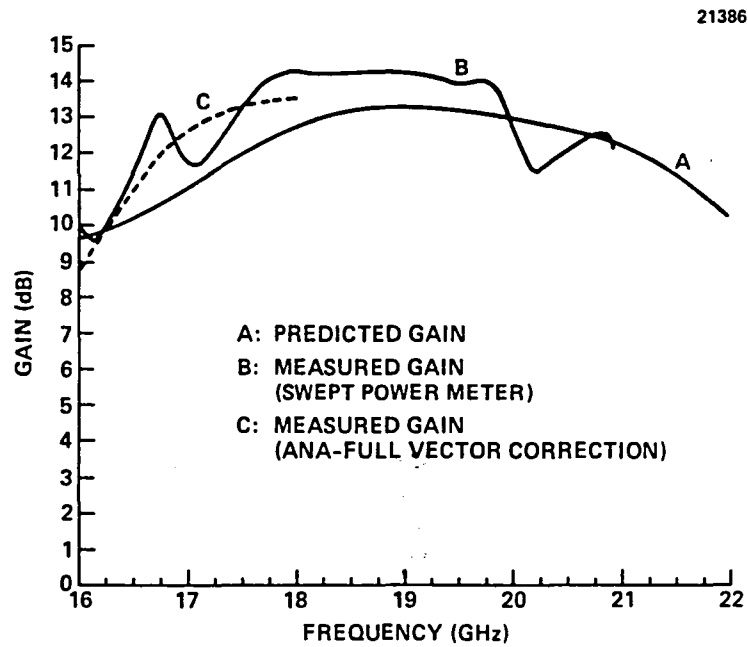
Fig. 18 Measured gain of the two-stage buffer amplifier.

SC83-23748
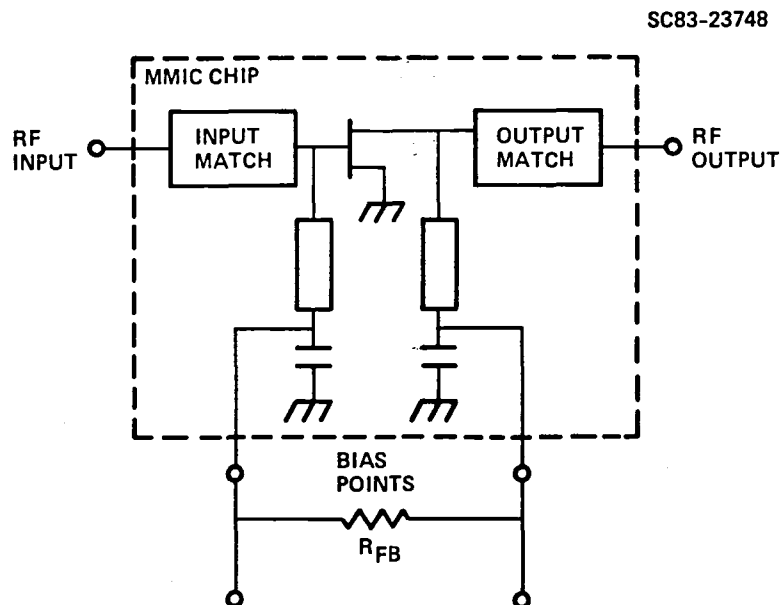
Fig. 19 Schematic of the external stabilization for the buffer amplifiers.

was directly connected from the drain to the gate at the oscillation frequency. Selection of a sufficiently small resistor (several hundred ohms) resulted in a reduction of low-frequency gain to the point that oscillations were eliminated. These resistors, added externally for the present circuits, were to be integrated into the amplifiers in the next design iteration, described in Sect. 4.0.

As shown in Fig. 17, the single-stage amplifier performed as expected. Detailed evaluation of this amplifier was not undertaken, since its main purpose was for diagnosis of any problems encountered in the two-stage design. It was useful in tracking down the oscillation problems described above; however, after this was accomplished, the evaluation was confined to the operation of the two-stage design.

The two-stage amplifier also operated as expected, as shown in Fig. 18. The figure includes the predicted gain of the amplifier, a swept power meter test, and a measurement up to 18 GHz on a standard 18 GHz network analyzer with full vector correction (the calibration software was modified to accept calibration standards developed for the MMIC test fixture). This comparison indicates the necessity of using the vector correction software for accurate measurements. The large ripples encountered on the swept power test set were due to fixture/circuit/test set VSWR interactions, which could not be eliminated by simple subtraction of magnitudes. However, the general gain level and shape of the curve are correct; therefore, the information is still valid, provided the limitations of the measurement technique are understood and taken into account.

2.3.4   Control Logic

During measurements, the TTL-compatible inverters needed for control of the phase shifters failed to change state when the input was switched between TTL 0 and 1 levels. The devices failed even when larger voltage swings were used to drive the input. With the aid of the expanded test cells on the NASA-1 mask and the discrete diodes in the test pattern, the problem was traced to high series resistance in the level shifting diodes. Figure 20 is an I-V curve of a test diode exhibiting the problem. The curve shows that although the diode operates correctly at low current levels, it rapidly approaches a saturation current typical of a saturated resistor. The current inverter configuration is inoperable with such a diode.
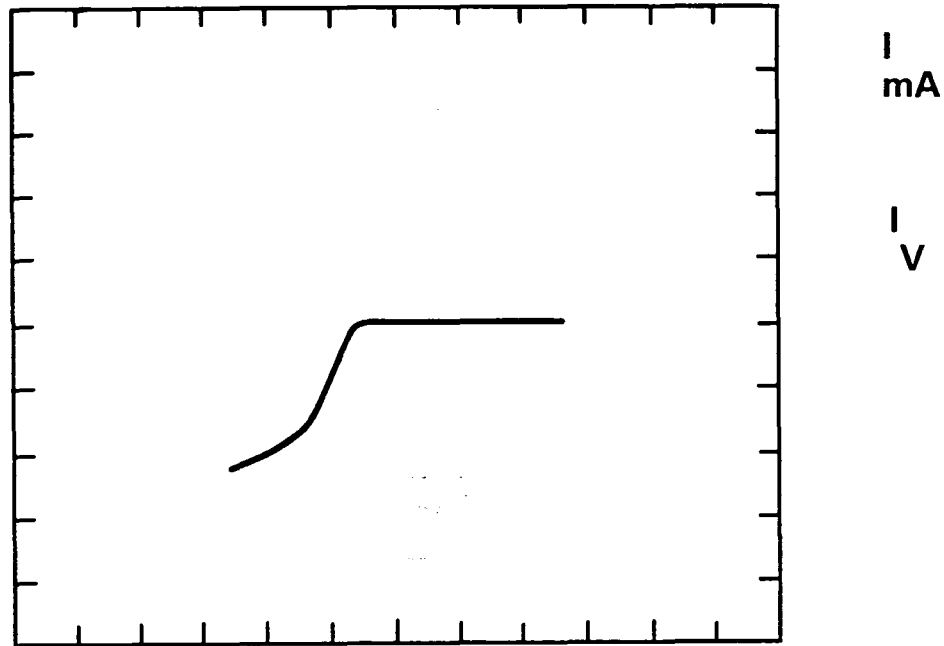
Fig. 20   I-V curve of TTL inverter diode showing the excessive series resistance due to overetch.

When the layout was made for the circuit, it was felt that the diode yield could be increased by increasing the diode metal finger width to 1 μm instead of the 0.7 μm used in the gates of the active devices (i.e., FETs). Since the diode fingers were placed on the same metal level as the FET gates, the gate recess etch was applied to the diode fingers, resulting in a recess for the diode also. For small fingers, this would only increase the diode resistance slightly; however, the larger finger width resulted in a faster etch rate and excessive resistance, as shown in Fig. 21. This problem was easily corrected on the next iteration of the circuit by putting the diode finger on the first metal layer (which was fabricated with the same metallization system performance of the junction was the same). The first metal layer was applied without any etch.

SCB2-19357
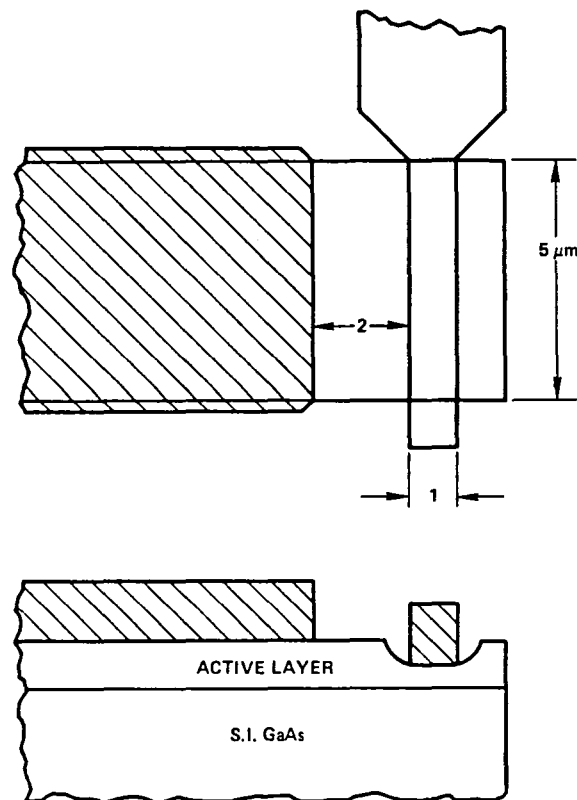
Fig. 21   Undercutting of the diode active layer that results in high series resistance. This problem has been cured.

2.3.5   Mask Modifications

Many of the mask modifications required to improve performance and correct problems discovered during evaluation have already been discussed in previous sections. In summary, these changes were to place the diode finger on the first metallization layer instead of the gate layer, and to add stabilization resistors on all amplifiers. Not previously mentioned but equally important are several modifications to improve circuit yield and/or performance.

A major performance-limiting factor for the phase shifters was a digitization error discovered which greatly increased the resistance of the 10 KΩ isolation resistors. The protective polyimide layer was exactly aligned with the resistive implant. Because a slight unavoidable misalignment left part of the resistor unprotected during processing, this often resulted in a resistance in the megohms instead of kilohms, which adversely

affected switching speed. This was not a primary concern for the present measurements; however, it also had a severe effect on required bias voltages due to gate junction leakage currents. In testing a single bit of the phase shifter, this was overcome (except for a possible increase in insertion loss); however, it became unmanageable for a cascade of phase shifters since the dc voltage on the rf signal lines was not sufficiently stable as the control voltages were altered. The problem was easily corrected by overlapping the ohmic contacts with a polyimide layer. The bias resistor on the two-stage buffer amplifier had a similar problem which was also corrected. It had a less significant effect for testing, since it only served to reduce the rf yield of the circuit when the gate junction leakage currents were somewhat high.

Another problem encountered in the measurement of the phase shifters was a 5 μm wide top layer metal line which was used to reduce rf losses in the circuit. This line was too thin and often peeled off, thereby shorting to other parts of the circuit. The problem was easily corrected on future masks by slight alterations in the layout, which leaves room for a 10 μm linewidth. A tolerancing problem at the gate feeders for the phase shifters was also corrected on the next iteration of the design (NASA-3).

3.0 POWER AMPLIFIERS

The second mask set designed under this program was used to fabricate and evaluate the power submodule of the 20 GHz monolithic transmit module. Included on the mask were single-stage, two-stage and full three-stage power amplifiers. The three-stage amplifier supplied an output power of greater than 100 mW with 16 dB of associated gain.

3.1   Design Approach

Assuming a gain of 6 dB per stage, except possibly for the output stage, it was determined that three stages of amplification were required to obtain a minimum of 16 dB gain across the 17.7 to 20.2 GHz band. A conservative output power density of 250 mW per millimeter of gate periphery was selected to compensate for the fact that low pinchoff voltage FETs ($\sim$ 3 V) would be used for maximum compatibility with the other circuits on the monolithic transmit module. Therefore, the output device had a width of 800 μm for 200 mW output power. Selection of a 400 μm wide driver and 200 μm wide predriver insured that only the output stage would contribute to the gain compression of the overall amplifier.

To maintain the schedule, the power submodule was designed as a three-stage amplifier without first designing and evaluating the stages as individual circuits. Following the same philosophy as was used in the design of the buffer amplifier for the phase shifter, single-stage and both possible two-stage versions were also designed and placed on the NASA-2 mask set. This allowed diagnostics of the final circuit without delaying the program if the full three-stage design was unsuccessful. Discrete power FETs were also included for further evaluation, independent of circuit properties. Since all six amplifiers were matched to 50 Ω, they were easily evaluated and possibly useful in their own right for hybrid versions of the monolithic transmit module or for other applications.

3.1.1   Single-Stage Amplifiers

Design began with the development of a small signal FET model for each finger of the actual FET. The finger length was a compromise between reduction of

feeder parasitic elements (which required long fingers) and small phase shift and loss along the gate width (which required short fingers). A compromise unit finger width of 100 μm was selected in both the small signal and power amplifier FETs. The gate itself was an 0.7 μm long T-bar structure for low resistance and high performance at 20 GHz while maintaining reasonable yield. A complete small signal FET model was then constructed for each FET in the amplifier from the intrinsic gate finger model and passive parasitic interconnection elements. The power FETs were structured as π-gate devices to eliminate possible output power reductions due to gate misalignment, while the small signal FETs used in the buffer amplifiers were more traditional structures to slightly improve source grounding and possibly improve gain performance.

Predicted gain for the three single-stage amplifiers is shown in Fig. 22. These amplifiers were mainly intended for diagnosis, so only moderate attempts were made to flatten the gain across the band of interest. Instead, a reasonable gain level was preferred along with as clean a layout as possible for accurate modeling of the passive components.

23486
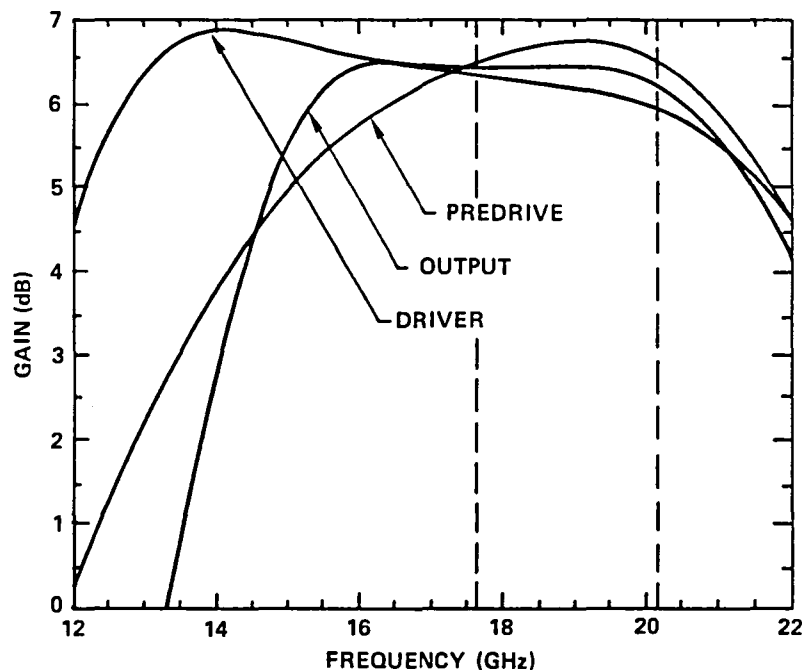
Fig. 22 The predicted gains of the three stages of the final power amplifier.

Figure 23 shows photographs of the three single-stage power amplifiers. Parts a-c show the predriver, driver and output stage, respectively. Each chip is 1.5 mm square and 125 μm thick. Note the symmetric nature of the output stage resulting from operation of two 100 mW amplifiers (each matched to 100 Ω) in parallel. This technique simplified the design of the output matching network for power, since the optimum load impedance for a 400 μm wide FET with the present device parameters had a real part very close to 100 Ω. This means the matching network consisted simply of a shorted stub to ground to tune out the parasitic capacitance of the FET. The series lines were then 100 Ω transmission lines which were not sensitive elements, since they were just used to reach the edge of the chip. The 100 Ω lines also used much less GaAs real estate than a 50 Ω line would need.

SC44472

SC44464

(a)
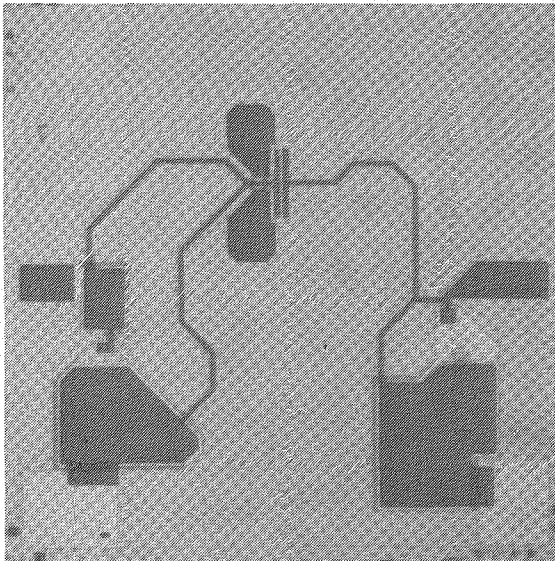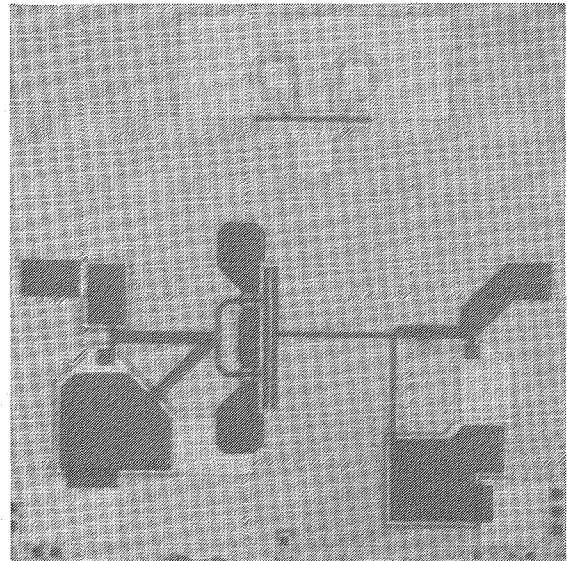
(b)

Fig. 23   Photographs of the three separate stages in single form: (a) the first stage (predrive); (b) the driver stage.

SC44473
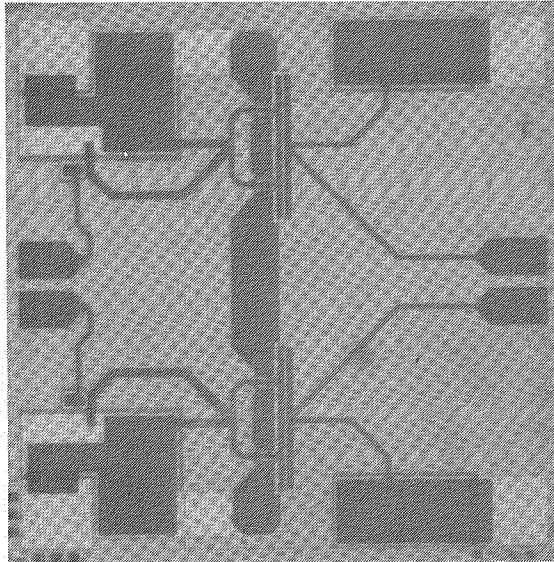
Fig. 23 (cont) (c) the output stage.

3.1.2   Two-Stage Amplifiers

The two-stage power amplifiers were designed to evaluate the interstage matching networks between the predriver and driver, and between the driver and output stage. Interstage matching was similar to that in the two-stage buffer amplifier, except that both drain and gate bias were inserted through shorted stubs. Due to the larger FETs used in the power amplifier, the stubs were shorter and did not cause as many layout problems as would have in the case of the buffer amplifier. Nonetheless, the two-stage amplifiers were packed very tightly on the 1.5 x 1.5 mm chips. Size constraints on the entire NASA-2 reticle precluded the use of double size chips for these amplifiers as was done for the three-stage amplifier described in Sect. 3.1.3.

Figure 24 contains a schematic of the two-stage dual driver. Figure 25a and 25b are photographs of the actual amplifier chips, which are both 125 μm thick for compatibility with the other NASA circuits. This thickness was expected to provide sufficient heatsink capability for the moderate power circuits, especially considering

18191
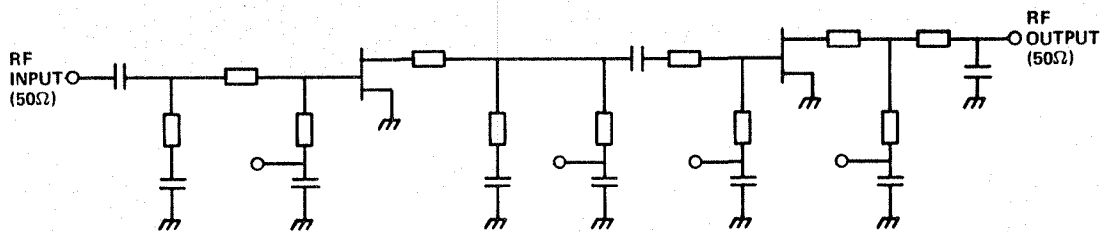
Fig. 24 Schematic of the two-stage driver (stages 1 and 2).

the distributed nature of the active devices as a result of the π-gate FET structure. Predicted performance is shown in Fig. 26. Great care was taken to model the parasitic elements, which was more difficult than usual on these compact designs. As a result, the amplifier designs tested both interstage matching networks, which critically depended on accurate modeling of the active devices, and modeling of the passive coupling due to close spacing of the components.

3.1.3   Three-Stage Power Submodule

A schematic of the three-stage power submodule is shown in Fig. 27. This amplifier was expected to perform as required in the final monolithic transmit module design. As in the other amplifiers, bias was applied separately to each FET. However, interstage blocking capacitors were included which allowed all FETs to be biased from a common power supply in the final design. It proved impossible to fit this amplifier on a 1.5 x 1.5 mm chip; therefore, it was placed on a 1.5 x 3.1 mm chip to simplify sawing of the NASA-2 circuits for evaluation (the extra 100 μm was due to the saw streets included between cells). With this much area allocated, the layout became very clean.

SC44475

SC44465

(a)
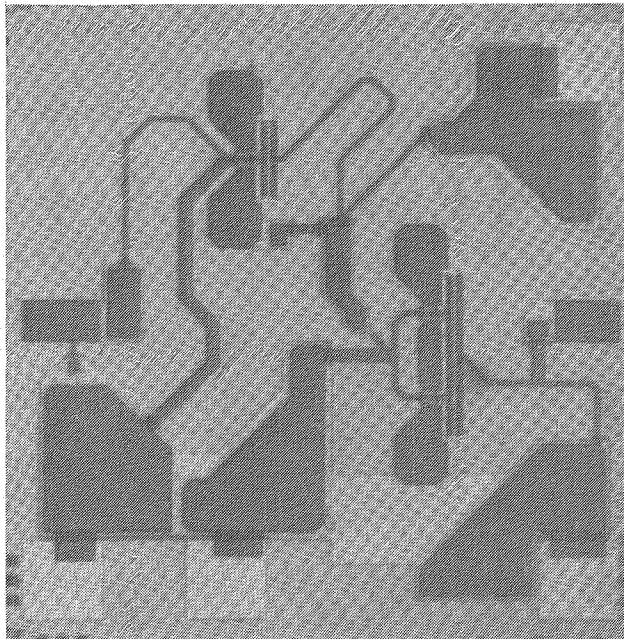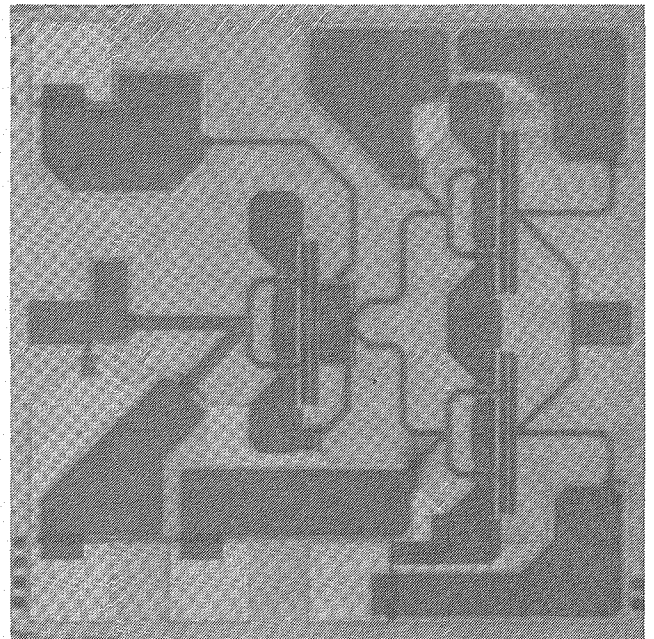
(b)

Fig. 25   (a) Photograph of the monolithic combination of stages 1 and 2; (b) photograph
of the monolithic combination of stages 2 and 3.

23485
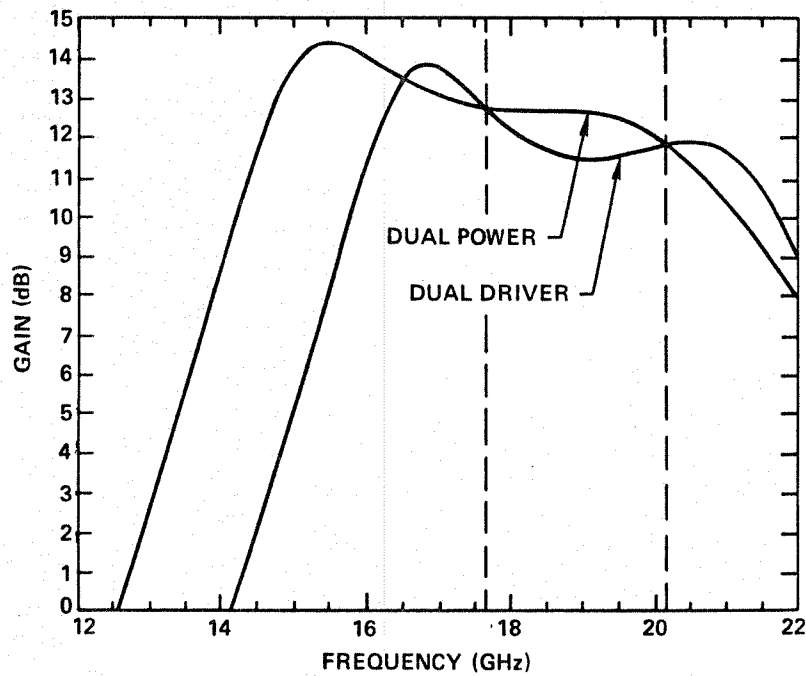
Fig. 26 Predicted gain of the two-stage driver combinations of Fig. 25.

18282
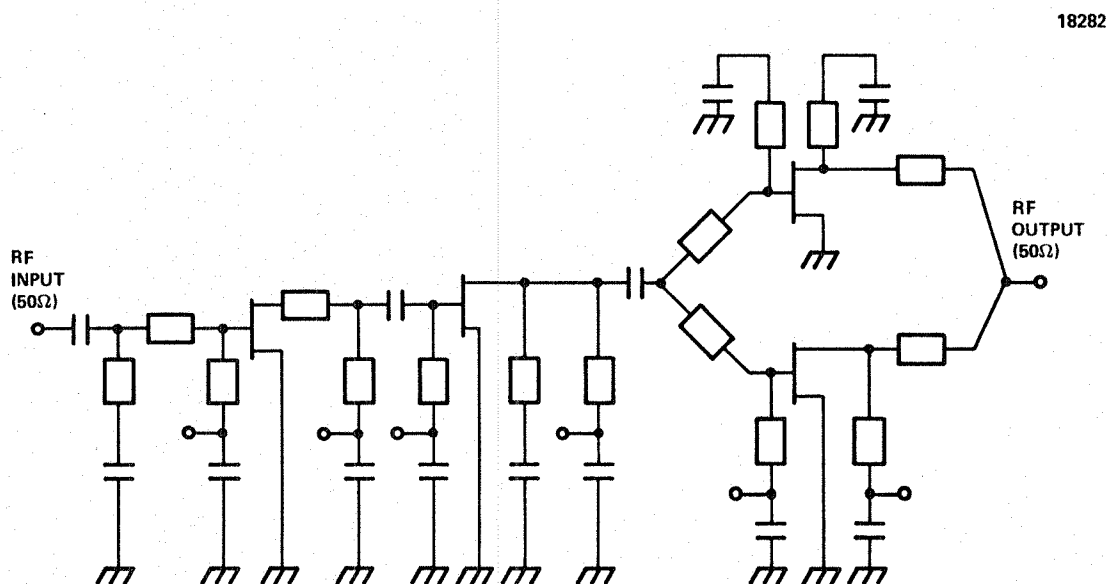
Fig. 27 Schematic of the three-stage combination of all the power stages.

Predicted gain of the three-stage power submodule is shown in Fig. 28. Gain was flat and slightly above the required level of 16 dB, and extended well beyond the band edges. The wider-than-required frequency range was expected to significantly improve rf yield, since slight shifts in the operating band did not move the performance out of specification. In addition, the low-end gain did not have a large gain peak, which could lead to oscillations in the actual amplifier at a frequency which would be difficult to control and suppress. Figure 29 shows the layout of the three-stage amplifier on the 1.5 x 3.1 chip.

3.2   NASA-2 Mask Layout

The NASA-2 layout was organized as follows. The upper left-hand corner is the test pattern which include the ever-present process monitor, some discrete power FETs (200 and 400 μm wide), and assorted passive and active devices from the other circuits on the mask. The remaining two cells on the top row are merged and form the three-stage power submodule. The left center circuit is a test pattern devoted to further evaluation of the switches used in the NASA-1 phase shifters, and the next two
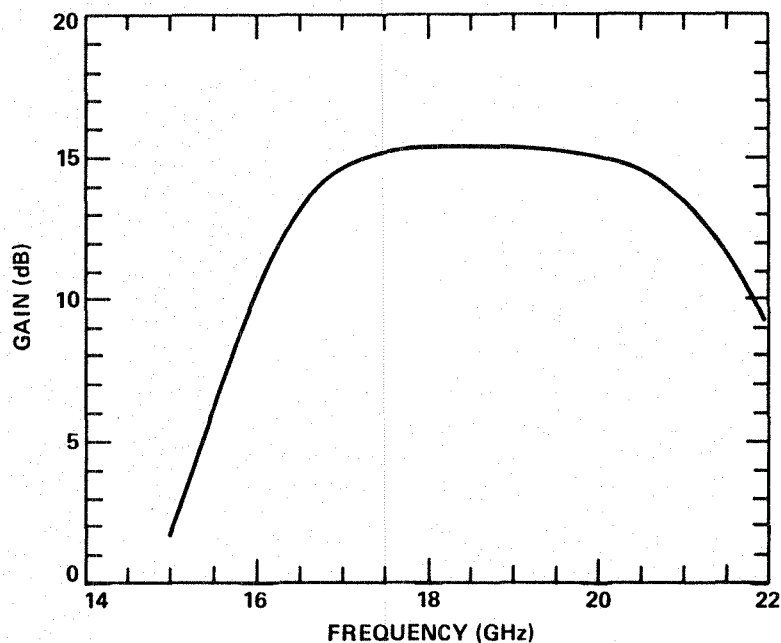
Fig. 28 Predicted gain of the three-stage amplifier for small signal conditions.

SC44458
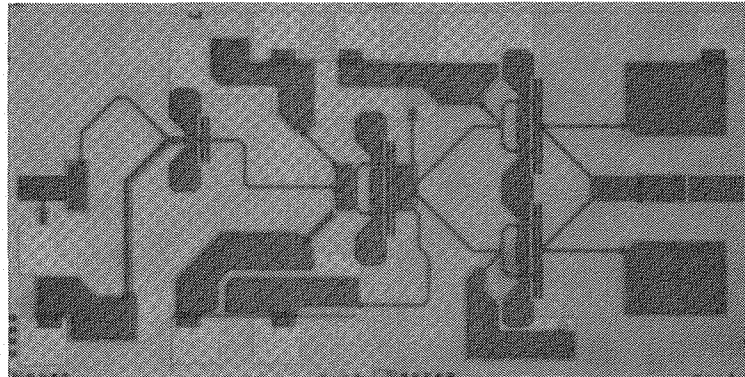
Fig. 29 Photograph of the layout of the three-stage amplifier.

center row cells are the dual driver and dual output stage, respectively. The bottom row consists of, from left to right, the predriver, the driver and the output stage. The two dual-stage amplifiers are arranged such that they can be sawed as a single four-stage unit if desired, and that the three single-stage amplifiers can also be sawed as multistage amplifiers.

3.3 Test Results

All test results presented, except the measured gain for the three-stage power submodule, were measured on the swept power meter previously described. With the exception of the dual output stage, which had a mask error resulting in a dc-shorted drain on the drive FET, all amplifiers performed close to expectations. Since the full three-stage amplifier was operating correctly, measurement and design efforts concentrated on characterizing and improving that design as much as possible for inclusion on the complete monolithic transmit module.

3.3.1 Single-Stage Power Amplifiers

Measured gain for the single-stage predriver amplifiers is shown in Fig. 30. Performance was close to expected values, the most notable aspect being the performance above band, which was designed for but was not fully expected to materialize. The driver had slightly less gain than expected, but gain was sensitive to the transconductance of the FETs used and only a few circuits from only two wafers were evaluated early in the program. Concentration on the three-stage amplifier precluded further analysis of these amplifiers.

3.3.2 Two-Stage Power Amplifiers

Measured gain for the dual driver is shown in Fig. 31. This amplifier had slightly less gain than desired, but once again the circuit was not studied in detail. This amplifier, as well as the single- and three-stage amplifiers, had oscillation problems similar to those described in Section 2.0. The solution proved to be the same also, i.e., the addition of low-frequency feedback resistors outside the dc bypass capacitors. These

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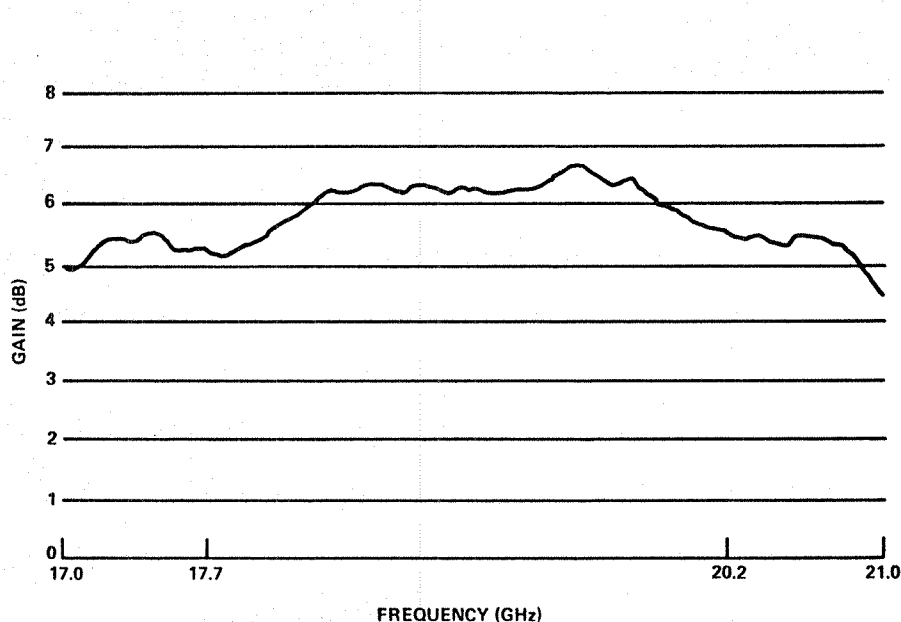
Fig. 30 Measured gain in small signal of the predriver stage.

MEASURED DUAL-DRIVER GAIN   23384
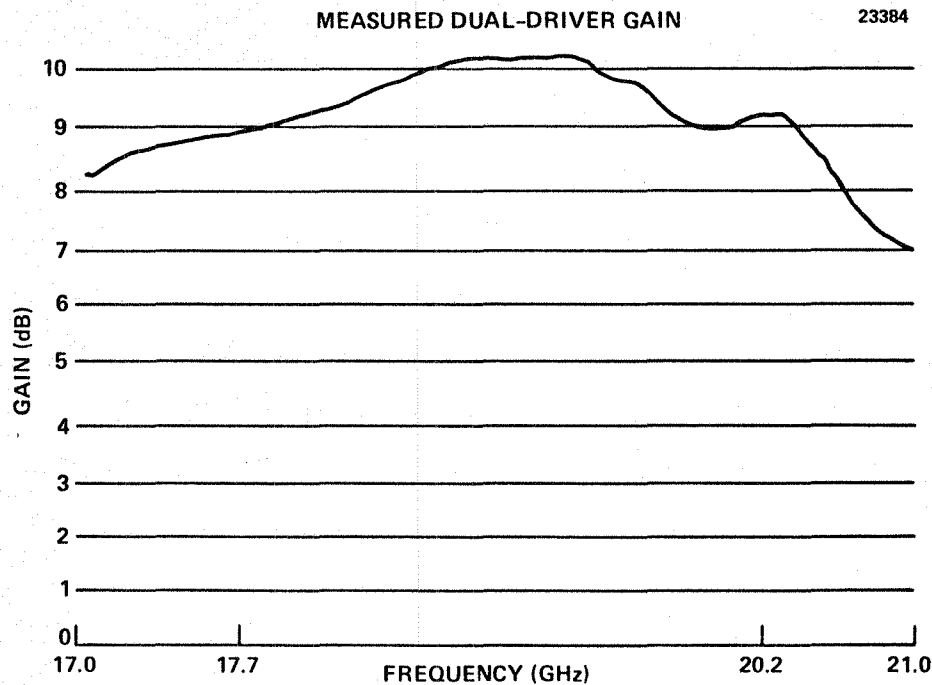
Fig. 31   Measured gain of the dual driver stage (monolithic combination of stages 2 and 3).

were to be monolithically integrated into future versions of the NASA circuits. The dual output amplifier had a mask error and could not be evaluated at rf frequencies.

3.3.3   Three-Stage Power Submodule

Measured gain for the three-stage power amplifier under small signal conditions is shown in Fig. 32. As shown in the figure, gain dropped significantly when the operating voltage was increased to the required 6 V for proper output power. This did not occur for discrete FETs taken from the test pattern (which went through the full MMIC processing), and the reason for this discrepancy is speculated upon in the following paragraph. Figure 33 shows measured performance for the discrete FET, and demonstrated that the FET was capable of the required 250 mW/mm with the existing doping profile (device B in Fig. 33). It also demonstrated that additional power could be obtained if an additional implant was used for the power devices; however, a gain penalty would be incurred by this process.[5] It is possible to make less dramatic changes in the

23383
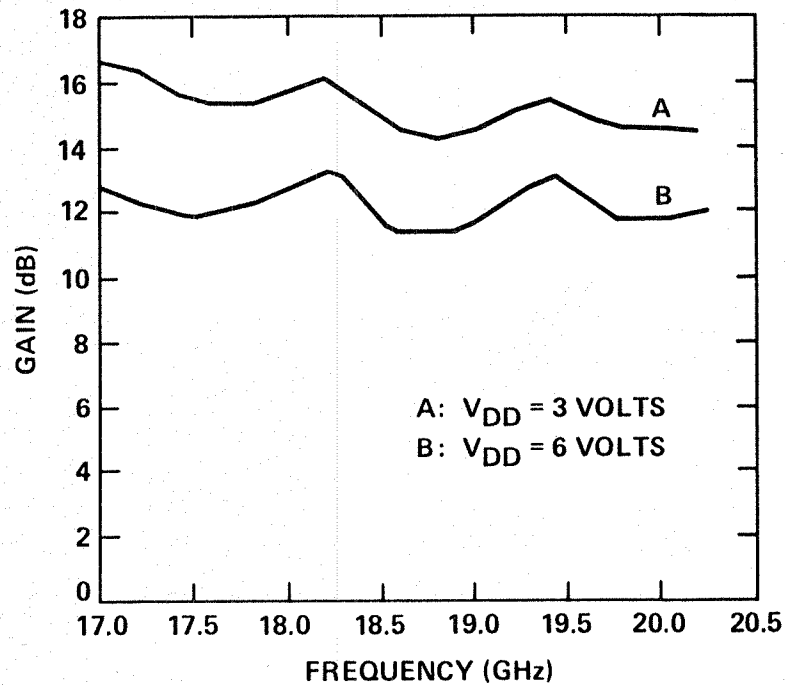
Fig. 32   Measured gain of the three-stage amplifier at two different bias levels and under small signal conditions.
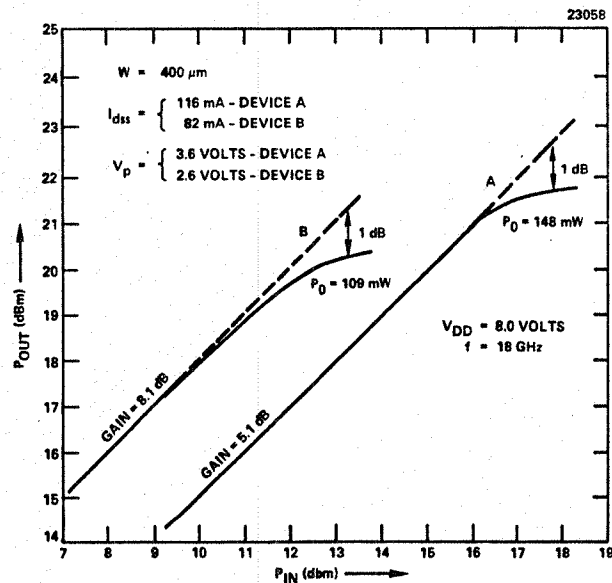
Fig. 33   The effect of profile tailoring in the enhancement of the power handling of transistors.   Device A with a profile optimized for power provides higher power levels at lower gain levels.

doping profile, which would produce less gain reduction and less power increase as well. Evaluation of a larger number of power submodules was expected to resolve the gain drop with increasing drain bias without major changes in the circuit or fabrication sequence.

Measured saturated output power for the three-stage power submodule was between +20 and +21 dBm. This was the same amplifier that exhibited the gain reduction, and was likely to represent a worst case for output power. The drop in gain in response to raising the drain voltage levels might be interpreted in terms of a bias level-dependent output impedance and the consequent detuning of the interstage matching networks. An alternative explanation might be that circuit elements such as the MIM capacitors exhibited voltage-dependent characteristics. A final possible explanation depends on thermal effects not being handled as well in the MMIC chip as in the discrete devices. No final selection of probable cause was made from these possibilities, although in retrospect the third (thermally related) cause is deemed the most probable.

4.0 20 GHz TRANSMIT MODULE INTEGRATION

Integration of the various components of the 20 GHz monolithic transmit module followed a two-step process. The first attempt at integration was realized in the NASA-3 mask set, which contained all the required elements totally interconnected on a 4.8 x 6.4 mm chip. Included in the chip were sufficient extra bias points and saw streets to diagnose any problems that might have been encountered. This was followed by a NASA-3A mask set incorporating some changes and eliminating redundant bias lines and wasted GaAs area.

In addition to the monolithic integration of the transmit module components, the early designs were interconnected via a hybrid approach. This served the dual purpose of uncovering any interactions not anticipated by the computer modeling, and providing a backup approach for the final module if insurmountable design flaws were encountered in the monolithic approach (which was not expected to be the case).

4.1 Hybrid Integration/Backup Approach

The hybrid interconnection of NASA-1 and NASA-2 circuits was initiated by cascading the five bits of the phase shifter on a single test carrier, as shown in Fig. 34. This configuration did not operate correctly, and exhibited an insertion loss in excess of 30 dB. Further analysis of the cascade indicated that the dc bias voltage on the rf signal lines was incorrect, and that it changed as a function of control line voltages (which should not have been the case). This problem was traced to extremely large bias isolation resistors on the phase shift modules, as previously described in Sect. 2.3.5, and illustrated the necessity of the hybrid interconnections even if they were not to be used in the final configuration.

The problem was discovered in time to be resolved on the NASA-3 mask set, and in addition a new polyimide mask was generated by electron beam lithography. The new mask set was used to process more NASA-1 circuits to obtain phase shifters without the resistor problem.

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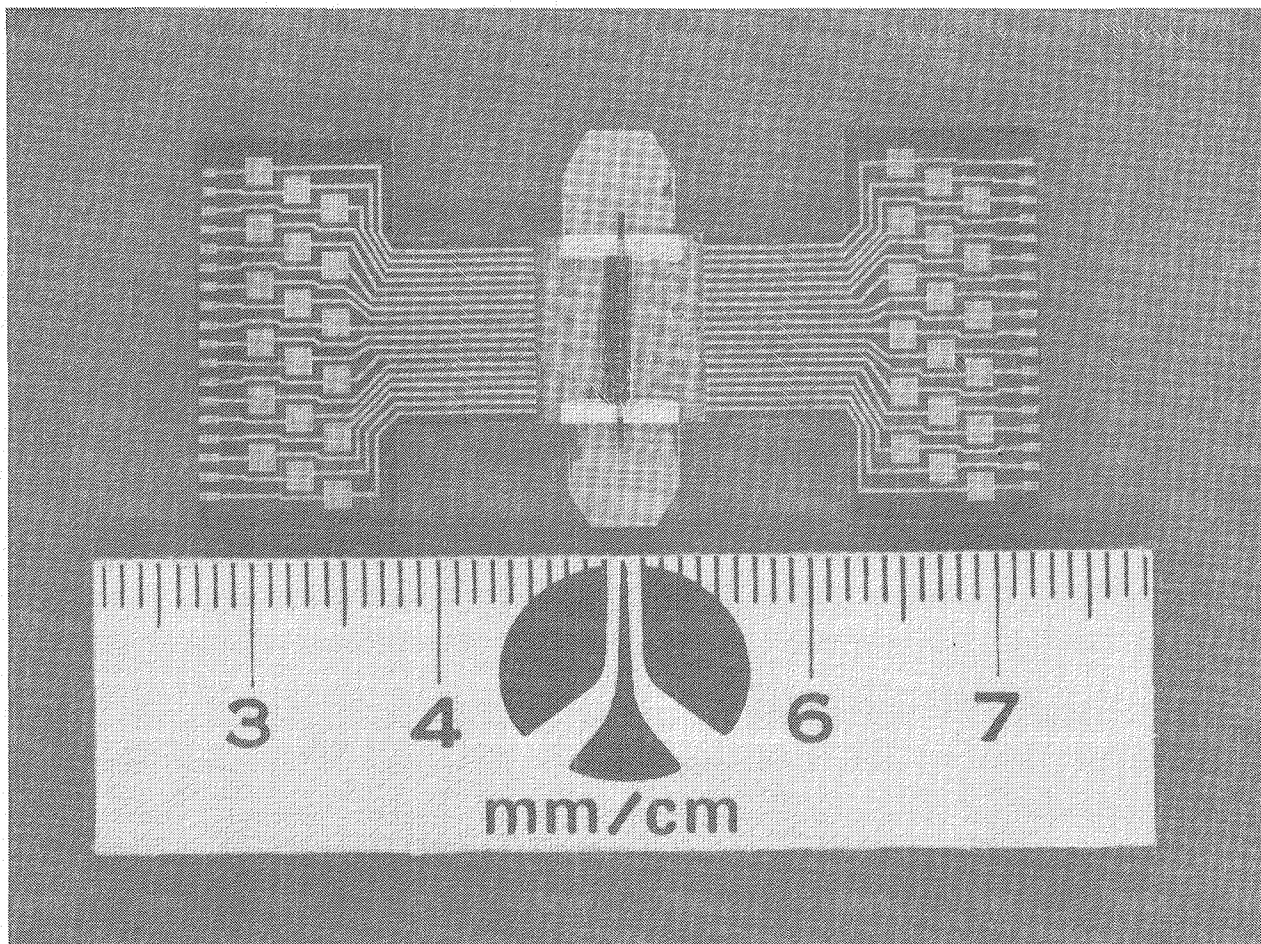
Fig. 34 Photograph of a 5-bit hybrid phase shifter in its test carrier.

4.2   Monolithic Integration

4.2.1   NASA-3 Designs

A fully monolithic transmit module chip operating over the 17.7-20.2 GHz band was designed. This 6.3 x 4.7 mm MMIC contained five phase shifter bits, five gain stages and digital interface circuitry. An overall gain of 15 dB has been achieved at band center, with only ±0.5 dB gain variation with changes in phase shifter state. Phase shifts were within 5° of the desired values. This MMIC represents the highest level of integration yet reported for circuits operating at 20 GHz. The IR-100 Award for Excellence in solid state designs was given to Rockwell for this work.

The module was required to have 5-bit phase control and gain of 16 dB over the 17.7-20.2 GHz frequency band and control of the phase shift state via a 5-bit, TTL-compatible digital input signal. Detailed design goals are summarized in Table 1. The design

41

of this circuit was implemented in terms of four functional building blocks, which are: 1) a 5-bit passive phase shifter; 2) a two-stage buffer amplifier to overcome the loss through the phase shifters; 3) a three-stage power amplifier; and 4) a digital interface to convert the control signal to appropriate voltages for the phase shifters. The 5-bit phase shifter was implemented as five distinct phase shifter circuits of 180, 90, 45, 22.5 and 11.25°. The interconnection of these building blocks is shown in Fig. 35.

The circuit design approach taken in the development of the fully monolithic transmit module was to implement each of the above building blocks and subcircuits as an individual circuit for test and design verification, as described in previous sections on NASA-1 and NASA-2. Next, the individual circuit designs were integrated into a mono-lithic IC with only minimal layout changes, resulting in the MMIC described here. By keeping the layout of the subcircuits unmodified, any interaction between circuits could be determined and analyzed.
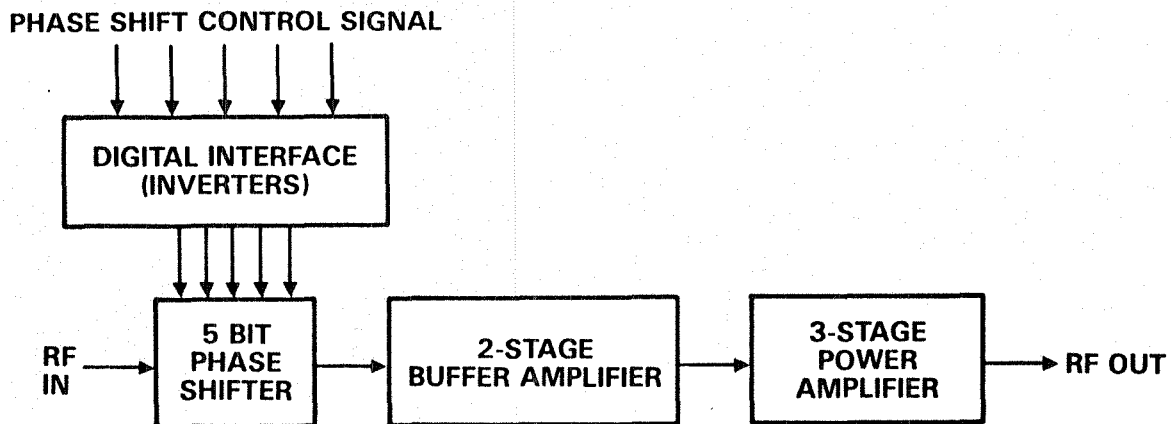

Fig. 35 Block diagram of the 20 GHz transmit module MMIC.

Table 1

Design Goals of 20 GHz Monolithic Transmit Module Chip

RF Band:	17.7 - 20.20 GHz
RF Gain:	≥ 16 dB
Gain Variation:	±0.5 dB over entire band and ≤ ±0.2 dB over any 500 MHz band
Power Output:	≥ 0.2 W at 1 dB gain compression
Power Added Efficiency:	≥ 15%
Phase Shifter:	Five bits with the following phase shift at band center (18.9 GHz): 180, 90, 45, 22.5 and 11.25° (±3° each). Total module phase shift should be proportional to frequency with a phase error ~ ±6° within the rf band
Phase Control:	Five-bit TTL signal

The first step in the development of the fully monolithic transmit module was to design, fabricate and test the subcircuits of the four building blocks shown in Fig. 35. These were designed as individual circuits on two different mask sets; the standard MMIC fabrication steps were used, assuring compatibility for subsequent integration. A summary of the results obtained is presented below.

Two-Stage Buffer Amplifier. The buffer amplifier was designed to have a gain of at least 12 dB from 17.7-20.2 GHz to overcome the expected loss of 12.5 dB (2.5 dB/ bit) through the 5-bit phase shifter chain. Measured performance was 13 ± 0.75 dB over the band.

Three-Stage Medium Power Amplifier. Design goals for the power amplifier were 16 dB of gain and 200 mW (23 dBm) of output power with power-added efficiency of 15% from 17.7-20.2 GHz. The starting point in the design of this high-efficiency power amplifier was the selection of the output FET characteristics; the power density and gain could be traded off under control of the device doping profile. Although localized ion implantation could be used to fabricate FETs with different doping profiles on the same chip, the design of this amplifier was based on a single, standard FET profile, the same as

used in the passive phase shifter switches and small signal amplifiers to avoid processing complexity and thus increase yield. With this constraint, the design goals of 16 dB gain, 200 mW power and 15% efficiency were quite challenging. Measured performance of the 1.5 x 3.1 mm, three-stage amplifier chip was 15 dB gain from 16.5-20.2 GHz and a saturated output power of 21 dBm, or 120 mW. Discrete FETs with the same doping profile and size as the output stage of the amplifier were evaluated for power performance, and were found to be adequate for the present requirements. Therefore, it was expected that minor changes in the matching networks would be required to meet the output power goal.

Five-Bit Phase Shifter. The phase shifter submodule consisted of a cascade of five binary phase shifters with phase increments of 11.25, 22.5, 45, 90 and 180°, respectively, at band center (18.9 GHz). Each bit was implemented as a switched line phase shifter (Fig. 2.1). This circuit approach was chosen as being the most appropriate when issues such as phase shift accuracy, amplitude variation with phase change, power consumption, and sensitivity to element values were considered. The phase shifter consisted of two SPDT switches capable of connecting either line A or line B (Fig. 1) to the rf signal. The difference in line lengths of A and B provide the desired phase shift. FETs with a 1 μm gate length are used in a series-shunt configuration to implement the SPDT switch. For a series FET width of 300 μm and shunt FET width of 120 μm, insertion loss of 0.7 dB and isolation of 15 dB were obtained in the rf band. Two such switches in each shifter bit provided an isolation of 30 dB, which was adequate for this application.

The five phase shifter bits can be clearly identified in Fig. 36, which is a photo of the fully monolithic transmit module. Measured phase shift and insertion loss data on an individual 90° phase shifter are presented in Fig. 37. Data for the other phase shifter bits are similar. The measurements were made on devices mounted in the Universal MMIC test fixture.[1] From Fig. 37, it is clear that the phase shift at band center is not exactly 90°. Such small errors in phase shift can be corrected easily by changing the lengths of the straight sections of delay lie in the phase shifter in the final design. The insertion loss of this phase shifter is also higher than the expected 2.5 dB at band center. Typical measured values ranged from 2.5 to 4 dB. Although measurement uncertainties of ±0.5 dB contributed to this variation; other (process related) reasons for the
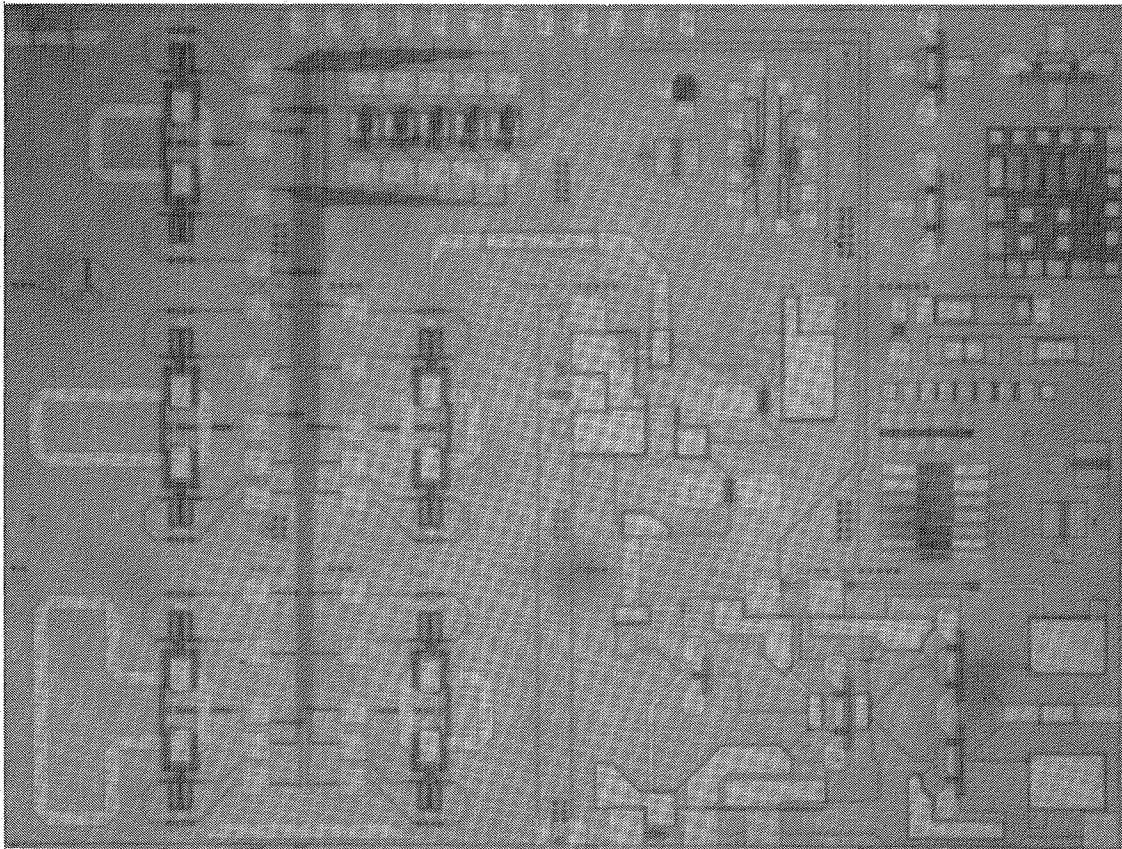
SC44460

Fig. 36 Photograph of the fully monolithic 6.3 x 4.7 mm 20 GHz transmit module.
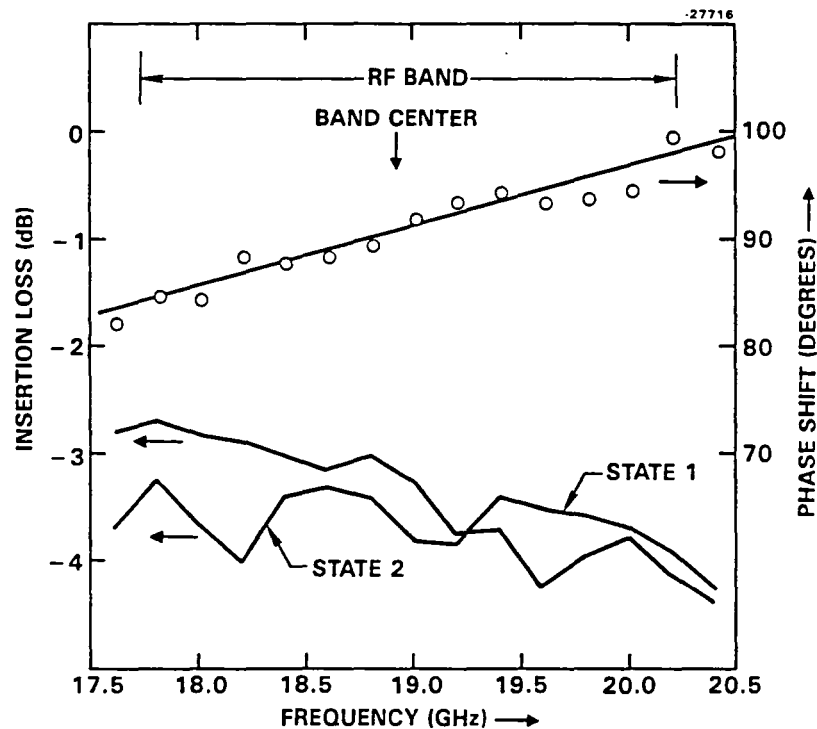
Fig. 37 Measured phase shift and insertion loss on an individual 90° phase shifter bit.

higher insertion loss were determined as the chips were being evaluated. The most apparent of these reasons included a larger FET "on" resistance than used in the model, mismatch losses, and a parasitic leakage current (through the semi-insulating substrate) between negatively biased ion-implanted resistors too closely spaced in the layout. This leakage current caused an uncontrolled voltage drop across the gate bias resistors so that the switch FET was only partially turned off. In summary, the loss of the transistor-implemented SPDT switch in the phase shifter was higher than expected, primarily because of higher resistance in the "on" state of the transistor. A secondary but significant cause of loss in the phase shifter was failure to fully pinch off the shunt device in the "closed" branch of the switch.

Digital Interface. Since the compound SPDT switch of Fig. 2 required both true and complement control signals, an inverter circuit was required for each of the five input control lines to minimize interconnections. Furthermore, the TTL input signal had to be conditioned to provide ≈ +1 V to turn a FET "on" and -5 V to turn a FET switch fully "off" (assuming a FET threshold of -3 V). The terminals of the phase shifter FET switch were maintained at +5 V and the inverter provided 0 or +7 V to the gate terminal (through a 20K resistor). Five such inverters were included on the fully monolithic chip.

4.2.2   NASA-3 Results

Except for the inclusion of some low-frequency ($<$ 50 MHz) stabilization circuitry, the circuits were essentially unchanged from their discrete form. Many bonding pads and test circuits were scattered throughout the chip for diagnostic purposes. Gain and total phase shift vs frequency for the reference state are shown in Fig. 38. Gain rolloff at the high band occurred at a lower frequency than predicted. This was consistently observed on the five-stage amplifier chains from this mask set, but was not observed in the discrete amplifiers fabricated earlier.[2,3]

Overall gain was lower than expected by ~ 2.5 dB due to the higher phase shifter insertion loss. Another problem encountered here was an in-band oscillation for large drain biases which had precluded output power measurements on these chips. The cause of this oscillation was determined; some of the intermediate stages were potentially unstable, although the entire amplifier was designed to be stable. Differential
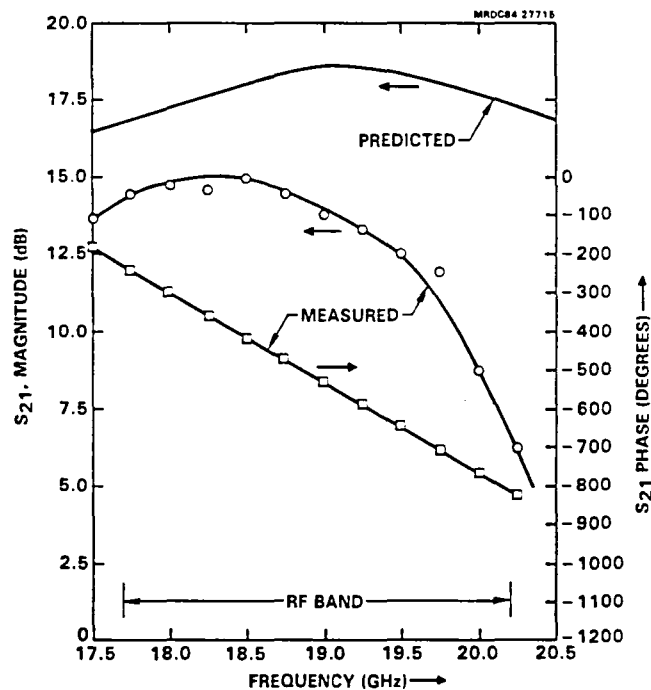

Fig. 38   Gain and total phase shift vs frequency for the reference state of the monolithic transmit module.

insertion loss (ΔIL) and phase shift (Δφ) data are presented in Figs. 39 and 40, respectively. At band center, ΔIL is ≤ ±0.5 dB, although this degraded at the high end due to the premature gain rolloff. Δφ was within 5° of the desired value. These data were obtained in some of the earliest functional chips, from which minor processing improvements have been determined.

Yield. The MMICs reported were fabricated by Rockwell's standard ion implantation based technology, which has been described earlier.[4] However, due to the significantly increased complexity of the fully monolithic chip, as evidenced by the statistics in Table 2, fabrication yields had to improve considerably before completely functional chips could be obtained. A topic of interest was the overall fabrication yield of the monolithic transmit module. Clearly, the yield depended on the design rules used for the circuits. The design of the final mask set incorporated the detailed experience gained in fabricating this circuit and adjusting the layout for maximum yield.
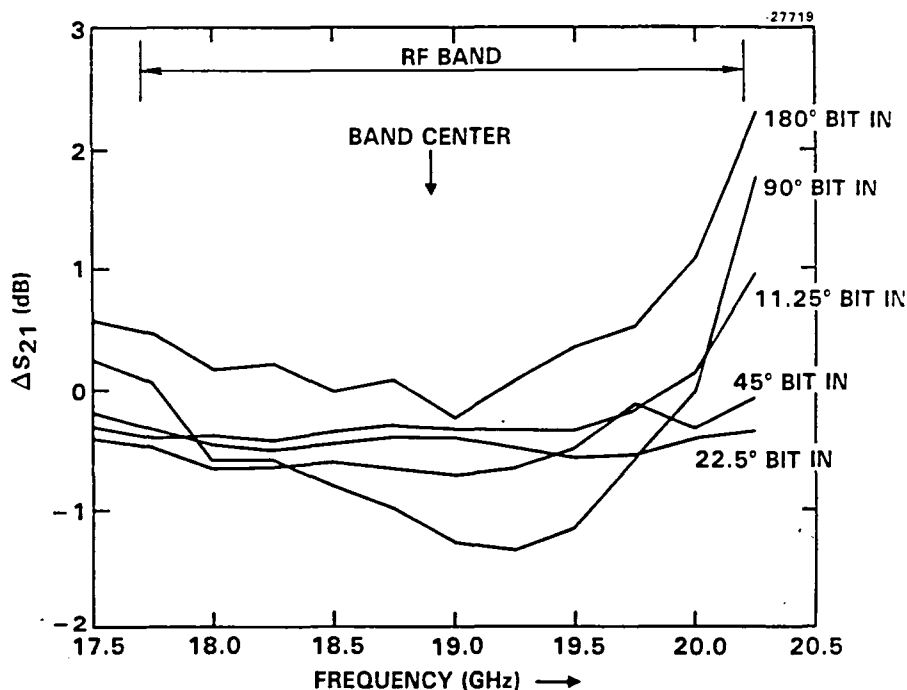

Fig. 39 Differential insertion loss for five different phase shifter states.

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Fig. 40 Differential phase shift vs frequency for the five different phase shifter sections.
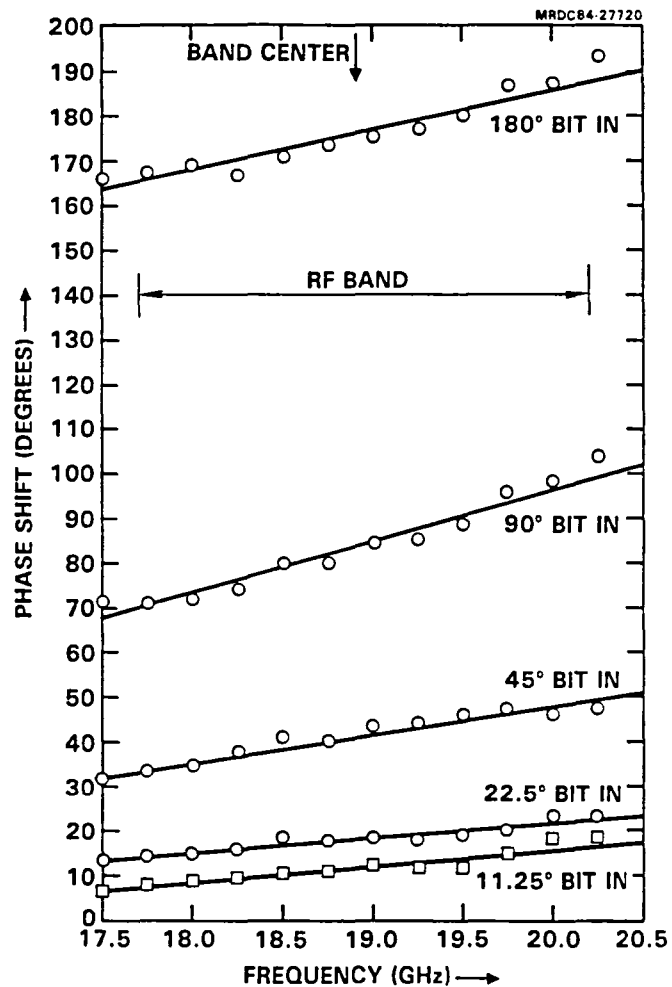
Table 2

Salient Statistics of Monolithic Transmit Module Chip

1.	Chip Size	6.3 x 4.7 mm^2
2.	Total Gate Periphery	11.5 mm x 0.65 μm
3.	Number of MIM Capacitors	32
4.	Total MIM Capacitance	180 pF
5.	Number of Resistors	106
6.	Number of Via Holes	28

The 6.3 x 4.7 mm MMIC contained five phase shifter bits, five gain stages and digital interface circuitry. An overall gain of 15 dB was achieved at band center, with only ±0.5 dB gain variation with changes in phase shifter state. Phase shifts were within 5° of the desired values. Prior to the fully monolithic version, four functional building blocks that together comprise the chip were designed and tested. Amplifier gains were

in accordance with the modeling, but the phase shifter insertion loss was ~ 1.5 dB/bit higher than expected. Further work was done to reduce the loss, including minor changes in switch design and the design rules used for circuit layout. The monolithic chip showed gain rolloff at a lower frequency than was measured for the discrete circuits; also, an in-band oscillation was observed. The causes of these problems were determined and corrected in the next mask set, i.e., NASA-3A.

4.2.3 NASA-3A Design

The experience gained from the activity using mask set NASA-3, which occurred during FY 1984, providing a lot of feedback information for the designers. On one hand, the proper function of each component in the transmit module was confirmed in that the phase shifters and power amplifiers worked as intended (or nearly so). On the other hand, the yield from this large IC was miserably small. Three factors stood out as needing attention in the preparation fo the next mask set. These were:

1. The yield of fully functional circuits had to be increased dramatically either with the existing contact lithography technology or in a new projection lithography technology.

2. The power amplifier (CGA) had to be modified in a manner to insure that it would provide the 200 mW of output power sought.

3. The variable phase shifter (VPS) had to be modified to provide a lower insertion loss.

The new mask set addressed all these problems. Since, faced by circumstances, it could not be construed as a final mask set with optimized chip designs included, it was named NASA-3A to affirm its developmental nature. The most significant change adopted for NASA-3A is the separation of the VPS from the power amplifier chips. The VPS and its associated buffer amplifiers were placed in one chip and the power amplifier on a separate chip. This was done in response to an unexpected request from the customer, but its implementation aided the cause of obtaining a higher yield of fully functional chips.

For the loss in the VPS, the principal design actions taken were to improve the matching condition prevailing at the input of each VPS section. The SPDT devices in shunt in the signal path line provided a substantial capacitive shunt admittance. This was solved by providing shorted shunt stubs in parallel across these devices designed to tune out the capacitive admittance with an inductive admittance. These shunting stubs are visible in the VPS section of Fig. 41 in the NASA-3A reticle.

The amplifier was changed to meet the power specification through two steps. A new amplifier (called CGAP) was designed which used larger transistors in all stages (i.e., 250, 600 and 900 μm of periphery in the three stages). This step was accompanied by a revision of the output matching circuit that takes into account the large signal output impedance of the output stage transistor. The interstage networks were also reoptimized.
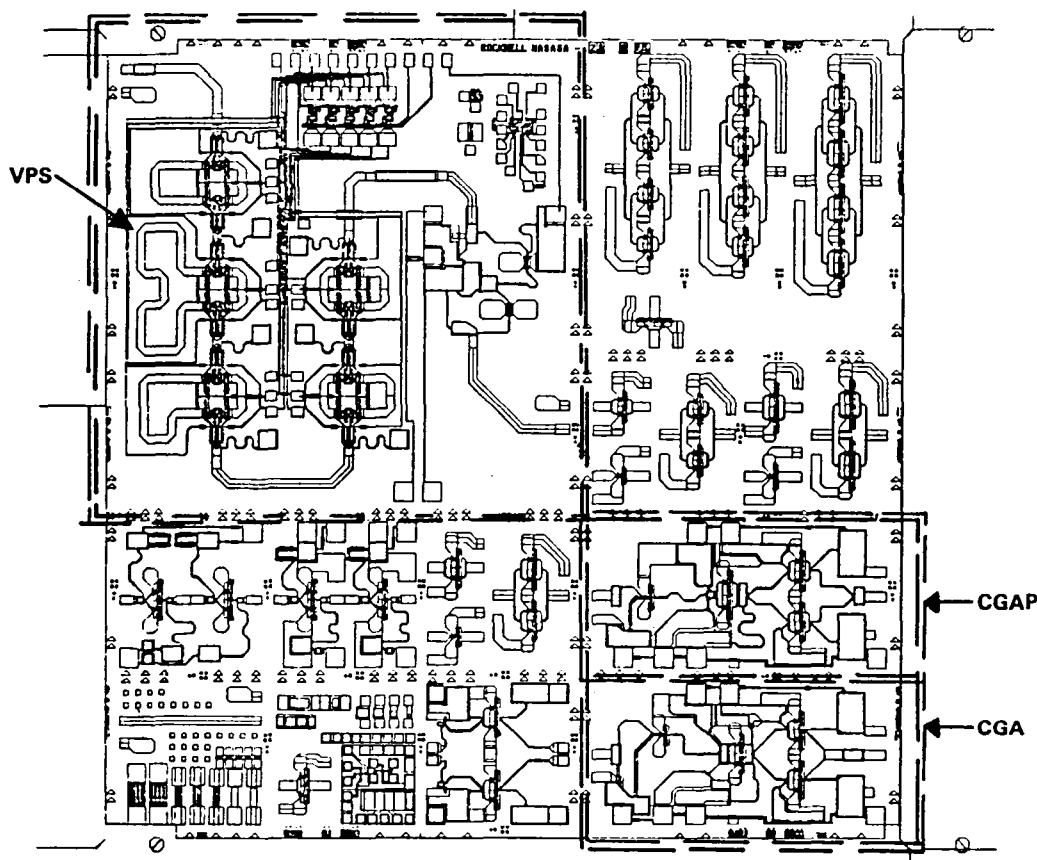

Fig. 41 Layout of the NASA-3A reticle.

The problem of achieving an overall upgrade in the yield of working circuits was the most significant step based on the NASA-3 experience. In general, it was discovered that the tolerances of alignments, overlay placements and protection layers were too tight and could not be met by the contact alignment technology.

As an example, the protection layer that must be placed over devices and ohmic contacts to protect against subsequent etch steps did not overlap the complete area to be protected. Alignment accuracies that were required could not be met, resulting in subsequent etching of critical ohmic contacts and the inevitable loss of working devices. The modifications made were to add more safety tolerance to these process steps. Electron beam lithography was made a normal part of the process (it had been introduced with later lots of NASA-3 for better yield).

The mask set NASA-3A was finally procured in two versions. The first, a projection mask set (10X), was procured under IR&D funds to develop the 3 in. wafer process. This latter intention was part of Rockwell's plan to move the processing of these wafers and chips into a more production-worthy environment, i.e., the DARPA Pilot Line. The second version was procured as a contact lithography based tool to provide some early samples of the chips from the NASA-3A wafers. In fact, most of the currently available chips (constituting deliverables) will come from the lots processed by the contact/electron beam lithography combination.

The processing of NASA-3A took place during FY 1985. Fifty wafers in total were processed, partly under contract and partly under IR&D, with the objective of adapting the process for 3 in. wafers and for introduction into the Pilot Line. A total of 500 die for the CGAP amplifiers were thus made available. From these, there has been a nearly 10% yield of working devices. The VPS chips were not so fortunate, as another mask error undetected for a long time spoiled yield of those devices. Nevertheless, some working fully functional VPS chips are available and have been tested.

The process was ultimately transferred to the Pilot Line. A new method was developed at that facility for the fabrication of submicron gates with optical lithography. MMICs are now routinely produced in that facility with final "rf good" yields in excess of 25%.

4.2.4   NASA-3A Results

4.2.4.1   Variable Phase Shifter Chips

This chip presents a complex test task. It must be checked for phase accuracy and gain or insertion loss variation for every phase setting. This is most conveniently and quickly done under computer control.

In total, about 24 wafers were successfully processed with a correct mask set for the VPS chip. A small number (seven) of fully functional phase shift chips has resulted. The low yield is a problem that can be dealt with by further mask improvements as the hazard is a process-related one.

To present the performance of the VPS chips, the method chosen is to show the results of measurements on one of the working VPS's in a series of figures.

In Fig. 42, the phase setting accuracy of a VPS from wafer 10427 is examined. The control exerted by the digital TTL input control signals is shown in this exhibit of phase vs frequency. The working band is between marker 1 and marker 5 on the display. The table in the figure provides a reading of accuracy. This is very good, with only the 11.25° and 180° VPS providing errors above 4°; 5° was the specification.

In Fig. 43, the total gain/insertion loss through the 5-bit VPS set to 0° reference is exhibited. The increase in insertion loss in the upper segment of the band is quite steep. This is believed to be a function of the buffer amplifier. The exhibited performance, however, is still quite good at 20.2 GHz, which is between (halfway) markers 4 and 5. Therefore, a net gain is available across most of the 17.7 to 20.2 GHz band.

In Fig. 44, the envelope of gain variation as the 32 different phase states are dialed in is recorded. it is apparent that the delta of insertion loss is most marked or observable for the 180° phase shifter, a fact that is confirmed by Fig. 45.
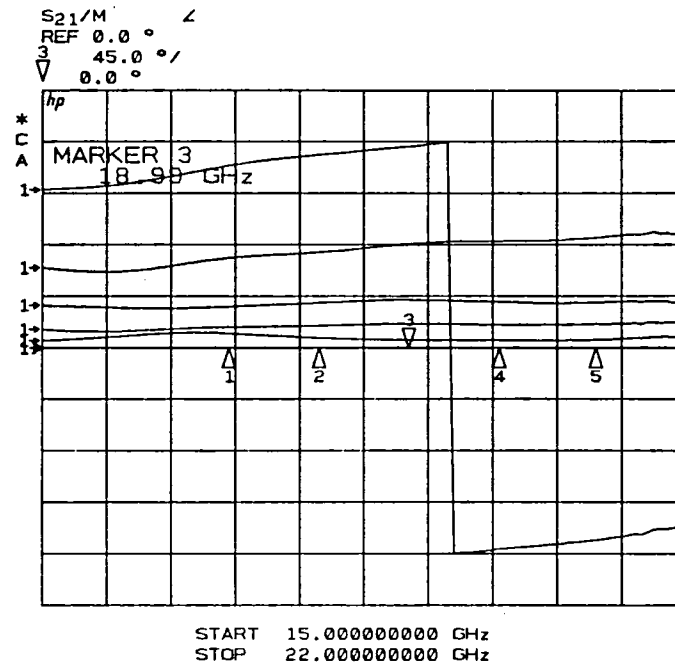
S₂₁/M∠
REF 0.0 °
3   45.0 °/
▽ 0.0 °

Fig. 42 Phase-setting accuracy of the 5-bit VPS chip from wafer 104271-1-6.

S₂₁   log MAG
REF -10.0 dB
3   2.0 dB/
▽ -8.4888 dB
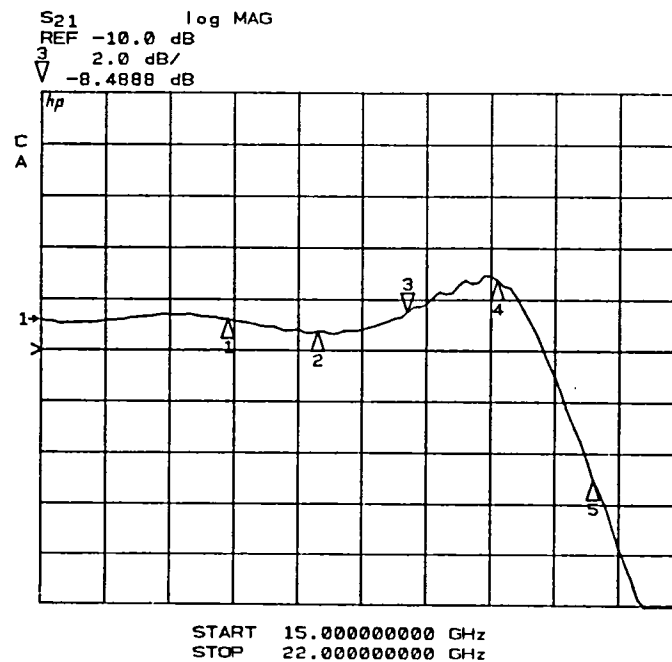
Fig. 43   Small signal gain/insertion loss through the VPS and associated buffer amplifier, chip 104271-1-6.

S21/M LOG MAG
REF 0.0 dB
3   0.5 dB/
▽   0.0002 dB

180°-258.75°

270°-348.75°

0°-168.75°

START 15.000000000 GHz
STOP 22.000000000 GHz
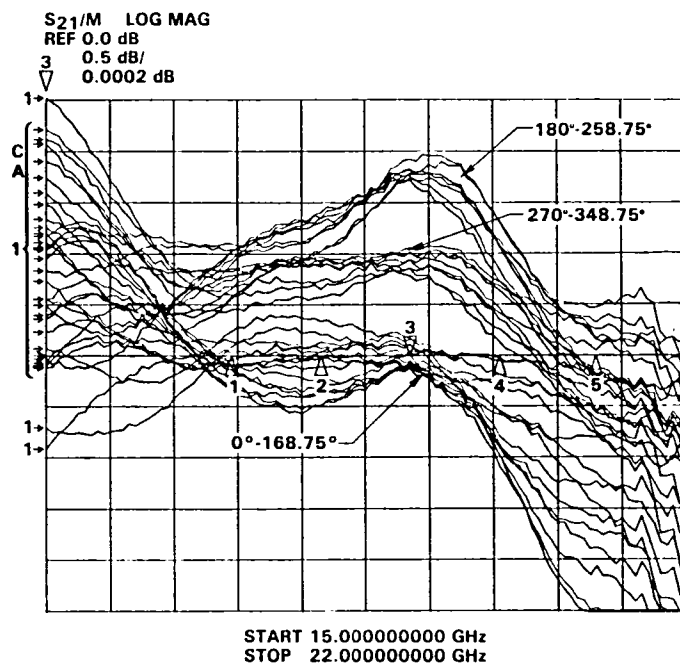
Fig. 44   Survey of the insertion loss delta for all 32 phase-setting combinaions, chip 104271-1-6.

S21/M LOG MAG
REF 0.0 dB
3   0.5 dB/
▽   0.3749 dB

A

180°

22½°

90°

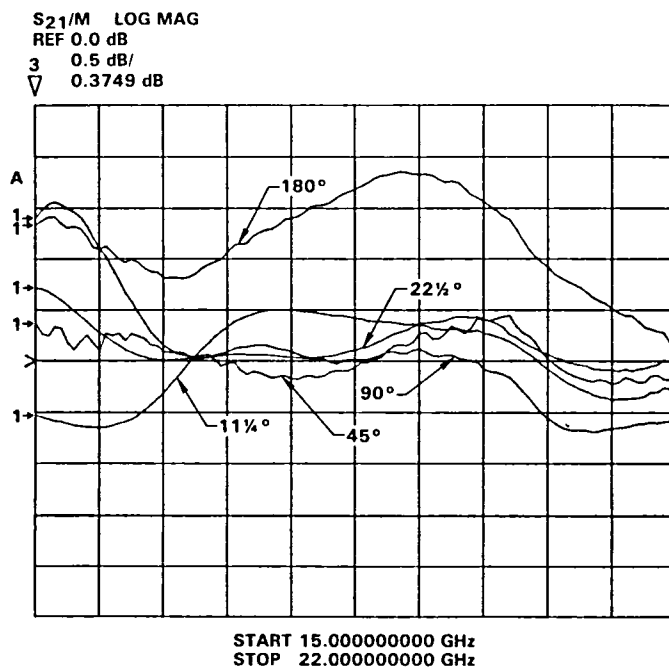11¼°

45°

START 15.000000000 GHz
STOP 22.000000000 GHz

Fig. 45 Differential gain or insertion loss for the five bits of phase shift.

The return loss of these VPS chips is generally well behaved, as attested to by Fig. 46. General return loss values are greater than 10 dB.

4.2.4.2 Amplifiers

The amplifier of interest must be the CGAP as it provided the greatest gain and high power performance. In general, with power supply voltage of 8 V to the final stage, the maximum power output, at about 2 to 3 dB of gain suppression, was +23 dBm. This is confirmed by the characteristics of Fig. 47. In this figure, a three-stage CGAP amplifier from wafer 10436 is providing a small signal gain of 18 dB and a 1 dB gain compression power level of +21 dBm. The maximum power output is +23 dBm.

The S-parameters of another representative amplifier from wafer 10427 (the same wafer as used for the VPS example) can be seen in Fig. 48. High levels of gain have been consistently observed. In Fig. 49, the gain from an amplifier from wafer 104271 is over 18.95 dB maximum and is over 18 dB from 16 to 22.5 GHz.

S_{11} LOG MAG
REF 0.0 dB
10.0 dB

45°/BIT OFF

45°/BIT ON

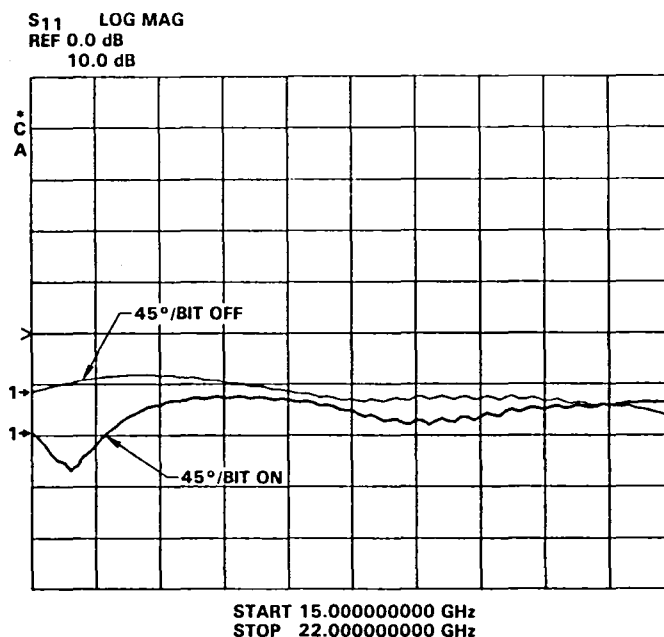START 15.000000000 GHz
STOP 22.000000000 GHz

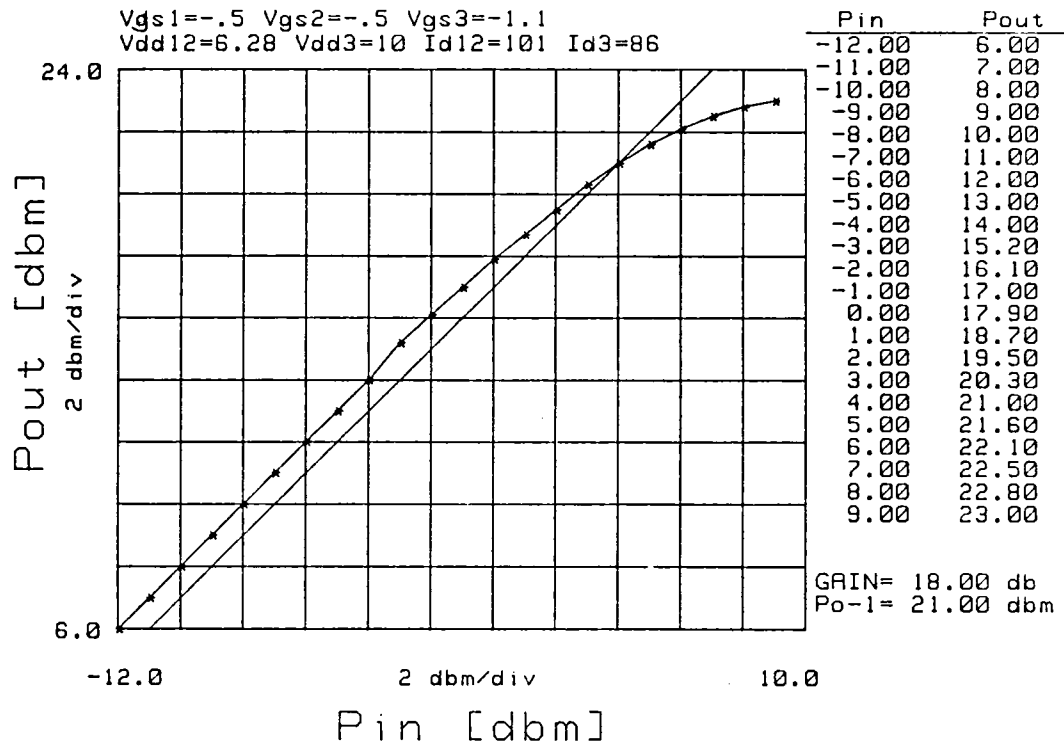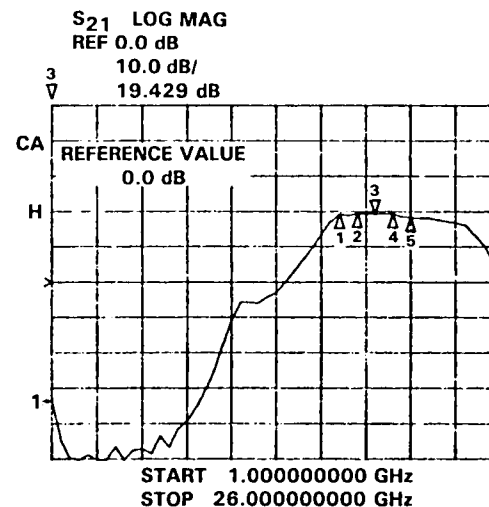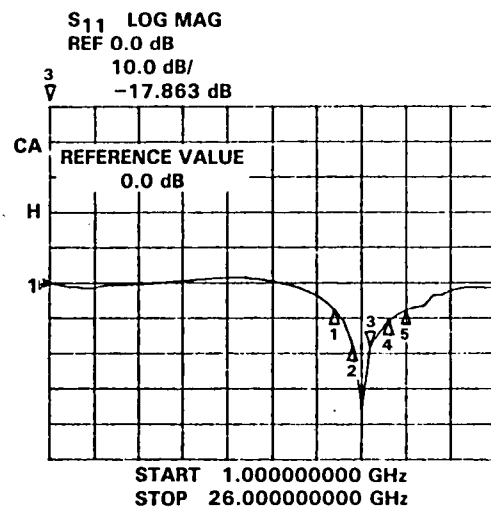Fig. 46 Return loss of the 5-bit phase shifter in two phase states.

Fig. 47   Power saturation characteristic for the CGAP power amplifier from wafer 10436. A 1 dB compression occurs at approximately 21.5 dB and a maximum output power of 23 dBm is observed.

These amplifiers were obtained with a very respectable yield from many wafers (about 10% average yield).

S$_{11}$ LOG MAG
REF 0.0 dB
10.0 dB/
−17.863 dB

CA REFERENCE VALUE
0.0 dB

H

START 1.000000000 GHz
STOP 26.000000000 GHz

S$_{21}$ LOG MAG
REF 0.0 dB
10.0 dB/
19.429 dB

CA REFERENCE VALUE
0.0 dB

H

START 1.000000000 GHz
STOP 26.000000000 GHz

NASA3A
104271-1-6
CGAP
$V_D = 3.0V$
$V_{61} = V_{62} = V_{63} = 0$
$I_{DSS} = 225.6$ nf
7/18/85

S$_{12}$ LOG MAG
REF 0.0 dB
10.0 dB/
−46.338 dB

CA REFERENCE VALUE
0.0 dB

H

START 1.000000000 GHz
STOP 26.000000000 GHz

S$_{22}$ LOG MAG
REF 0.0 dB
10.0 dB/
−6.7864 dB

CA REFERENCE VALUE
0.0 dB

H

START 1.000000000 GHz
STOP 26.000000000 GHz
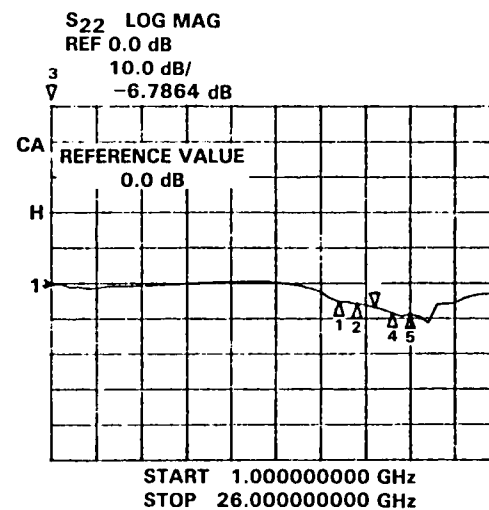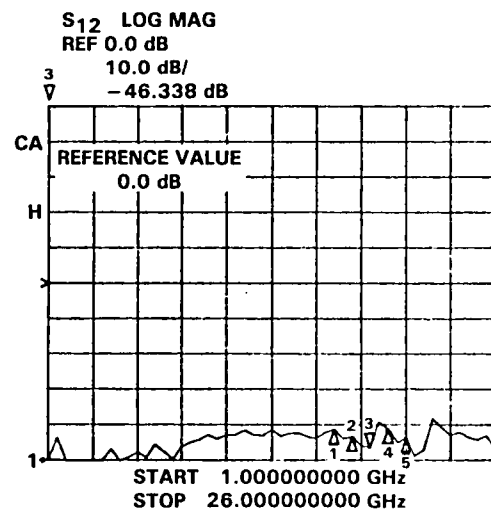
Fig. 48 S-parameters of the typical three-stage power amplifier module.

Rockwell International
Science Center
SC5492.FR

S21   log MAG
REF 0.0 dB
3   10.0 dB/
∇   18.956 dB

hp

*
C
A

SCALE
10.0 dB/div

1→

START   1.000000000 GHz
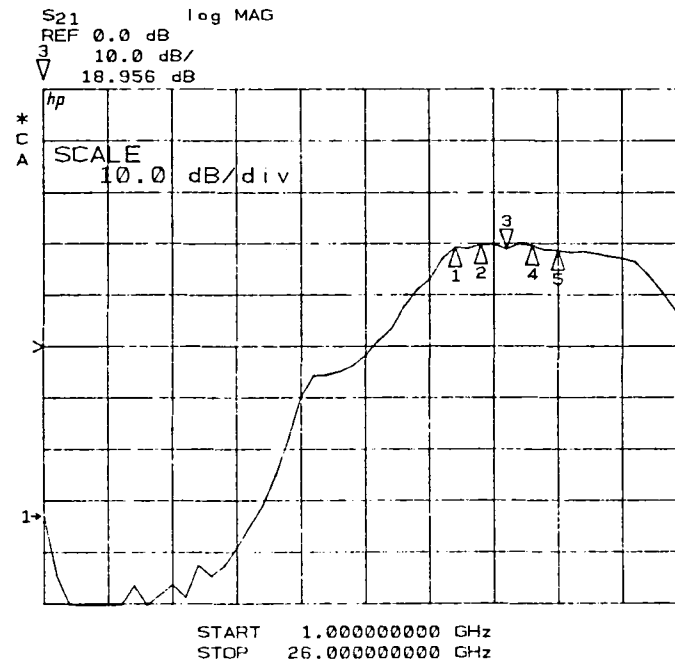STOP   26.000000000 GHz

Fig. 49   A CGAP amplifier from wafer 104271 exhibits 18.9 dB small signal gain. The design band is between markers 1 and 5.

5.0 PROCESSING TECHNOLOGY

5.1 Fabrication Technology

GaAs MMIC fabrication technology at Rockwell is based on direct, localized ion implantation for active layer formation, contact photolithography for most patterning steps, plasma-enhanced CVD Si_3N_4 for MIM capacitors, air bridges for crossovers, through-substrate via holes for ground connections, and a refractory metal-based metallization system for promoting high reliability. Dry processing techniques including ion milling, reactive ion etching and plasma etching were used extensively where required. This led to the development of a high yield process with state-of-the-art circuit performance. Tight control of all important fabrication steps was maintained through an extensive use of test patterns on the wafer. Further control over device performance was afforded by the availability of in-house grown semi-insulating GaAs and a strong internal program in materials technology. A CALMA GDS II computer-aided design system was used for design and layout of IC masks, producing the pattern generator tapes required for mask fabrication. The incorporation of this system greatly facilitated circuit design operations. Mask sets were digitized in metric units (microns). Except for mask fabrication, which was either carried out at a different Rockwell facility (Optomask) or by a commercial outfit, all operations required for MMIC processing were performed at the same location in Thousand Oaks, CA.

A contact lithography process (including FET gate definition) has been used successfully for fabricating devices for this program. Although electron beam lithography direct write was not strictly required for this program, it has been used for the NASA-3 and NASA-3A mask sets. Details of the fabrication approach, including material considerations and processing sequence are presented in the following sections.

5.1.1 Material and Implantation Technology

Complex monolithic circuits require more than one type of active layer on the same substrate to optimize the performance of the circuits. To accommodate this need, active layer formation is based on direct, localized ion implantation into high-quality semi-insulating GaAs substrates. In previous years, lack of control in the preparation of semi-insulating GaAs led to the development of qualification procedures which assessed

the suitability of individual ingots for direct ion implantation processing. Typically, ingots are doped with Cr to compensate the background impurities or are grown undoped from the melt under conditions where stoichiometric defects cause compensating deep centers. In recent times, this latter type of undoped semi-insulating GaAs dominates. In either case, the following conditions must be met to allow the successful implantation of an active layer.

1. The compensating impurities and defects in the substrate must not significantly affect the electrical properties of the ion-implanted layers, so that carrier concentration, mobility, carrier lifetimes, etc., depend only on the identify and dose of the implanted ions. Meeting this condition would insure that the electrical properties of the implanted layers are independent of the substrate, and it will guarantee that the implanted layers can be prepared reproducibly.

2. Unimplanted portions of the semi-insulating substrate must retain their high resistivity after a wafer has been capped and annealed, so that electrical isolation is maintained between the doped regions.

3. The substrate must be homogeneous. This implies that conditions 1 and 2 must be met with a minimum of short- or long-range inhomogeneities or defects. In addition to homogeneity, flatness requirements on the wafers are stringent for high yield realization of small geometries on large wafers.

The preselection tests for bulk semi-insulating substrate involve qualification of the entire GaAs ingot by sampling the front and rear of each boule. Extensive data have shown all wafers within the ingot are qualified when samples from both ends pass the qualification tests. The electrical criteria for qualification involves the two tests listed below:

1. **Thermal Stability.** The semi-insulating GaAs samples are capped with 1100Å sputtered Si_3N_4 and annealed at 850°C for 30 min in a H_2 ambient.

After removal of the Si_3N_4 cap, Au-Ge-Pt ohmic contacts are formed and the sheet resistance is measured. A sheet resistance $\geq 10^7$ Ω/sq is required to pass this test. The uniformity of sheet resistance across the wafer and variation between the two ends should be within 10%. This test assures against thermal conversion of conduction type and gross resistivity degradation effects.

2. **Ion Implantation Test.** A 3.5×10^{12} cm^{-2}, 125 keV Si ion implant is performed at room temperature. Samples are then capped and annealed as in No. 1. Following annealing, the cap is stripped and Al Schottky barrier metal is evaporated onto the test samples. Doping profile and mobility measurements are made to characterize the active layer and certify that it is suitable for device fabrication. Activation $\geq 80\%$, electron mobility ≥ 4500 cm^2/V-s, and a peak carrier concentration of $\sim 1.5 \times 10^{17}$ cm^{-3} with depth at a concentration of 10^{16} cm^{-3} of 2600 ± 300Å is required. The uniformity of doping profile across the wafer and variation between the front and the tail end of the ingot is required to be within 5% to permit a reproducible implant profile in the active from wafer to wafer.

Three-inch diameter undoped LEC GaAs wafers are currently available for IC fabrication. During the time of this contract, however, the processing of MMICs at Rockwell followed a contact lithography method so that the subject program of this report was executed using quarters of 3 in. wafers for the most part. In the later stages of the program, 3 in. wafers were used and they are the only size used in the Rockwell Pilot Line.

Si, S and Se gave been used as implanted dopants in our laboratory for MMIC active layers, with Si as the preferred dopant because of its high activation and excellent profile reproducibility. Si implants can be done at room temperature (instead of 200°C, as required by the heavier elements), thereby permitting greater sample throughput. Si implants are carried out through a 500Å thick cap of reactively sputtered Si_3N_4 using an Extrion 400 keV implanter. A 1.4 μm thick layer of photoresist is used as an implantation mask. Typical implantation conditions are as follows:

	Ion	Temperature	Dose
FET Active Layer	^{29}Si	~ 23°C (room temp.)	5×10^{12} cm^{-2}, 260 keV 5×10^{12} cm^{-2}, 100 keV
Bulk Resistors	^{29}Si	~ 23°C (room temp.)	3.5×10^{12} cm^{-2}, 170 keV
N$^+$ Contacts	^{29}Si	~ 23°C (room temp.)	---------

The FET channel implant is deep (peak at ~ 2000Å) and has a high surface concentration. This allows the FET gate to be recessed by ~ 1000Å and minimizes gate-source parasitic resistance. Following the localized ion implantation, the wafers are cleaned, capped with an additional 600Å of reactively sputtered Si_3N_4, and annealed at 850°C for 30 min in H_2 to electrically activate the implant.

5.1.1.1 Reproducibility and Uniformity

Excellent uniformity and reproducibility of active layers formed by direct, localized ion implantation has been seen. Figure 50 shows the reproducibility of a 100 keV, Si, 3.5×10^{12} cm^{-2} implant doping profile in various types of substrates, processed at different times. It indicates that well-controlled active layers with identical profile depth, carrier concentration level and mobility have been achieved to insure uniformity from run to run. Saturation current uniformity (I_{dss}) of a 200 µm wide FET for one quarter of a 3 in. LEC wafer is shown in Fig. 50. A standard deviation of less than 6.5%, the mean current, is a typical result. These results clearly show that direct ion implantation in semi-insulating GaAs is capable of providing highly uniform, reproducible device-quality active layers. In addition, this technology leads to planar structures with improved reliability over the mesa approach. Highlights of the ion implantation technology are presented in Table 3. It is because of these advantages that we favor this approach for active layer formation in MMIC programs for 1 to 26 GHz.
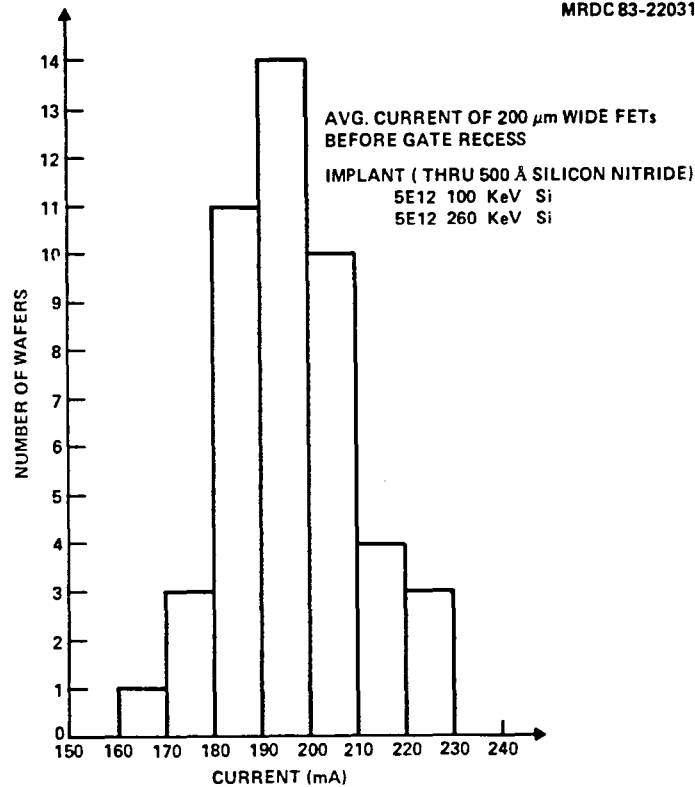
MRDC 83-22031

AVG. CURRENT OF 200 μm WIDE FETs
BEFORE GATE RECESS

IMPLANT (THRU 500 Å SILICON NITRIDE)
5E12 100 KeV Si
5E12 260 KeV Si

Fig. 50   A histogram of I_{dss} values in 200 μm wide FETs on an implanted layer. These values were measured prior to gate recess etch.

Table 3

Summary of Wafer Uniformity and Reproducibility
by Ion Implantation

Wafer Properties	Ion Implanation
Active Layer Uniformity (I_{dss})	6%
Reproducibility (I_{dss})	6%
Buffer Layer Capability	None required
N^+ Capability	10^{18}
Planar Capability	Yes

5.1.2 Circuit Fabrication Technology

The circuits described in this report were fabricated on semi-insulating GaAs substrate using state-of-the-art high yield processes. All processes were consistent with the design goal for operating life in excess of 2×10^5 h. Typical circuit elements comprising an MMIC are depicted schematically in Fig. 51. GaAs MESFETs were used as the active devices and Schottky diodes for level shifting applications. Except for very small values, resistors were formed by ion implanting a 1000 Ω/sq active layer. Small resistors were fabricated using the ohmic metallization which had a sheet resistance of ~ 2 Ω/sq. The dissimilar active layer requirements of FETs, diodes and resistors were met by multiple, localized ion implantation, as discussed in the previous section. In the processing sequence outlined later, contact lithography was used at the time of this work for all patterning steps, including the definition of 0.8 μm long FET gates. MIM capacitors, with plasma-enhanced CVD Si_3N_4 as a dielectric, were used for both rf tuning and bypassing due to a good control on capacitance per unit area with our process. Some yield data are presented later. A capacitance of 130 pF/mm^2 was obtained, although higher values were possible by thinning the dielectric layer. However, much higher values made the area of tuning capacitors so small as to jeopardize their reproducibility due to small variations in lithography. The fabrication process incorporated a two-level metallization scheme with 1.3 μm thick polyimide/Si_3N_4 crossovers for minimum parasitic capacitance between the two metallization levels. Wafer fabrication was done on 635 μm thick substrates (to minimize breakage), but before etching via holes from the backside, the substrates were thinned to 125 μm. Thinning was accomplished by a combination of lapping and polishing that left a mirror finish on the final surface. This aided in reducing rf losses in the microstrip ground plane, which was formed by metallizing the backside by an "electroless" process with a thin Au film and subsequently electroplating to increase the thickness of this ground plane metallization to 2 μm. Backside metallization also plated all the via holes, thereby providing ground points at appropriate locations on the chip. Transmission lines were constructed in the form of microstrips. Although coplanar and slot-line techniques have been used in the past, they consumed large chip areas and caused interconnection problems. The second metallization level that formed all the microwave circuitry, top plates of MIM capacitors and many interconnects was plated to a thickness of ~ 3 μm to minimize rf losses.
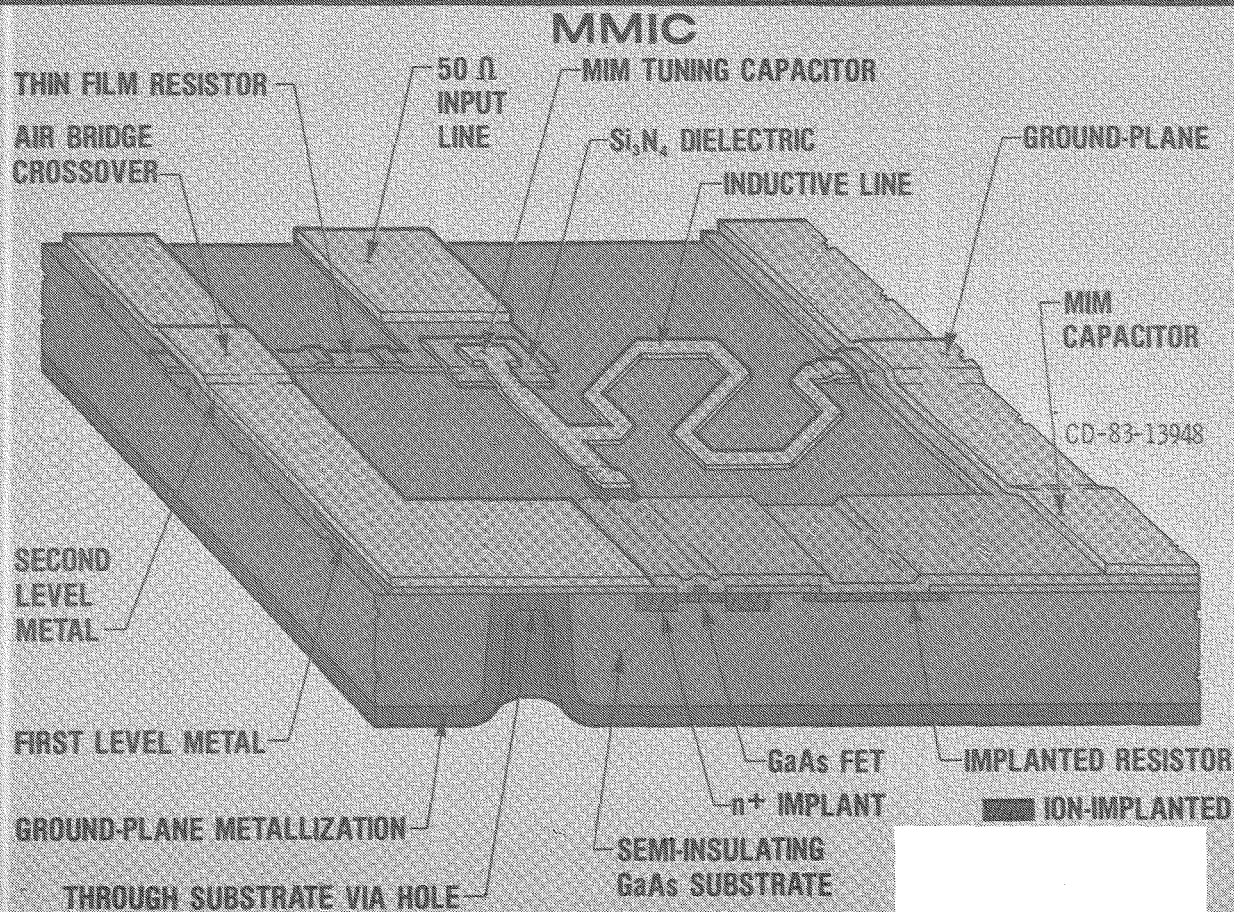
Fig. 51   Features of the MMIC technology developed at Rockwell and used on the NASA project.

Successful implementation of the MMIC technology required the use of advanced and innovative processing methods. The fabrication techniques provided high device yields and simultaneously satisfied the demands for state-of-the-art device performance. These considerations impacted the choices of materials technology, lithographic processes for fine-line pattern definition, etching techniques, metallization systems, interconnect methods and wafer thinning. A discussion of the processing sequence used is presented next.

5.1.2.1 MMIC Processing Sequence

A pictorial presentation of the sequence of steps involved in processing MMICs during this program is given in Fig. 52. As noted earlier, all patterning was done by contact photolithography. AuGe/Ni-based ohmic contacts were used and gate metal was Ti/Pt/Au. A Ti/Au overlap was placed on the ohmic metal to reduce resistance. Second-
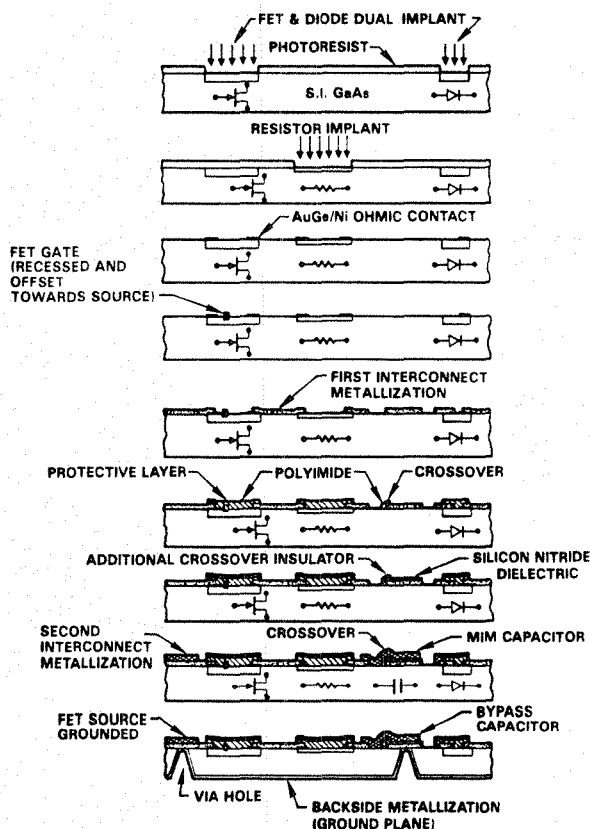
Fig. 52 The MMIC ion implant based fabrication process.

67

C9144D/sn

level metal was also Ti/Au, with the Au electroplated to a thickness of 3 μm. A two-level metallization scheme was used with 1.3 μm thick polyimide/Si_3N_4 crossovers. Final substrate thickness was 125 μm and via holes were chemically etched from the back using a photoresist mask (Fig. 53). After etching the via holes, the backside was first electro-less-plated with Pd and then electroplated with Au to a thickness of 2 μm.

5.1.3   Ku-Band GaAs FET Technology

At Rockwell, the device fabrication technology was developed using contact lithography.   FETs fabricated by this approach showed good performance through 21 GHz. The following steps were taken to improve the standard FET device:

SC20663
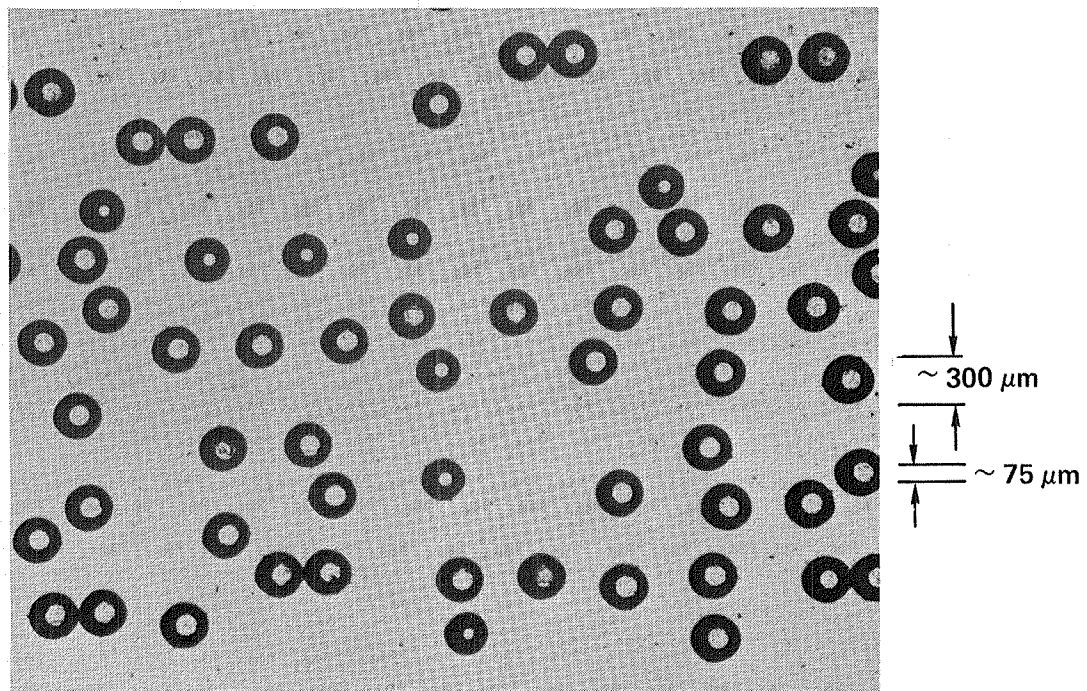
Fig. 53 Via holes etched through the substrate of an MMIC.

1. Low gate-source resistance was achieved by decreasing both ohmic contact and active layer sheet resistances. This was accomplished through the use of localized n^{++} implantation in contact regions and using a shallow n^+ surface layer in the channel region in conjunction with recessed gate techniques. In addition, the mask set was designed with the gate only 0.9 μm away from the edge of the source metallization, resulting in a tight alignment tolerance for contact lithography.

2. Electron beam lithography was used to direct write gates that have a very short gate junction length and yet have over 7000Å of metal thickness to keep resistance per unit gate width at a minimum.

3. Traps in the active device material were minimized by using high purity, in-house undoped LEC semi-insulating GaAs as the substrate material.

Typical I-V characteristics of a 200 μm wide device obtained by this technology are shown in Fig. 54. Note the low knee voltage which indicates low parasitic resistances.

5.2 Yield Experience

5.2.1 Introduction

MMICs have been under development at Rockwell for over eight years. The processing technology for fabricating these circuits, developed during this period, reached a level of maturity to produce routine circuits operating at frequencies in excess of 20 GHz approximately four years ago. Since then, the basic fabrication steps have been essentially unchanged, and process refinements have been made only as their advantages were verified. This baseline process has been used to fabricate circuits from different mask sets, labeled NASA-1, NASA-2, NASA-3 and NASA-3A. On all masks, there were 20 GHz circuits with devices of similar dimensions and alignment requirements. Wafers processed using these mask sets have been included in this yield study. The yield-limiting factors that have been investigated were selected from past experience as being the most important ones. They are: 1) wafers terminated in process (broken); 2) FETs; 3) MIM capacitors; 4) metal and dielectric adhesion; 5) wafer thinning; and 6) via holes.

WIDTH = 200 μm
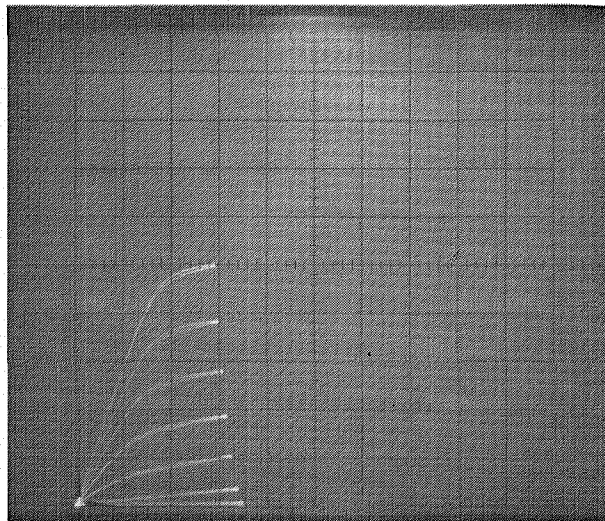
SCALE: VERTICAL 10 mA/DIV

HORIZONTAL 0.5 VOLTS/DIV

STEP SIZE: 0.5 VOLTS

$g_{mo} \cong 24$ ms(120 ms/mm)

$V_K \approx 0.8$ VOLTS

$V_p \approx 3.0$ VOLTS

Fig. 54 I-V saturation characteristics of a 200 μm wide MESFET.

5.2.2   Procedure

The following procedures were used to obtain quantitative estimates of the yield loss due to each of the yield-limiting factors. The first, wafers terminated in process, was investigated by reviewing the process followers and noting the reasons why processing of certain wafers was terminated. Measurements of FET dc yield were made by checking the I-V characteristics of test FETs in the test cell, using a Tektronix 576 curve tracer; these FETs are identical to the ones in use in the MMICs. In addition to gate yield, this test also revealed the cause of failure (broken or shorted gate) and allowed measurement of FET I_{dss} variations. For MIM capacitors, the capacitance per unit area was determined from capacitance measurements on small test capacitors using a Boonton Model 72BD capacitance meter. The dc yield was determined on capacitors used for bypass. This yield was measured simultaneously with via hold yield on a NASA circuit in which these components are interconnected, in such a configuration that it was possible

to isolate shorts. The integrity of bonding pads on MMICs was checked by a bonding test on chips from several wafers. A visual examination was made on a larger number of wafers to identify those with obvious metal or dielectric adhesion problems. Other problems, such as excessive chipping during the dicing operation, were also identified during this visual examination.

5.2.3   Results

A review of process followers indicated that over 150 wafers had been processed using the same fabrication process and the four mask sets mentioned earlier. The wafers were mostly 1 in. sq. or a quarter of a 3 in. wafer. The statistic on wafer completion was as follows:

1. Completed   61%
2. Not completed due to processing problems   21%
3. Not completed due to breakage   14%
4. Not completed due to equipment failure   4%

Yield loss of prematurely terminated wafers is thus 39%.

5.2.3.1   FET Gate Yield

The early process (pre-electron beam lithography) used contact photolithography and liftoff for the delineation of 0.7 μm long W-Au gates. Gate-source spacing was designed to be 0.9 μm. The dc characteristics of test FETs were measured on a curve tracer to identify bad devices. The most common failure mechanisms were found to be broken gates and gates shorted to the source. Two-hundred and fifty-three FETs 400 μm wide and 253 FETs 200 μm wide were tested for good dc characteristics with the following results:

FET Width	Good Devices	(%)
400 μm	168 out of 253	66.4
200 μm	165 out of 253	65.2

Of the failed devices, approximately equal numbers had gate-source shorts and broken gates (which includes "no gate"), indicating that these two problems are of equal importance. It is interesting to note that the measured FET gate yield appears independent of gate width. This result is unexpected, but is not expected to hold for significantly larger devices. It indicates that gate yield is limited by factors which are independent of gate width such as misalignment and poor mask-wafer contact in some areas during gate lithography, which results in large numbers of broken gates. Gate yield is also dependent on gate width, but this effect is small for the devices studied. Gate yield has improved markedly (to 90%) with the use of electron beam lithography for gate definition.

5.2.3.2 I_{dss} Uniformity

Microwave FETs use recessed gate technology which involves etching the channel below the gate until a specified maximum channel current is reached. This was done in our process by wet chemical etching. Device current uniformity over a wafer is usually degraded by this step when compared with current uniformity before gate recess. Typical results measured on a large number of wafers were:

Condition	$\Delta I_{max}/\langle I_{max}\rangle$
1. Before gate recess	±6% (2σ)
2. After gate recess	±20% (2σ)

Reproducibility of $\langle I_{max}\rangle$ is ~ ±25%.

5.2.3.3 MIM Capacitors

Uniform and Reproducibility. The capacitance of three small capacitors in the test cell was measured for ten chips each from 18 wafers (540 measurements). Average uniformity across a wafer for all three capacitors was found to be 4% (2σ). Reproducibility over the 18 wafers was as shown in Table 4.

Table 4

Reproducibility over 18 Wafers

Capacitor No.	Capacitor Area	Measured Capacitance Average (pf)	σ (2)
1	4×10^{-3}	0.634	5.3%
2	6.85×10^{-3}	0.814	5.1%
3	2×10^{-2}	2.95	4.9%

Based on the area of Capacitor 1, the average capacitance per unit area that has been obtained is 126.8 pF/mm^2. The target was 130 pF/mm^2. The capacitance of these three capacitors does not scale according to their area. This effect was due to stray capacitance associated with capacitor periphery and is geometry-dependent. Detailed modeling of this effect is being carried out. The results will be used for more accuracy in circuit designs.

Bypass Capacitors. The dc yield of a 15 pF bypass capacitor was measured by testing 175 capacitors, obtaining an overall yield of 86%. This capacitance value is the largest used in circuits; more commonly, a value of 10 pF is used for bypassing. Smaller capacitors have a higher yield, given by the approximate formula:

$$\text{Yield} = 1 - 0.14 \frac{C}{15} \times 100\%$$

where C is in pF. Thus, e.g., anticipated yield for 10 pF capacitors was 91% and 99% for 1 pF.

5.2.3.4 Metal/Dielectric Adhesion

Bonding pad adhesion was checked on 30 wafers. A chip from each wafer was mounted on a ceramic substrate and Au wires were bonded to each pad. 56.7% of the wafers passed this test with no pad adhesion problem. Of the remainder, 40% showed poor adhesion at the Ti/Au interface of second-level metallization, and 3.3% showed poor adhesion at the GaAs/Ti interface (first-level metallization). The bonding pads were formed by first depositing a layer of first-level metallization and then increasing its thickness by depositing another layer of second-level metallization on top.

5.2.3.5   Chip Thickness

MMIC processing was carried out on 25 mil (635 µm) thick substrates which were thinned to a nominal thickness of 5 mils (127 µm) by backside lapping and polishing prior to via hole etching and ground plane plating. The flatness of a wafer after polishing and average thickness after the thinning operation were measured. The thickness of ten chips each from 37 wafers was measured to an accuracy of ±0.1 mil. The results are:

Average thickness after backside processing:	4.7 mils with σ = 0.5 mils
Average flatness across a wafer:	±0.3 mils

5.2.3.6   Through Substrate Via Holes

Via holes were tested for electrical continuity between the top electrode and the ground plane. Of 548 via holes tested, 95% were good.

5.2.4   Projections of Anticipated Yield for Three-Inch Wafer Processing

The early MMIC process was a laboratory process used to fabricate developmental circuits in small quantities in an R&D laboratory. Subsequent to the work and period that is the subject of this report, a Rockwell production facility for MMICs was established. This facility employs production techniques similar to those used in the silicon industry, which are optimized for high yield and volume. Moderate quantities of MMICs for near-term program demonstration needs are produced with substantially higher yields than within our R&D laboratory by incorporating certain changes in process steps:

1.   Changes in wafer handling techniques have been introduced which reduce the incidence of wafer breakage. In a production facility, wafer handling is considerably reduced through the use of automated equipment and breakage is not a problem in production.

2.   Improvements in yield come by using 3 in. diameter wafers (instead of the smaller wafers used for this program). This increase in wafer size reduces

the proportion of chips near the wafer edge, which are more likely to get damaged through wafer handling.

3. The gate definition is accomplished by a new technique (presented in simple form in Fig. 55) which has already demonstrated a high yield of sub 0.5 μm gate lengths through the use of optical lithography. For 0.25 μm gate length (or less), the use of electron beam lithography is retained.

4. For lithographic steps other than FET gates, a Censor DSW (10X) alignment machine is used. This approach reduces defects generated by hard contact of mask and wafer as occurs in contact mask aligners. Thus, MIM capacitor yield is also improved with the use of projection printing.

5. A better understanding of the reasons for poor adhesion process has changed yield for the better.

6. The via hole process is considerably improved. Although via hole yield is high (95%), the current process requires a highly skilled operator. Process changes are aimed at improving the yield further and making it easier to implement. Concurrently, new etches are being investigated to speed up the process. Current developments are in the area of dry etching processes to further improve yield and reduce the required operator skill of this step.

As more experience was gained with this fabrication technology, the number of process-related failures have been reduced. Process refinements incorporated in the process sequence have raised yield. A comparison of "old" yield vs current yield for 3 in. diameter wafer processing is given in Table 5.

A copy of the report/proposal to NASA, Lewis Research Center of June 22, 1987 giving details of Pilot Line yields and the production of MMIC components at that facility is attached to this report as an Appendix.

IMRDC85-30968

PHOTORESIST

SUBSTRATE

|←0.8 μm→|

**a. DEFINE A 0.8 μm
LONG POSITIVE
PHOTORESIST STRIPE
USING A LIGHT
FIELD MASK**

ORIGINAL
RESIST PROFILE

FINAL
RESIST PROFILE

|0.5 μm|←

**b. ISOTROPICALLY ETCH
THE PHOTORESIST
BY 0.15 μm
IN A HIGH
PRESSURE PLASMA**

DIELECTRIC

**c. DEPOSIT DIELECTRIC
AND PATTERN
BY LIFTOFF**

PHOTORESIST

|←0.8 μm→|

**d. EXPOSE PHOTORESIST
USING A DARK FIELD
GATE MASK.
GATE OPENING
WILL BE ~0.8 μm**

T-BAR
Ti-Pt-Au
GATE

**e. EVAPORATE Ti/Pt/Au
AND PATTERN
BY LIFTOFF.
RECESS GATE
IF NECESSARY**

Fig. 55   An optical lithography technology for the realization of sub 0.5 μm gate length FETs.

Table 5

Comparison of Old Yield vs Current Yield for 3 in. Wafers

Item	Old R&D Yield or Uniformity	Pilot Line Yield or Uniformity for 3 in. Processing
Wafers Completed	61%	> 85%
FETs		
1. Gate (w = 400 µm)	66%	> 95%
2. I_{dss} Uniformity Across a Wafer	±20%	±15%
3. I_{dss} Reproducibility	±25%	±20%
MIM Capacitors		
1. Reproducibility	±10%	±10%
2. DC Yield (15 pF)	86%	> 90%
Metal Adhesion	57%	> 90%
Via Holes	95%	> 95%
Chipping	90%	> 99%
Representative Complex Large-Scale MMIC with 5-Bit Phase Shifter and 5-Stage Amplifier (dc yield)	3.5%	> 20%

6.0 CONCLUSIONS

Although the program took much longer than originally planned, a complete development of a transmit module (power amplifier and five bits of phase shift) has been accomplished. The modules work very satisfactorily.

The process is now available in the Rockwell Pilot Line. There, similar MMIC technology is producing similar ICs for phased arrays with very high rf "good" yields.

Rockwell is justifiably proud of this accomplishment of realizing a practical MMIC technology with implanted MESFETs. It is a salient fact that this NASA program was a contributory factor in the assembly of this valuable capability.

7.0 REFERENCES

1. J.B. Benet, "The Design and Calibration of a Universal MMIC Test Fixture," IEEE 1982 Microwave and Millimeter-Wave Monolithic Circuits Symp. Digest of Papers, June 18, 1982.

2. W.C. Petersen and A.K. Gupta, "A Two-Stage Monolithic Buffer Amplifier for 20 GHz Satellite Communications," Proc. 1983 IEEE Microwave and Millimeter-Wave Monolithic Circuits Symp., pp. 37-39, May 1983.

3. W.C. Petersen and A.K. Gupta, "A Three-Stage Monolithic Amplifier for a 20 GHz Transmit Module, " Proc. 1983 IEEE Microwave and Millimeter-Wave Monolithic Circuits Symp. Tech. Digest, pp. 119-122, October 1983.

4. A.K. Gupta, W.C. Petersen and D.R. Decker, "Yield Considerations for Ion-Implanted GaAs MMICs," IEEE Trans. Elect. Dev. ED-30 (1).

5. J.A. Higgins and R.L. Kuvås, "Analysis and Improvement of Intermodulation Distortion in GaAs Power FETs," IEEE Trans. on Microwave Theory and Technique MTT28 (1), 9 (1980).

APPENDIX

20 GHz MONOLITHIC TRANSMIT MODULE

20 GHz MONOLITHIC TRANSMIT MODULE

Contract No. NAS3-23247

TECHNICAL PROGRESS NARRATIVE

For the period September 1, 1986 to June 1, 1987

J. A. Higgins

Rockwell International Science Center
Thousand Oaks, CA 91360

Prepared for:

NASA Lewis Research Center
Cleveland, OH 44135

Introduction

The subject contract is one in which Rockwell undertook to design, fabricate, and supply prototype quantities of two different MMIC chips for NASA LeRC. The chips in question are: (a) 17 to 20 GHz Transmit Amplifier with constant gain (CGA) and (b) 17 to 20 GHz Variable Phase Shifter (VPS). The program was transferred to the Science Center (Corporate Research Laboratory) on October 1, 1986 and since that time has been dormant. The reason for this period of inaction has been that the program had been completed as far as the design and fabrication of test samples, which illustrated the required performance, but had insufficient funds remaining to complete the production of the deliverables. These deliverables are 100 of each type of chip.

The proposed plan, which has been followed, was to await the insertion of the MMIC production capability into the Rockwell GaAs Pilot Line which was to proceed independent of any external program (on internal funds). When a high level of confidence for the MMIC process in the Pilot Line was established, then Rockwell would propose to NASA that the subject contract be completed by the fabrication of the deliverable chips in the Pilot Line facility. That time has now come and what follows in the nature of a status report, an estimate of the extra funds necessary to be added in order to complete and a proposal to complete the program. The current funding level is $1,021,068 of which there remains a balance at this point of $16,000.

It will be seen in what follows that there is now little doubt that this contract can be completed very successfully. A high yield process is available to produce the 100 deliverable chips of each type. 100% testing of 110 chips of each type and delivery of all the wafers and materials will be accomplished in an eight month period, if the extra funds are added. This amount is provided in Appendix 1 of this report.

Status Report on Pilot Line Processing

A baseline process has been established at the Rockwell Pilot Line for fabricating 20GHz MMICs on 3-inch GaAs wafers. Wafers are processed in lots of 10 using a CENSOR SR-100 direct-step-on-wafer mask aligner for all lithography operations except via hole masking. This includes the 0.5 micron FET gate fabrication step. Via hole lithography is done on a 1X mask aligner fitted with infrared optics. All backside processes which include wafer thinning, via hole etching, and ground plane plating are performed on whole 3-inch wafers, i.e. wafers are not "quartered" for these steps. This baseline process is very similar to the process developed at the Science Center. It uses direct, localized ion-implantation, $0.5\,\mu m$ gate length FETs, M-I-M capacitors, and through-substrate via holes. The differences are gate lithography is performed optically instead of by electron-beam-lithography, and some changes have been made to account for the absence of polyimide from the pilot line process. There are no organic substances present on these MMICs.

The test vehicle used for process development was a mask set that contains a 20 GHz 3-bit receive MMIC. A photograph of the chip is shown in Fig.-1. It consists of a low noise amplifier, a buffer amplifier, and 3 phase shifter bits. Except for the LNA, other circuit elements are similar to those used on

the NASA3 VPS chip. Six lots were processed initially to establish the baseline fabrication process. Since then five more lots have been processed

for the Air Force MANTECH Program (Contract# F33615-85-C-5064). Frontside processing and backside processing of two of these lots is complete; the remaining will be completed within a month. Backside processing of lots in the Pilot Line can proceed only after extensive parametric characterization, which is currently in progress.

The experience with these lots indicates that the process is well under control. The table in Fig.2 illustrates how tight this control is. For the data shown there is parameter data of discrete transistors fabricated alongside the MMICs and then measured at 20 GHz in the wafer probe stage. The standard deviation of all of these 20 GHz S-parameters are held to less than 10% This is a sign of readiness to produce in quantity.

The major RF yield limiting factor is variation in FET gate length. In-process SEM inspections have been instituted to keep this parameter under tight control. On the first MANTECH lot, DC yield of the buffer amplifier ranged from 43% to 95%.

RF Performance Data

The performance is similar to that of the prototype MMICs fabricated in the research facility with 0.5 micron gates defined by EBL. The amplifier gains are higher with gain for the entire chip i.e. signal passing through the amplifier and the three phase shifters, being between 5 and 13 dB. This gain is seen in Fig. 3. The variation in gain is thought to be due mostly to the Phase shifter circuits. The phase shifter insertion loss is increased by 0.9 dB per phase shifter. The added loss is due to extra loss in the switches of the phase shifters due to a slightly increased gate to ohmic capacitance in the switch FETs. The total loss through the VPS is therefore close to 11 or 12 dB.

The phase shift of the VPS chip in all eight modes is seen in the Fig. 3, and the variation of the insertion loss around a mean value for all eight states is seen in Fig. 4. The group delay of these amplifier/phase shifter circuits is measured as being less than 1 nsec in a parabolic distribution over the band 17 to 20 GHz. Although sufficient data have not yet been collected to determine the RF yield of the 3-bit receive chip, it is expected to be >25% based on the experience during process development.

Pilot Line Yield Predictions

The results obtained thus far are very encouraging. The baseline process is stable and reproducible due to extensive automation of the processing equipment. The experiments currently in progress are aimed at making this MMIC fabrication process even more manufacturable. We feel that the processing technology is now ready to fabricate 100 units each of the variable-phase-shift (VPS) and the constant-gain-amplifier (CGA) MMICs for which the NASA3A mask set was designed. Early processing efforts at the Science Center using this mask set on 3-inch GaAs wafers indicated that RF yields of the VPS and CGA chips can be as high as 10% and 75%, respectively.

2

The lower yield of the VPS chip implies that it must be used to estimate the total number of wafers that must be processed. For this estimate we may assume that the highest yield obtained at the Science Center will equal the average yield at the Pilot Line due to the better processing equipment available there. Since there are 44 VPS and CGA circuits per 3-inch wafer, a total of 23 wafers must be processed to obtain 100 functional VPS MMICs. Assuming a 10% loss in packaging, a total of 26 wafers or 3 lots must be processed to obtain 100 packaged VPS MMICs. These lots should also provide enough chips to obtain 100 packaged functional CGA MMICs.

REVISED STATEMENT OF WORK

The various tasks that must be performed to obtain the required MMICs are summarized in this section. A schedule is shown in Fig.-6. Tasks 3 and 4 are optional.

TASK 1: Revise mask set

The NASA3A mask set must be modified to account for the pilot line process. Four new mask plates will be required. This task will cover the CAD and procurement of these layers.

The mask set will be delivered to NASA at the end of this program.

TASK 2: Lot Fabrication

Three 10-wafer lots will be fabricated using the modified NASA3A mask set. Parametric measurements at the wafer level and DC functional measurements of the diced chips will be carried out. A sample of five each VPS and CGA MMICs from each lot will be RF tested at the chip level.

All tested devices will be delivered with data. All wafer and device residuals will be delivered if so desired by NASA.

TASK 3: 100% RF Testing (optional)

RF testing of 110 each, VPS and CGA MMICs will be carried out at the chip level. These chips will be selected based on the DC functional testing carried out in Task 2. The CGAs will be tested under small signal conditions. The VPSs will be tested in the reference state and in five other states corresponding to 180, 90, 45, 22.5, and 11.25 degree phase shift, respectively. The number of MMICs selected for this task assumes a need for an extra 10% functional chips due to packaging losses.

All tested devices will be delivered with data. All residuals, wafers, and devices will be delivered, if so desired by NASA.

TASK 4: RF Packaging (optional)

100 each CGA and VPS chips will be packaged in packages provided by NASA.

All packaged devices will be delivered to NASA. All wafer and device residuals will be delivered to NASA.

TASK 5: A Final Report summarizing the entire program and covering in detail the activity from the beginning of mask NASA3, which is the final mask set of this project, through to the present will be written and delivered to NASA-LRC.

A schedule for the performance of these tasks is shown in Fig.-6.

4

FIGURE CAPTIONS

Fig. 1 The Low Noise Receiver and three bit phase-shifter chip. This circuit is designed to provide a 10 dB through Gain, a 4 dB noise figure and three bits of phase shift between 17 and 20 GHz. The chip is 1. mm by 3.5 mm and .125 mm thick.

Fig. 2 A table providing the Idss,current gain bandwidth, and S-parameters for one three inch wafer processed in the Pilot Line. Tight control is amply shown by the small sigma values.
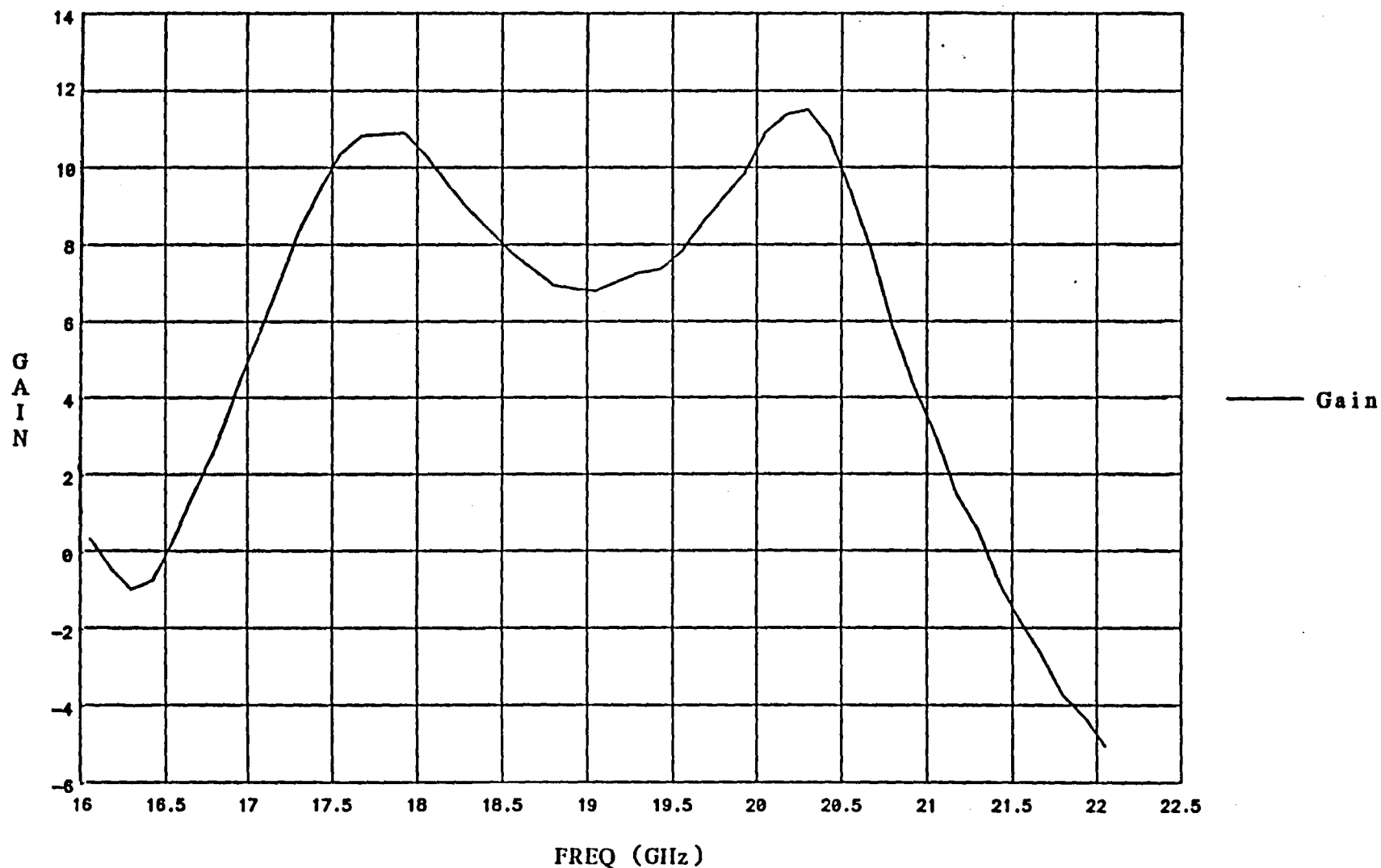
Fig. 3 The through gain of these modules has been measured showing a maximum of 13 dB and a minimum of 4 dB.

Fig. 4 The phase shift against frequency for all eight states.

Fig. 5 Variation of gain about a mean state for all phase states.

Fig. 6 A fabrication and test schedule for the finish-it-off activity proposed by this report.

APPENDIX I

Subject: *Budgetary and Planning Estimate*

Reference: Statement of Work in Status Report for Contract No. NAS3-23247

The contractor provides herein its budgetary and planning estimate to complete the referenced statement of work.

Budgetary and Planning Estimate: $244,000

The estimate set forth herein is submitted for budgetary and planning purposes only and does not constitute a firm commitment on the part of the Rockwell International Corporation.

If further information is required, please contact D. H. Graves or the undersigned at (805) 373-4581 and 373-4415 respectively.

ROCKWELL INTERNATIONAL CORPORATION
Science Center

R. A. Johnson, Director
Contracts and Pricing

G.O. 5492

Fig. 1 - The Low Noise Receiver and three bit phase-shifter chip.
This circuit is designed to provide a 10 dB through Gain, a
4 dB noise figure and three bits of phase shift between 17
and 20 GHz. The chip is 1. mm by 3.5 mm and .125 mm thick.

Fig. 2 – A table providing the Idss, current gain bandwidth, and S-parameters for one three inch wafer processed in the Pilot Line. Tight control is amply shown by the small sigma values.

Gain of RCVR_37070_001_72

FREQ (GHz)

Figure 3 - The through gain of these modules has been measured showing a maximum
of 13 dB and a minimum of 4 dB.
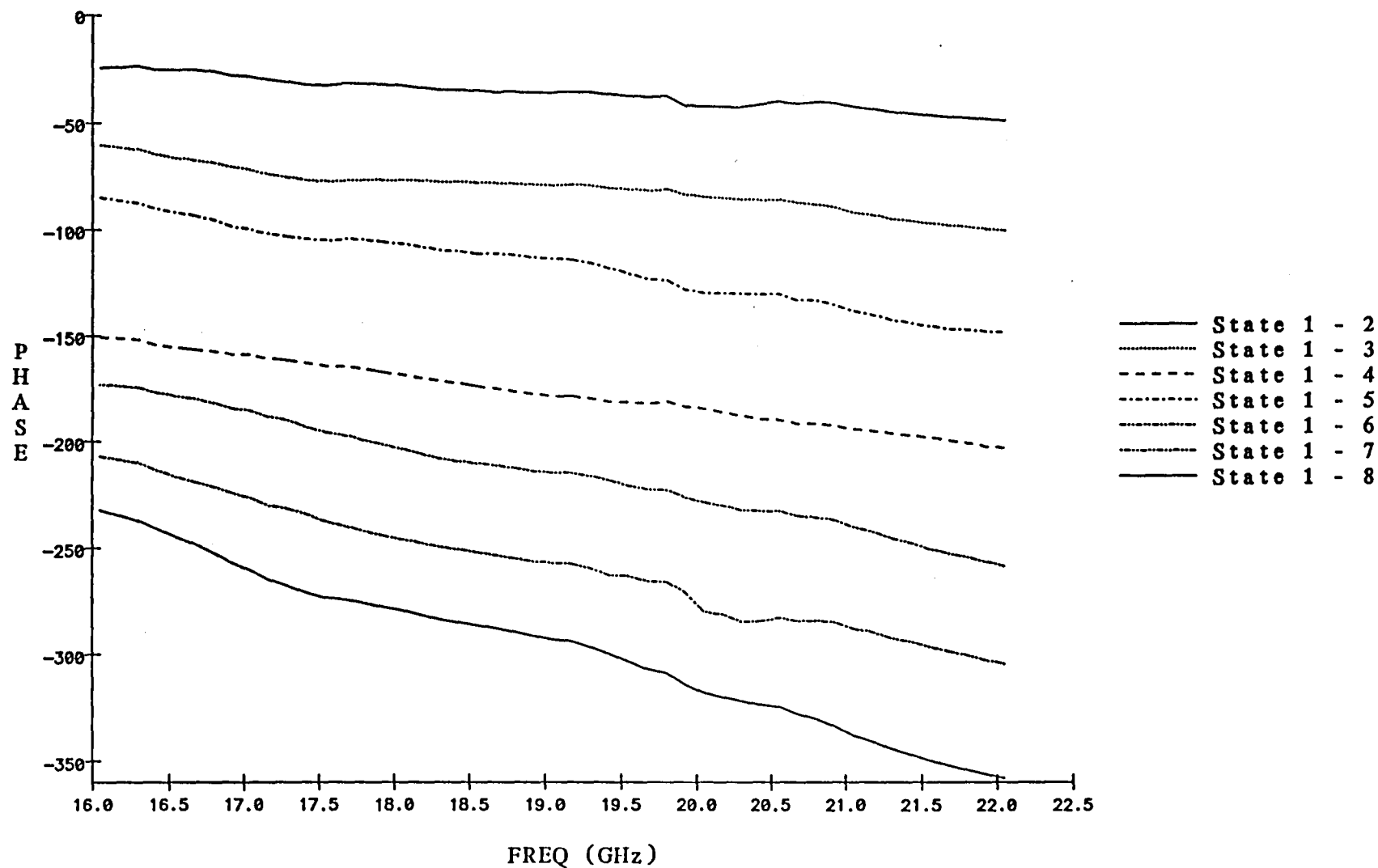
PHASE SHIFTS of RCVR_37070_001_72_4_

Figure 4 - The phase shift against frequency for all eight states.
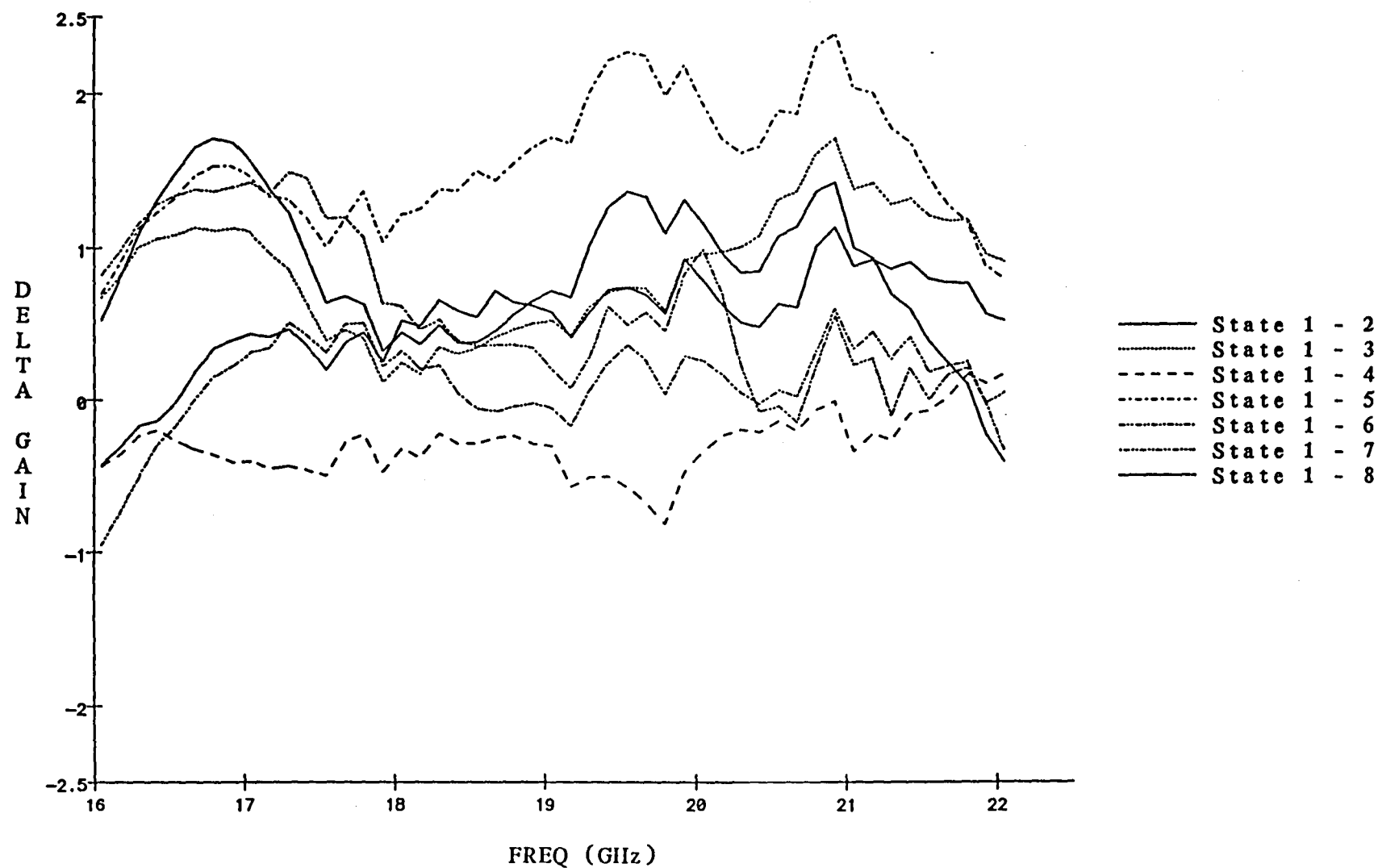
DELTA Gain of RCVR_37070_001_72_4_

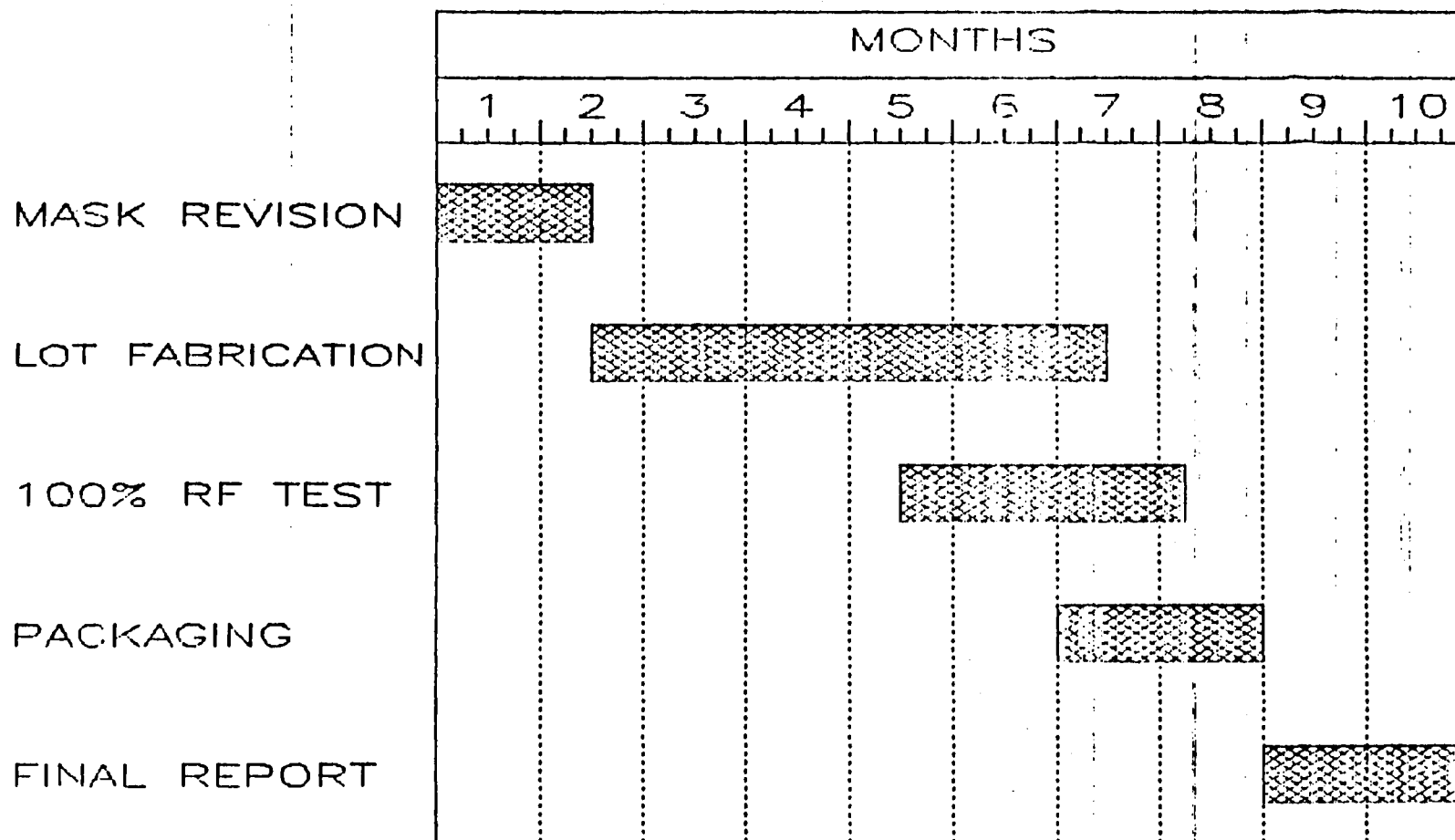Figure 5 - Variation of gain about a mean state for all phase states.

Figure 6 - A fabrication and test schedule for the finish-it-off activity
proposed by this report.

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