Power Hardware-in-the-Loop-Based Anti-Islanding Evaluation and Demonstration

Karl Schoder, James Langston, John Hauer, Ferenc Bogdan, and Michael Steurer
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Technical Report
NREL/TP-5D00-64241
October 2015

Contract No. DE-AC36-08GO28308

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Final Report

April 2015

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April 2015

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Executive Summary

The National Renewable Energy Laboratory (NREL) teamed with Southern California Edison (SCE), Clean Power Research (CPR), Quanta Technology (QT), and Electrical Distribution Design (EDD) to conduct a U.S. Department of Energy (DOE) and California Public Utility Commission (CPUC) California Solar Initiative (CSI) -funded research project investigating the impacts of integrating high-penetration levels of photovoltaics (PV) onto the California distribution grid. One topic researched in the context of high-penetration PV integration onto the distribution system is the ability of PV inverters to (1) detect islanding conditions (i.e., when the distribution system to which the PV inverter is connected becomes disconnected from the utility power connection) and (2) disconnect from the islanded system within the time specified in the performance specifications outlined in IEEE Standard 1547. This condition may cause damage to other connected equipment due to insufficient power quality (e.g., over-and under-voltages) and may also be a safety hazard to personnel that may be working on feeder sections to restore service. NREL teamed with the Florida State University (FSU) Center for Advanced Power Systems (CAPS) to investigate a new way of testing PV inverters for IEEE Standard 1547 unintentional islanding performance specifications using power hardware-in-loop (PHIL) laboratory testing techniques.

The first project objective was to evaluate the suitability of PHIL laboratory testing techniques for performing IEEE Standard 1547/UL 1741 unintentional-islanding tests and to compare the results to traditional testing techniques that require highly specialized resistive, inductive, and capacitive discrete load banks. The second objective was to utilize the flexibility inherent in PHIL simulation techniques for establishing alternate rest-of-system (RoS) conditions to demonstrate the unintentional islanding performance of a PV inverter when connected to alternate circuits and conditions. These two objectives were investigated with alternative PHIL simulation approaches and were intended to determine testing feasibility.

The traditional unintentional islanding test methods bear several challenges. First, once islanded, the solar PV inverter tries to destabilize the system to allow it to detect the islanding conditions. As a result, the system is inherently unstable and test results cannot be reproduced in the common sense. Only patterns of behavior may emerge and allow comparison of alternate test approaches. Second, the resonant resistive-inductive-capacitive (RLC) load bank is prone to cause high levels of harmonic currents in cases where the supply voltage contains harmonic components. Furthermore, the supply voltage harmonic content may depend on the day and time of the day, and therefore cause different levels of harmonic currents to be recorded in experiments before islanding. Third, the discrete RLC load bank components are not ideal and have tolerances that will lead to mismatched resistive and reactive power components. The PHIL approach does not have this limitation; the experimenter can perfectly match ideal inductive and capacitive components, and even change component values during operation, thereby greatly reducing the time it takes to modify test conditions.

The adequacy of the RLC load-based testing for unintentional islanding has been questioned many times—as has the corresponding quality factor or range of quality factors. Points under debate have included methods of estimating realistic load parameters, as well as the possibility of including induction motor loads in tests. However, implementation of alternative test conditions has mainly been hindered by the difficulties of ensuring comparable test setups.

In this unintentional islanding test project, we succeeded in applying the PHIL approach in a wide range of RoS model cases. The PHIL tests performed were stable for quality factors above one, but they did not perform well under conditions of low quality factor or low power levels. Improving implementation aspects of the PHIL interfacing algorithms could partly increase the stable operating regions, but not all limitations could be overcome. The difficulties are due to inherent limitations imposed by the hardware (i.e., primarily the power amplifiers, communication delays, and control bandwidth limitations). We demonstrated that the PHIL simulation approach offers flexibility and efficiency in establishing alternate test conditions, which, consequently, opens the door to cost-effectively probe for proper islanding mechanisms. In addition, the PHIL simulation approach can be used to determine whether methods other than RLC load bank-based RoS conditions are of concern. In the scenarios we tested, the possibility of extended islanding conditions, with larger induction machines as part of the island, were confirmed, which indicates that the load bank alone is not sufficient for operation under conditions that can realistically be expected as part of a distribution feeder.

The positive outcomes of this systematic exploration of using the PHIL simulation approach to test for unintentional islanding are encouraging. As the current standard requirement in unintentional islanding testing concerns quality factors of and about one, which could not be reached in a broad enough set of test scenarios, further investigations into improving PHIL interface algorithms and requirements on power amplifiers are warranted. Also supported by the PHIL concept are investigations of issues concerning inverter interfaced generation resources with advanced controls that are expected to be of concern in high-penetration situations.

Selected tested conditions have shown that evaluations using methods other than RLC load banks, as the RoS models do make detection of island situations more difficult. These conditions were based on assumptions for models of other power electronic devices and motors connected to the islanded system. Additionally, the following investigations should be conducted to address the concerns raised:

1. Determine the risk of extended islanding conditions—and test for viable alternate conditions—under conditions of unmatched active and reactive power levels.
2. Identify corresponding RoS models that unify and standardize test conditions.
3. Improve PHIL simulation technology and interface algorithms.
4. Initiate modeling and simulation standardization efforts that incorporate and support requirements for PHIL simulation-based modeling.

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Terminology and Acronyms

AC	alternating current
AI	anti-islanding
CAPS	Center for Advanced Power Systems
DAQ	data acquisition system
DIM	damping impedance method
DQ	direct and quadrature (frame axis)
DUT	device under test
DC	direct current
FFT	fast Fourier transformation
ITM	ideal transformer model
MPPT	maximum power point tracking
MVA	megavolt ampere
NREL	National Renewable Energy Laboratory
PCC	point of common coupling
PEBB	power electronics building blocks
PHIL	power hardware-in-the-loop
pu	per unit
Qf	quality factor
RLC	resistive-inductive-capacitive (load bank)
rms	root mean square
RoS	rest–of-system
RTS	real-time simulator
VVS	variable voltage source

1 Introduction and Objectives

The National Renewable Energy Laboratory (NREL) teamed with the Florida State University (FSU) Center for Advanced Power Systems (CAPS) to investigate a new way of testing photovoltaic (PV) inverters for the IEEE Standard 1547 unintentional islanding (also referred to herein as anti-islanding) performance specifications using power hardware-in-the-loop (PHIL) laboratory testing techniques.

NREL is leading a U.S. Department of Energy (DOE) and California Public Utility Commission California Solar Initiative-funded research project investigating the impacts of integrating high-penetration levels of PV onto the California distribution grid. NREL has teamed with Southern California Edison, Clean Power Research, Quanta Technology, and Electrical Distribution Design to complete this research project. One topic being researched in the context of high-penetration PV integration onto the distribution system is the evaluation of the ability of PV inverters to detect islanding conditions[1] and disconnect from the islanded system within a period mandated by the performance specifications outlined in IEEE Standard 1547.

The primary project objective was to compare the suitability of PHIL laboratory testing techniques to perform IEEE Standard 1547/UL 1741 unintentional islanding type tests with traditional testing techniques, which require highly specialized resistive, inductive, and capacitive discrete load banks. The second objective was to utilize the flexibility allowed by PHIL simulation techniques in establishing alternate rest-of-system (RoS) conditions to demonstrate the anti-islanding performance of a PV inverter when connected to alternate circuits and conditions. These two objectives were investigated with alternate PHIL simulation approaches, and they were intended to determine feasibility and identify stability regions.

Sections 2-7 provide background information on unintentional islanding, the PHIL concept, test facility, real-time simulation, and test facility and equipment. Sections 8–13 summarize efforts undertaken in preparing, performing, and evaluating the unintentional islanding tests. Sections 13 and 14 provide a discussion of salient experience gained and concluding remarks.

[1] Island conditions occur when a PV inverter becomes disconnected from a utility power connection.

2 Unintentional Islanding

The term unintentional islanding refers to the possibility that distributed resources keep operating after being disconnected from the utility's distribution feeder. Unintentional islanding may damage connected equipment because of insufficient power quality (e.g., overvoltages and undervoltages). It also represents a potential safety hazard, as personnel may be working on feeder sections to restore service. To counteract the possibility of sustained islanding conditions, a special unintentional islanding test was devised as part of the IEEE Standard 1547 series [1]. This type test is specified in IEEE Standard 1547.1[2], and it has to be successfully passed as one of many tests by, for example, solar PV inverters, before they can be certified as 1547-compliant. Many states require IEEE Standard 1547 as requirement for interconnected distributed resources, and the importance of this test cannot be underestimated.

The test itself is based on a simple parallel resonant resistive-inductive-capacitive (RLC) circuit. This RLC load bank is tuned to be resonant at 60 Hz (and with small variations permitted for additional test conditions). Figure 1 depicts the test setup as used for solar PV inverters. The figure shows the AC grid source (emulator), and the switch used to initiate the islanding conditions (separating the AC grid from the solar PV inverter). The RLC load bank is wye-connected with an accessible neutral point as the solar PV inverter is a three-phase, four-wire system; the solar PV inverter is under test; and, a controllable DC source as multiple operating points are to be tested.

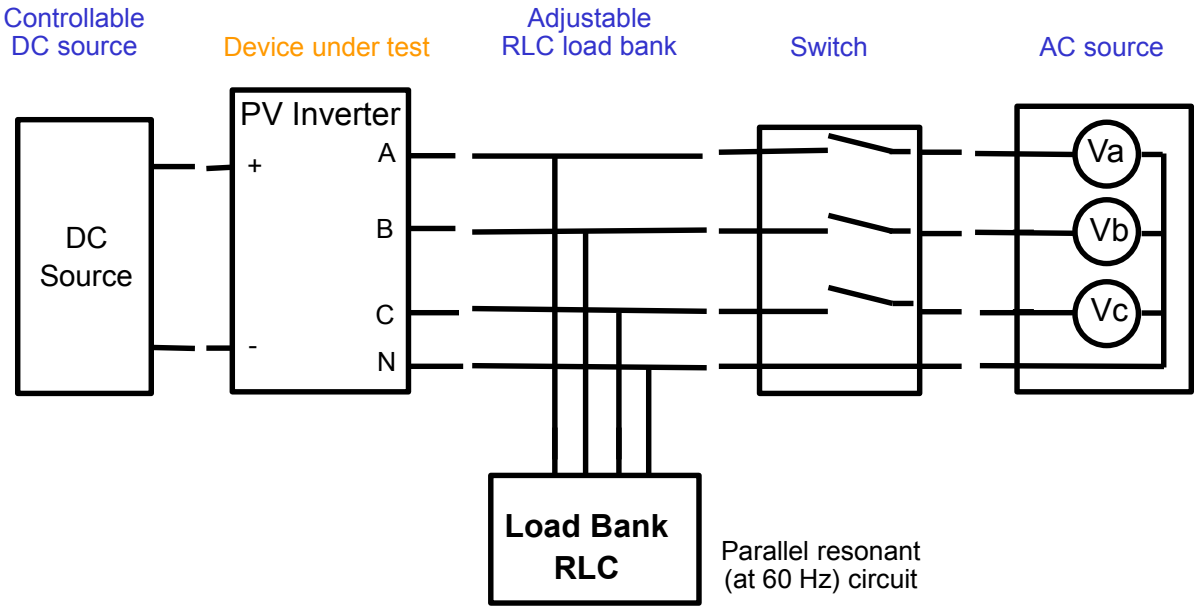


Figure 1. Unintentional islanding test setup (IEEE Standard 1547.1)

The test procedure is to island the solar PV inverter with the load bank by opening the switch. IEEE Standard 1547 requires the inverter to detect the islanding condition and stop energizing the circuit within two seconds. The costs of testing using RLC load banks are high, as load banks used in the tests must be frequently rebuilt to match the rating of the device under test. This is partly due to the availability of PV inverters with a wide range of ratings and partly because larger-capacity PV systems are being interconnected in increasing numbers.

3 Power Hardware-in-the-Loop Concept

This section briefly introduces the PHIL concept and current state-of-the-art applications. The conceptual PHIL setup is depicted in Figure 2. The main (hardware) components involved are a real-time simulator (RTS), a power amplifier, and the device under test (DUT; in this case, an inverter). The DUT's power terminals are connected to the power amplifier and during the PHIL simulation, they experience conditions similar to those when operated in the field under actual system conditions. To emulate system conditions, an RTS simulates in real time the rest of the system together with the power-interactions of the device under test. The DUT may be modeled as a current or voltage source, and the corresponding voltages and currents represent the device-system interface. The true replication of the currents and voltages is achieved through the PHIL interface. The interface conditions and controls information exchanged allow the amplifier's power stage to create the RoS conditions and fed back the DUT response into the real-time simulation of the RoS, operating the overall system as a closed loop for a true PHIL simulation experiment.

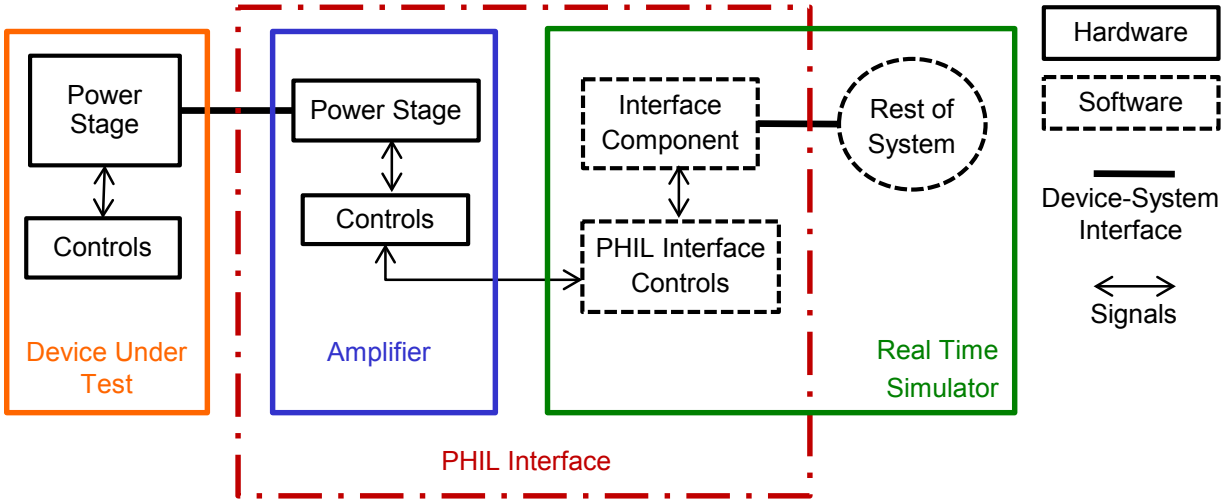


Figure 2. PHIL simulation concept

As an application example, Figure 3 shows the PHIL simulation concept as used for testing solar PV inverters on the AC-side. In the case shown, the solar PV inverter is represented as a current source in the real-time simulated model. The voltages of the RoS conditions are controlled and replicated by the power amplifier at the terminals of the DUT. This process may include filters to eliminate high-frequency components that cannot be truly replicated by a bandwidth-limited power amplifier. The power amplifier shown here is of variable voltage source (VVS) type, establishing the (three-phase) voltages through an intermediate transformer to match the voltage level of the DUT.

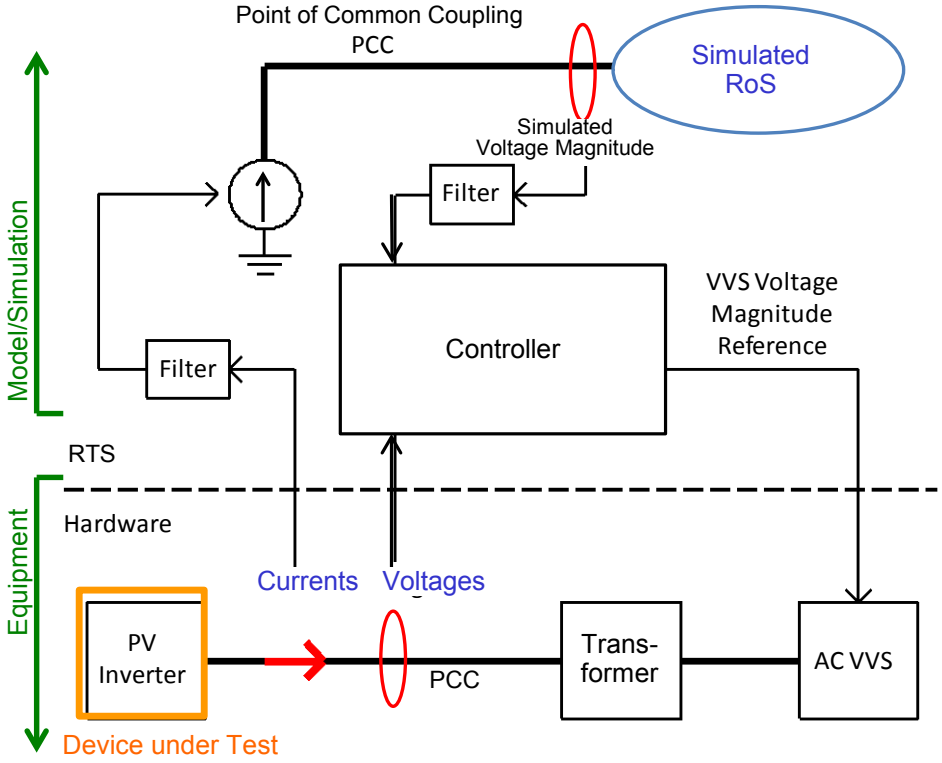


Figure 3. PHIL simulation for solar PV inverters (AC-side)

Recent applications of PHIL simulation with respect to power electronics converters have involved subjecting large inverters (up to the megawatt level) to RoS conditions, including steady-state operation, abnormal voltage and frequency, and distribution feeder interaction, to probe for possible consequences of active advanced inverter control functions [3]. The PHIL concept has also been applied in the context of commissioning a test setup systematically [4]. A reported effort in applying PHIL simulation in unintentional islanding tests is given in [5], which successfully examined the behavior of 3-kW single-phase inverter units. The intention of the project reported herein was to broaden the test conditions relative to the current RLC load bank-based tests, investigate alternate PHIL interface algorithms, and determine stability regions.

4 Test Facility

This section provides an overview of some of the facilities used to perform the PHIL experiments at CAPS. The facility shown in Figure 4 is based on a 5-MW power electronics-based VVS. The VVS can be split into two parts: 2.5 MW AC and 2.5 MW DC. The nominal AC-voltage output is 4.16 kV at 60 Hz but a 1.5-megavolt ampere (MVA) transformer is available to interface components at 480 V. This AC-system can be operated from zero voltage to as much as 20%–25% overvoltage. The nominal AC-frequency ranges from 45 Hz to 65 Hz and can go even wider at lower voltage levels. The DC-voltage maximum is 1150 V. Therefore, depending on the specifications of the inverters under test and tests to be performed, solar PV inverters with output ratings up to 1.5 MW may be tested. As an alternative to the VVS DC (not shown in the figure), a set of linear amplifiers was available to provide a controllable DC-source with a maximum available power of 10 kW and 350 V. Data concerning salient hardware components used in this project are provided in Appendix A.

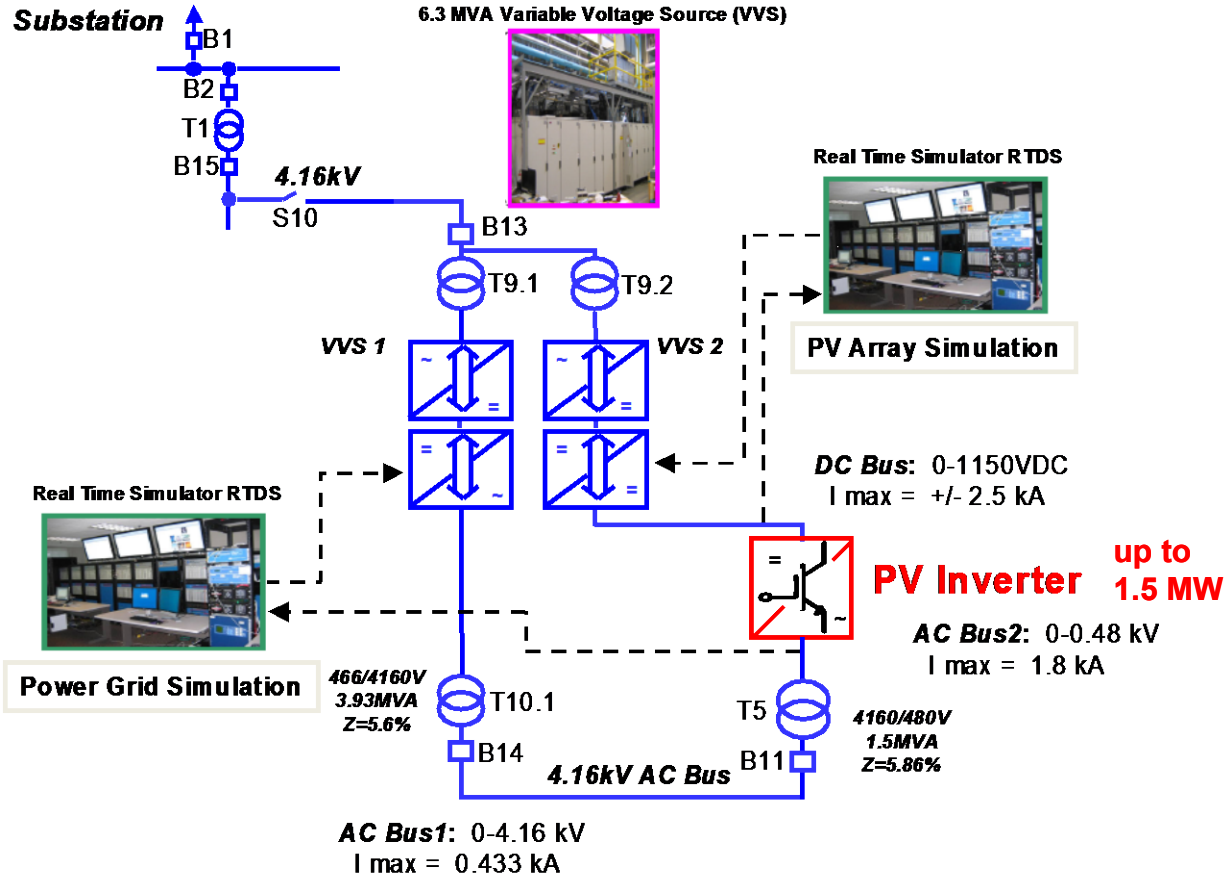


Figure 4, CAPS test facility for PHIL simulation of solar PV inverters

5 Real-Time Simulator

The core component of PHIL simulation is a real-time simulator (RTS). CAPS has a 14-rack digital real-time simulator from RTDS [6], and it was used in all experiments covered in this report. Depending on the test performed, the RTS case was set up to:

- Control the DC-side to provide either a fixed DC-voltage or emulate a solar PV array
- Command the AC-grid voltage level (the VVS-AC was used in most experiments to establish the grid voltage source)
- Provide protection for the tests including over-current, undervoltage and overvoltage, under- and over-frequency, zero-sequence detection
- Simulate a simple solar PV inverter model to allow testing of protection components
- Simulate the RoS model (e.g., RLC load bank, induction motor, active and reactive power injections
- Monitor and log selected data (e.g., rms-quantities, frequency, etc.) with an approximate update time of one second
- Capture experiment data sampled at multiples of the time step (i.e., multiple of 50 μs), typically limiting data captures to a few seconds Execute with a time step of 50 μs.

In addition, the runtime environment was set up to allow many of the settings and parameters to be changed while operating the equipment (e.g., setting the DC-power level), setting the RoS model parameters, and triggering the PHIL-based unintentional islanding tests.

6 RLC Load Bank

As the main project objective was to establish the feasibility of using the PHIL approach as an alternative testing method to the "conventional" RLC load bank-based approach, an RLC load bank was used to record unintentional islanding behavior. The recorded results were used for building reference behavior patterns. In Section 13, we compare the RLC load bank test results to the PHIL results.

The load bank—nominally 436 kvar and 480V—is a three-phase, delta-connected unit. For each of the components, we can choose from 13 available settings each for resistance, inductance, and capacitance.

In the unintentional islanding tests, the resistive component was chosen to set the active power level of operation for the solar PV inverter (P_{PV}). The inductance and capacitance were chosen to achieve a desired quality factor Q_f; inductive and capacitive reactive power levels were $Q_{L,C} = Q_f * P_{PV}$. IEEE Standard 1547.1 specifies that tests are to be performed with a quality factor of one (and small variations about $Q_f = 1$.) In the tests performed for this project, we used quality factors as high as three, as we wanted to determine the impact of higher quality factors on unintentional islanding behavior.

Note: All solar PV inverters used in this project were three-phase, four-wire systems; IEEE Standard 1547.1 requires wye-connected load banks with an accessible neutral point. Therefore, in some of the tests, we used additional wye-connected resistors to establish an accessible neutral point, but we could identify no significant differences in responses between the connection methods.

Note: The RLC load bank was only available for a limited time during the project and only experimental results for Inverter 2 are included in this report.

For technical RLC load bank details, see Table A-5 (Appendix A).

7 Solar PV Inverters Tested

This section briefly summarizes salient aspects of the solar PV inverters used in these tests. Additional data for the inverters are provided in Tables A-2, A-3, and A-4 (Appendix A).

Inverter 1 is a 17-kW, three-phase, four-wire, transformer-less solar PV inverter that was developed for the international market. By choosing the KEMCO 501/2009 (South Korea) setting, it was configured for a 400-V and 60-Hz system. Furthermore, the internal unintentional islanding setting used an escalation factor of 12 (in non-dimensional proprietary units) and a maximum islanding time of 500 milliseconds (ms). Note that tests with Inverter 1 could only be performed for RLC load bank-based tests and not the PHIL-based approach. Consequently, no comparison can be given here and no results are included.

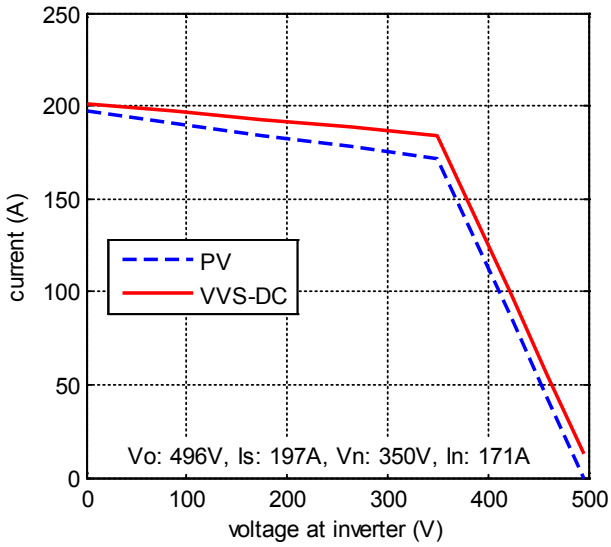
Inverter 2 is a 20-kW, three-phase, four-wire, transformer-less solar PV inverter that was developed for the U.S. market; it was, therefore designed and tested according to IEEE Standard 1547.1. This inverter was tested with both load bank and PHIL arrangements but only at lower power levels of up to 40%. Tests using PHIL simulation were based on only RLC as RoS model.

Inverter 3 is a 60-kW, three-phase, four-wire solar PV inverter that was developed for the U.S. market and tested according to IEEE Standard 1547.1. The inverter was based on single-phase units and has a high-frequency transformer on the DC-side. This inverter was only tested with the PHIL simulation approach, but for both RLC and alternate RoS conditions.

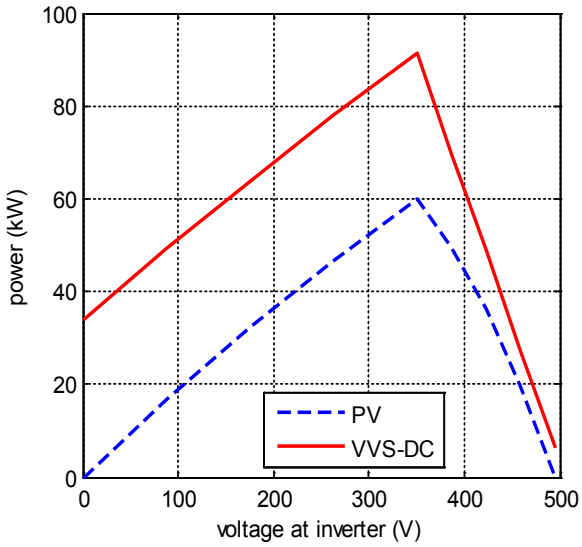
8 Emulating Solar PV Array Characteristics

We used a controlled DC source to emulate the DC-side of the PV inverters, and we used two different power amplifiers—a linear amplifier and a PWM-switching amplifier—but with consistent methods used for establishing the DC voltage. In this section, we summarize the procedure used to emulate the DC section of the hardware, and we provide an example of emulating a solar PV array.

Solar PV arrays provide an open-circuit voltage when no current is drawn. With increasing current demand, which is controlled by the solar PV inverter, the voltage across the DC terminals drops—at first, with a lower slope until the knee-point of the voltage-current characteristic is reached. Beyond the knee-point, the voltage drops faster until short-circuit conditions are reached (i.e., zero voltage across the DC terminals). An example characteristic of such a solar PV array behavior is shown in Figure 5. The figure depicts both the voltage-current characteristic and the corresponding active power characteristic. The voltage-current characteristic was implemented as a look-up table (with linear interpolation) to derive reference commands from the feedback signal.



(a) Emulated PV array characteristic (dashed/blue) and corresponding current-voltage profile for DC amplifier (solid/red)



(b) Power-voltage profile for desired 60-kW-peak PV array (dashed/blue) and corresponding DC amplifier profile (solid/red)

Figure 5. Solar PV array characteristic example: Emulating a 60-kW array

We used a controlled voltage source to emulate the DC array behavior in a configuration similar to that shown in Figure 6. The parallel resistor (Rp) provides damping and an opportunity to operate the array as a current source. We set the series resistance (Rs) to match the desired voltage drop at the point when current begins to flow. We adjusted the reference value for the DC amplifier to emulate the fast drop of the available DC voltage as current is increased when operating above the knee-point region.

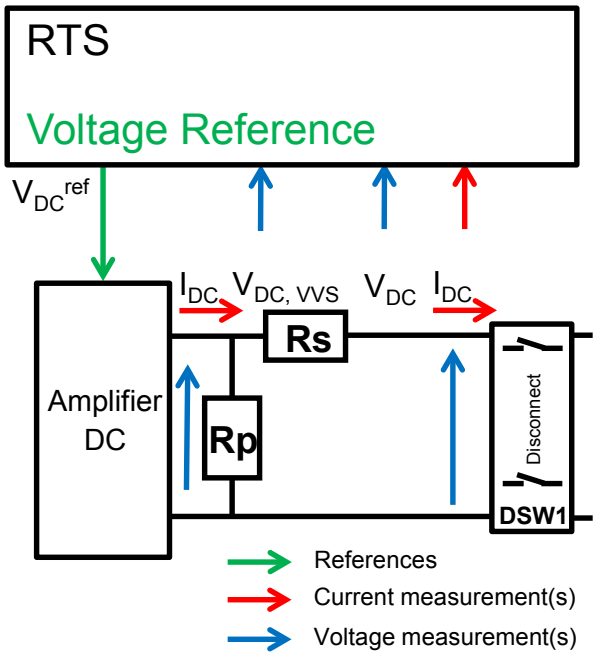


Figure 6. Emulation of solar PV array characteristics

9 Test Setups

This section describes the test setups used to perform the unintentional islanding tests. Fundamentally, three types of setups were used:

1. RLC load bank-based testing
2. PHIL approach with RLC load bank as part of the RoS model
3. PHIL approach with alternate RoS models, including:
    A. Induction motor with adapted LC-circuit
    B. Constant active and reactive power injection model-based on controlled current injections
    C. RoS models and active volt-var inverter controls

The following sections provide details about these individual setups.

9.1 RLC Load Bank-Based Tests

The test setup is shown in Figure 7. All of the components (i.e., AC- and DC-amplifiers, load bank, RTS, and other components) as introduced above were arranged to test the solar PV inverters according to IEEE Standard 1547.1 [2]. A switch on the AC-side was used to open the grid (actual or emulated) connection. The tests were repeated multiple times to allow the establishment of patterns of behavior to emerge. The figure depicts the salient elements of the RTS case, the measurements fed into the RTS case, and the references provided to the power amplifiers. The load bank was remotely configured according to the desired active power level and quality factor. The RLC load bank was configured in delta, but the inverters available were four-wire systems. According to the setup guidelines in [2], a wye-connected load bank should be used. A variation of this setup is shown in Figure 8 in which wye-connected resistors were used in addition to the load bank to provide a load-related neutral point to the inverter (100 ohm/phase).

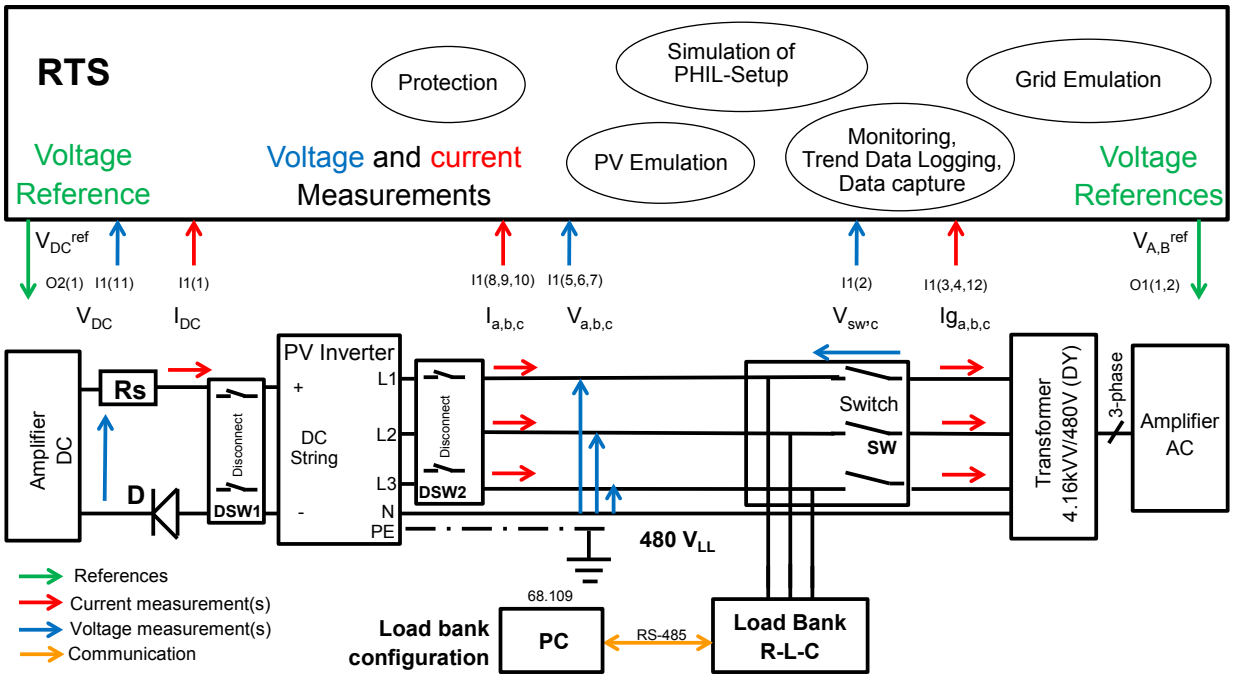


Figure 7. Test setup with load bank (1/2)

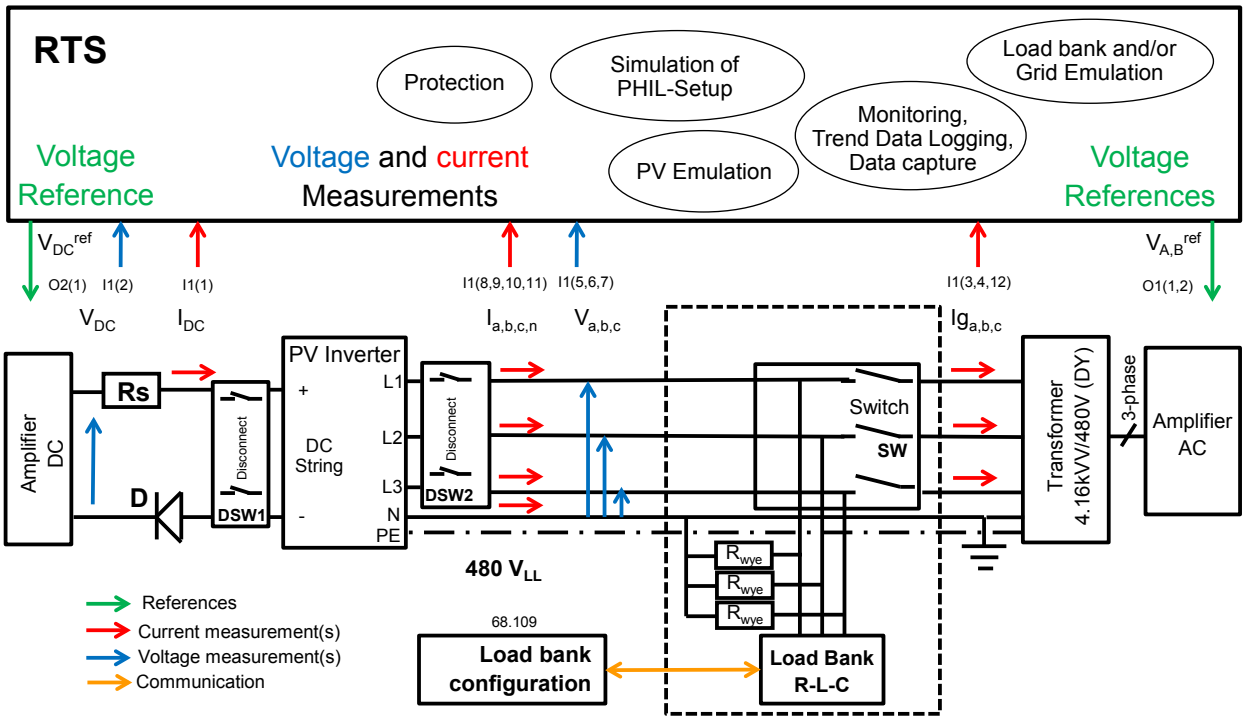


Figure 8. Test setup with load bank and additional wye-connected resistors (2/2)

9.2 PHIL Simulation-Based Tests

The test setups used are shown in Figures 9 through 11. We performed unintentional islanding tests using the PHIL setup, following the RLC load bank-based tests. The test set-points followed those used in the load bank-based approach, with some additional tests with variations in quality factor.

As shown in the figures, notable differences between the test setups included that the RLC load bank was modeled and simulated in the RTS case and interfaced to the inverter under test. We used a transformer (4.16 kV / 480 V) to match the voltage levels of the solar PV inverters. We adjusted the VVS-AC references to match the nominal inverter voltages of either 480 V or 400 V. As shown here, some of the measurements were taken by multiple probes for reasons of redundancy. Furthermore, when using the VVS-DC, we attached a ground resistor from the negative rail to the ground connection of the device under test, and we grounded the rail at the VVS-DC to avoid effects of possible parasitic rail-to-ground coupling.

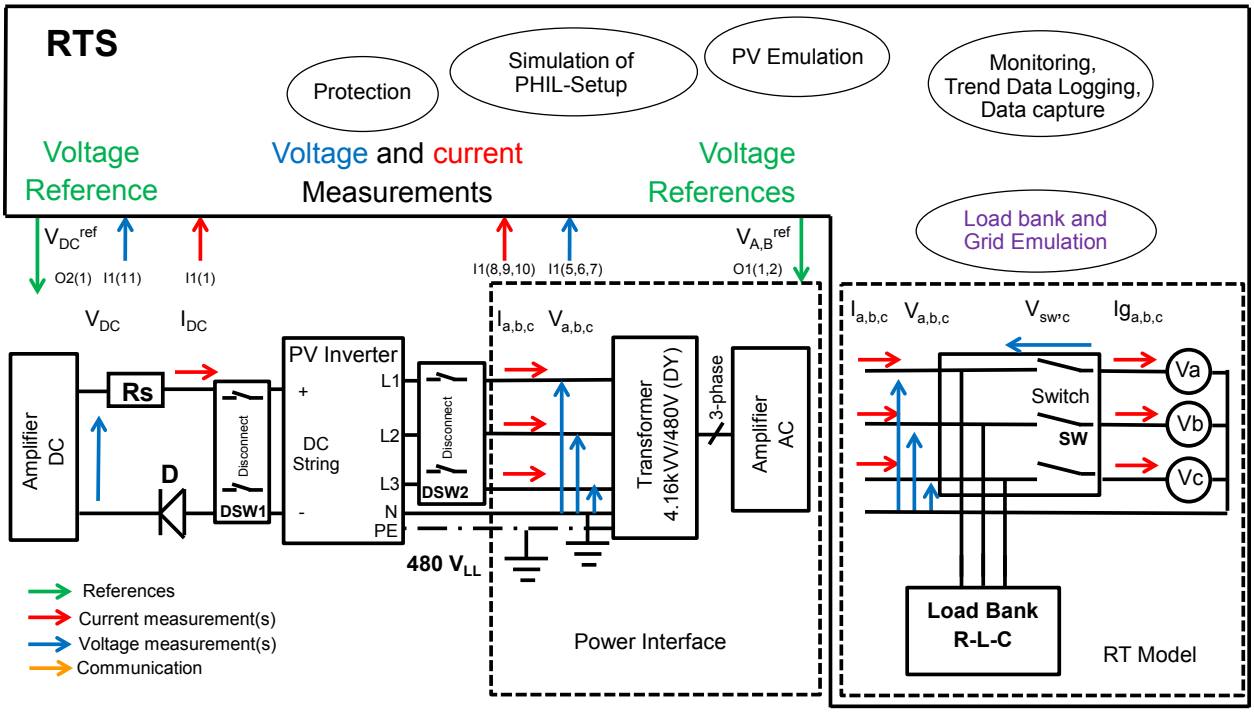


Figure 9. Test setup for PHIL simulation (1/3)

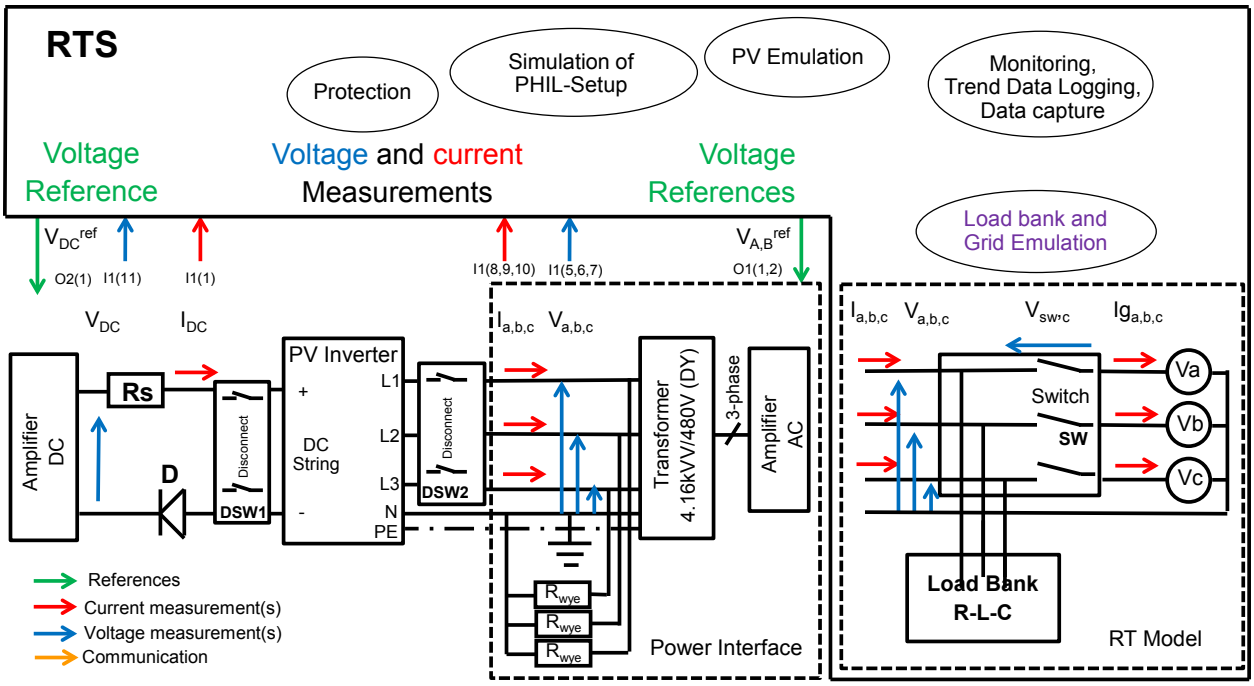


Figure 10. Test setup for PHIL simulation (2/3)

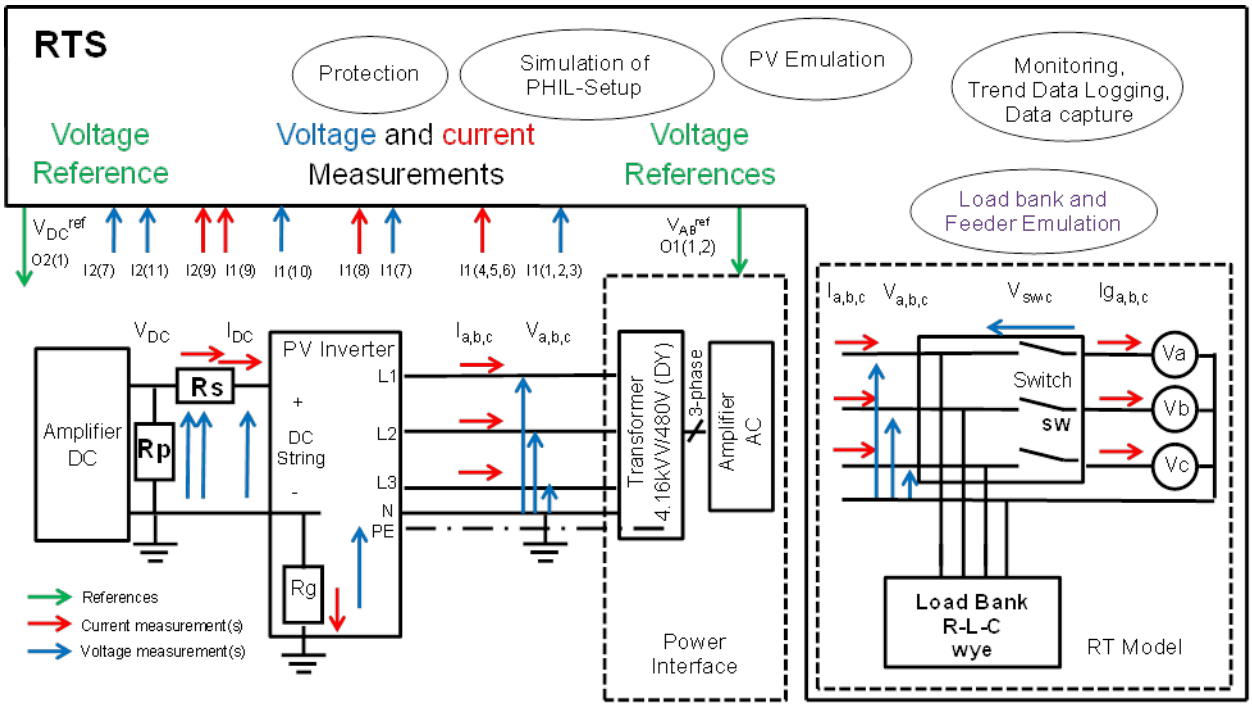


Figure 11. Test setup for PHIL simulation (3/3)

10 Selecting Test Conditions and Test Procedure

This section details choices made in selecting the RLC load bank and alternate conditions.

10.1 IEEE Standard 1547.1-Based Conditions

In this section, we present the factors that guided our selection of test conditions. First, the operating conditions for the solar PV inverter had to cover a representative range, but considering that only a limited number of tests could actually be performed. Too many individual levels for a single parameter would yield too many combinations to be tested and would be infeasible from a time perspective. The time it takes for a single test depends on an inverter's design, but every test requires restarting the solar PV inverter, i.e., establishing AC grid and DC-source conditions, solar PV inverter startup procedure and turn-on process, allowing the maximum power point tracking (MPPT) to settle at the desired power level. With respect to the active power levels before islanding, conditions were selected based on three ranges: low (less than 20% of rated power), mid (30% to 60%), and high (90% and above).

The second key parameter was the quality factor. As test conditions followed the IEEE Standard 1547.1 procedures, which tests at a quality factor of one (i.e., Qf = 1) and with small variations about one, our interest was focused on using a base quality level of one and multiples thereof. The range of quality factors was limited to four, as higher values seem to be unrealistic for actual conditions of distribution feeders. The nominal quality factor settings chosen for testing were Qf = [1, 1.5, 2, 3, and 4]. These values were only approximately achieved in the RLC load bank tests due to inherent component tolerances, and as accurately as possible in PHIL-based tests by tuning the simulated inductor and capacitor values based on reactive power measurements. Not all quality factors were tested in all test setups due to encountered instabilities, need, or both. The two key parameters in unintentional islanding tests are depicted in Figure 12.

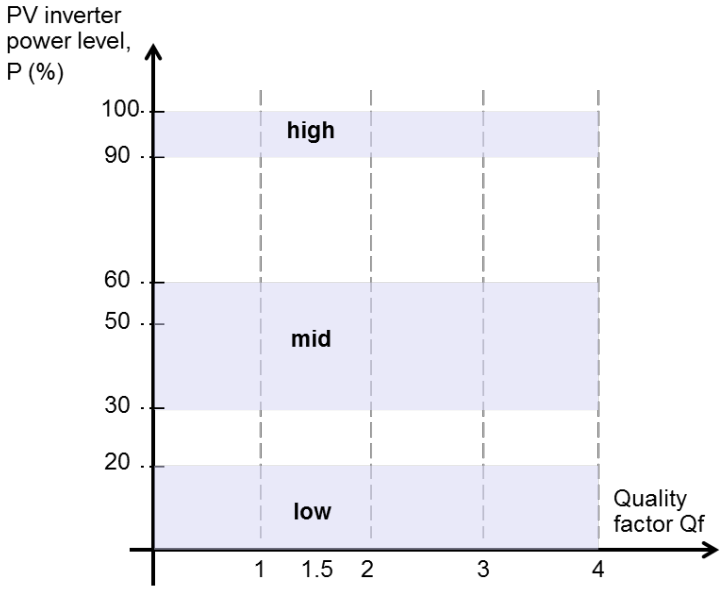


Figure 12. Selected ranges of interest for unintentional islanding tests (power level vs. quality factor)

10.2 Review of Alternate RoS Conditions

The question of the adequacy of the RLC load-based testing and the corresponding quality factor—or range of quality factors—for unintentional islanding has been visited many times during the development of standards for interconnecting solar PV inverters and distributed resources in general. Examples of estimating realistic load parameters and the physical meaning behind motor loads while islanded are given in [7] and [8]. For example, before a quality factor of one (Qf = 1) as specified in IEEE Standard 1547.1-2005 was agreed upon, IEEE Standard 929-2000 [9] suggested using a quality factor of 2.5. While the IEEE Standard 1547.1 does not include any other requirements, the Japanese standard does (as described in [10][2]) by including an idling induction machine in the test setup (but not specifying a quality factor for the load bank).

The following cases are of concern with respect to the possibility of degraded anti-islanding detection methods (see [10], [11], and [12]):

4. **"Large" number of inverters and inverters from different manufacturers:** As this situation becomes more realistic with the rapidly increasing use of solar PV resources, the need to test for multiple inverters as part of the same island may need to be revisited. In the PHIL simulation context, this test setup would be feasible with the "other" inverters simulated in real time in the case where appropriate and validated inverter models are available. As the main interest with respect to islanding issues concerns a time range of electric fundamental cycles to a few seconds, average value models may suffice in representing these inverters within the RoS model, and details required for full switching-based models could be avoided.
5. **Mixture of rotating machines and PV inverters:** Reference [11] indicates that earlier studies suggest that in the event more than 25% of generation is based on rotating machines, the likelihood of long run-on times becomes considerably higher. Reference [10] describes part of a Japanese standard on anti-islanding testing, which requires testing with one idling induction machine.
6. **Interconnecting impedance between inverters is significant:** A large impedance (especially inductive) has the effect that inverters do not see the same voltage at the same time and may therefore counteract each other. Guideline [12] suggests that if fault current levels differ by a factor of three or more, further studies are warranted.
7. **Advanced inverter functions:** Newly available inverter capabilities, which adjust active and reactive power output, may negatively interact with the unintentional islanding algorithm and prolong run-on times.

Based on these salient points, test facility capabilities, and the availability of appropriate PV inverter units, we used variations of the items above as guidelines for determining candidate test conditions:

- Induction motors with inertia loads

[2] Concerning the unintentional islanding requirements, IEEE Std. 1547 allows a maximum of two seconds and the Japanese standard allows 0.2 seconds to cease to energize and/or disconnect.

- Constant active-reactive power injection models to mimic other inverters without other controls or disturbances in power (e.g., unintentional islanding algorithms)
- Advanced inverter features: active volt-var controls as part of the inverter setup and as part of the active and reactive power (PQ) model.

We used all of the corresponding test conditions to ensure that the solar PV inverter operating conditions closely matched active and reactive power demands before islanding. Furthermore, we added LC circuits to achieve an effective quality factor—in a fashion similar to the conventional RLC load bank testing approach.

10.3 Selected Alternate PHIL RoS Conditions

The following RoS models were chosen as the most valuable candidates for testing alternate RoS conditions based on the review and discussion of alternate test conditions in the Section 10.2. These conditions were applied while testing Inverter 3, a PV inverter rated for 60 kW.

- **Induction motor:** *detailed induction motor model simulated with its rating based on the power rating of the PV inverter, and the mechanical load at the shaft tuned to match the desired PV inverter active power output*
  A parallel LC circuit (as in the RLC load bank tests) is modeled to achieve a desired quality factor. As the induction motor already draws inductive reactive power, a higher inductance value results when compared to the RLC tests;
- **Constant RLC and PQ-model:** *model based on a parallel RLC model and a constant power model*
  We used an RLC circuit with settings to achieve a desired active power load level (i.e., multiples of the PV inverter active power output) and a desired quality factor with respect to the PV inverter output power. The constant power model represents other power electronic-based resources with active controls. Though not modeled at the device switch level—instead representing the average value equivalent—the PQ-injection model is set to inject power based on DQ-current controls (i.e., controlled current components that are derived from a phase-locked-loop and the local voltage measurement). The active power part is varied in the experiments, but the reactive power part is always zero. The active power difference (i.e., desired power level minus the PV inverter set-point) is the set-point for the PQ-model. Consequently, the resulting overall quality factor becomes equal to $(Qf * P_{PV}) / (P_{PV} + P_{PQ}) = Qf / n_P$, with n_P representing the overall active power level (i.e., the sum of PV inverter power and constant PQ-injection power).
- **Constant RLC and constant PQ-model with V-var controls (50 kvar):** *same model as above but the PQ-injection model considers a volt-var curve as the basis for providing a reactive component as well*
  Parameters of the chosen curve (95% 98% 102% 105%) voltage levels are mapped to (50% 0% 0% -50%) reactive power.
- **Constant RLC and constant PQ-model with V-var controls (25 kvar, 100 kvar/s):** *same model as above but with half the reactive power and reactive power ramp rate limits*
- **Constant RLC, constant PQ-model, and PV inverter with active V-var control:** *same voltage-to-reactive power mapping but performed by the PV inverter instead of the PQ-model*

The grid voltage set-point is adjusted to 1.02–1.03 pu to operate the PV inverter at a point with reactive power before islanding (about 10 kVA). The actual volt-var characteristic was verified by slowly ramping operating conditions over the full voltage range while operating at 90% output power (54 kW). The reference and measured characteristics are shown in Figure 13.

- **PV Inverter with V-var control and scaled induction motor:** *combination of the cases above: PV inverter with active volt-var control and induction motor as part of the RoS* Again, parallel L-C are used to achieve a Qf = 2. The induction motor rating is scaled up in its kVA rating, but the mechanical load at the shaft is kept at the PV inverter output power level of 54 kW. Grid voltage set-point is adjusted to 1.02–1.03 pu to operate the PV inverter at a point with reactive power (about 10 kVA) before islanding.

The volt-var characteristic chosen is depicted in Figure 13. The measured reactive power vs. voltage is shown in solid/blue, and a reference characteristic is shown as dotted/red. The inverter is operated at about 90% of its rated capability, and the reference characteristic is based on the nominal rating. The characteristic is showing a systematic shift in voltage level (to lower values by 1%), but this may be due to the voltage probes, which have an accuracy of 2%.

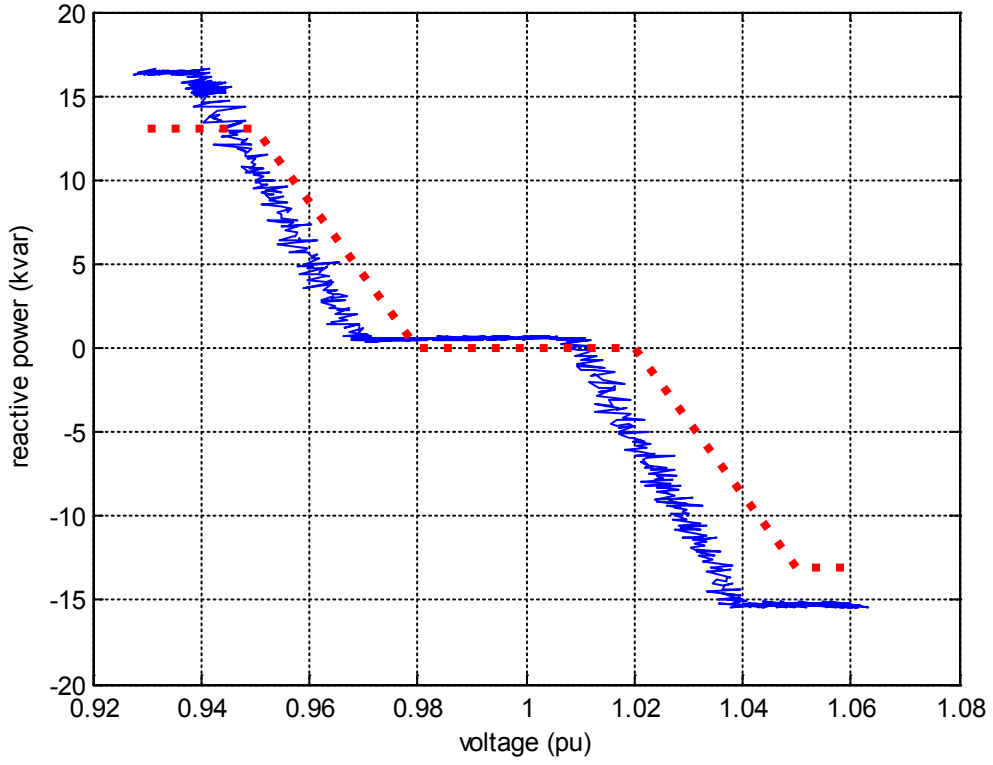


Figure 13. Volt-var characteristic (Inverter 3): Measured (solid/blue) and Reference (dotted/red)

10.4 Test Procedure

We used the following load bank and PHIL-based unintentional islanding test procedures:

1. Configure RoS.

D. In discrete RLC load bank-based tests, configure load bank by sending appropriate commands.

E. In PHIL-based tests, configure applicable settings (e.g., RLC load bank or induction motor parameters).

2. Establish normal test bed operating conditions.

F. Set AC-system at nominal voltage and frequency.

G. Set DC-system at initial target voltage for either constant voltage source or solar PV array characteristic operation.

3. Close AC and DC disconnect switches.

4. Wait for solar PV inverter to turn on.

5. In case of PHIL experiments:

H. Gradually engage feedback loops.

I. If applicable, gradually increase DC-side power reference until target value is reached.

6. Wait for PV inverter to establish desired operating conditions as MPPT finds the operating point at chosen power level).

J. In case of PHIL experiment, iteratively tune settings to achieve test conditions (e.g., reduce grid current level, reduce reactive power mismatch)

7. Initiate island.

K. For discrete load bank, open switch.

L. For PHIL, open switch that disconnects modeled grid source from remaining RoS model.

8. Observe experiment until:

M. Inverter turns off, or

N. Experiment timer expires. (all experiments safe-guarded and halted in case island is not detected; default setting is 2.2 seconds)

Note: The steps listed do not include several details—such as activating and adjusting protection settings—but provide the outline of performing one experiment. We repeated all of the islanding tests multiple times to allow patterns of behavior to be observed.

11 PHIL Interface Algorithms

The PHIL interface algorithms are an important part of performing PHIL simulation-based experiments, as the algorithm deployed impacts stability and accuracy. An overview diagram of the PHIL interface algorithms used during the testing for this project is shown in Figure 14. The diagram shows in a unified manner the algorithms considered: the ideal transformer model (ITM) and the damping impedance method (DIM). Furthermore, depending on the filters implemented, both instantaneous and DQ reference frame-based approaches can be realized. All of the approaches used were based on sending voltage commands to the amplifier and feeding currents and (in the case of the DIM algorithm) voltages back into the RoS model. The following sections summarize the underlying concepts of the approaches. For additional information on the methods, see [13].

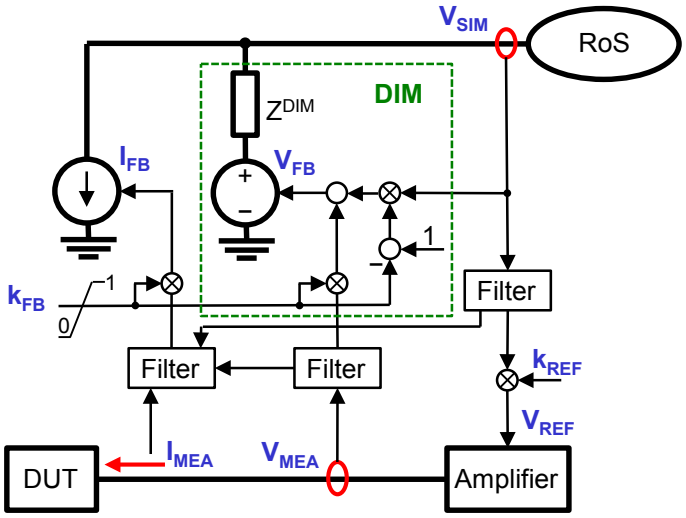


Figure 14. PHIL Interface Algorithms

11.1 Ideal Transformer Model

This implementation of the ITM interface algorithm is used for coupling systems in which instantaneous voltage references are provided to the power amplifier. Depending on the filter implementation, this module can be configured for a pure instantaneous quantity implementation, a pure DQ-axis implementation, or a hybrid combination of the two. If used with instantaneous values, the interface can be used for DC systems as well. The filters can be used to limit the bandwidth of the respective quantities based on needs for stability and accuracy of the interface. The gain k_{REF} is typically set to a value between zero and one, and it is used to enable and scale the references to the amplifier. The gain k_{FB} is used to engage the current feedback to the model. Typically, this gain is initially set to zero to inhibit current feedback, and it is gradually ramped to a value of one to fully engage the current feedback.

The filters may include reference frame transformations where phase-locked loops (PLL) track the frequency and phase angle at both the terminals of the RoS model and measured voltages, V_{MEA}. The phase angles are used to convert the instantaneous voltages and currents into D- and Q-axis components. These components are optionally filtered and converted back into instantaneous quantities with respect to the RoS model's stationary frame. The actual voltage

references to be sent to the VVS can be scaled through k_{REF} to gradually increase the test bed voltages. If the ITM algorithm is selected, the damping impedance, Z^{DIM}, is set to represent an open circuit, and the voltage feedback, V_{FB}, as shown in Figure 14 is not used.

11.2 Damping Impedance Method

The damping impedance method (DIM) adds to the ITM method a second feedback path. In addition to the measured current, the measured voltage is used in combination with an impedance, Z^{DIM} (also denoted as Z* in the literature), as feedback to the RoS model. As described above for the ITM method, the algorithm's principle of operation and implementation allows both instantaneous and reference frame-based PHIL interfacing. The amplifier reference commands and the feedback can be gradually engaged to allow for a controlled transition from open-loop to closed-loop PHIL operation. For initialization purposes (e.g., starting up a PHIL experiment without feedback and then engaging the feedback), the simulated voltages, V_{SIM}, are used in the feedback path. As the feedback gain is gradually increased from zero to one, the inserted voltage V_{FB} transitions from the simulated voltages to the measured quantities. The choice of the damping impedance is critical for both stable and accurate operation, and the impedance value should match the DUT impedance characteristic in the frequency range of interest.

11.3 RTS Simulator and PHIL Experiment Interfacing Considerations

The PHIL test bed established at CAPS is based on the following. First, as shown in the test setup in Section 9, the VVS-AC is interfaced to the solar PV inverters through a delta-wye transformer. Second, reference commands to the VVS-AC amplifier and feedback (measurements) from the DUT need to be linked to the RoS model through either a reference frame (i.e., DQ-frame) or an instantaneous approach. In case of a reference frame, a phase-locked loop is required that can follow possibly distorted and unbalanced voltages. For example, while islanded, solar PV inverters may be able to change voltages enough to go from a positive to a negative sequence. While positive sequence tracking PLLs are available in many software tools (such as the one used for the RTS at CAPS), alternate implementations were used to improve PLL performance. The improved PLL was based on positive and negative sequence tracking allowing two reference frames (also known as a decoupled double synchronous reference frame approach) and using second-order generalized integrators (see [14]).

12 Test and Signal Analysis and Detection and Timing of Islanding Conditions

The test results were inspected and analyzed with respect to the following: instantaneous voltages and currents, instantaneous active and reactive power DC voltage and current, voltage and current rms-values, fundamental frequency, and frequency (FFT) content of AC-voltages, AC-currents, and AC-power terms before islanding.

The island formation and de-energization can be detected based on several signals. In RLC load bank tests, both were detected by comparing voltages to thresholds (i.e., voltage above 1 V across the switch and less than 5% of nominal voltage remaining). We used a second method for computing the time required for disconnect based on the inverter currents (i.e., filtered, absolute phase currents less than a threshold). In later tests, a third time was computed based on inverter DC-current dropping below a threshold (50% of pre-island current level). The islanding times based on these rules are consistent in that the AC-voltages decay more slowly than the AC-currents. The DC-current yields the fastest timing results, and these results are independent of the quality factor (the higher quality factors result in longer post-event oscillations.)

12.1 Test Results

The following sections summarize the unintentional islanding tests performed. We start by discussing selected results in the time domain and then present island detection timing results. The timing results are presented for both load bank and PHIL as applicable to allow a direct comparison.

The different setups and scenarios tested were a consequence of several factors. First, some of the islanding tests yielded highly dynamic results with respect to frequency content (primarily in currents), and efforts were undertaken to understand and possibly reduce effects. Second, as stability was a concern in PHIL simulations, several improvements and changes were made to the PHIL interface algorithm. Third, the nominal ratings of inverters, the RLC load bank, and the DC-amplifiers available for testing were not a sufficient match to cover the desired test conditions with just one setup. During the course of the project, three inverters were tested, two of which are reported herein (Inverters 2 and 3). Furthermore, the PHIL test setup and facility had to be changed, as the amplifier on the DC-side had a failure of one of its power stages and could afterwards not provide enough power to perform tests in the targeted high-power range (i.e., above 90%).

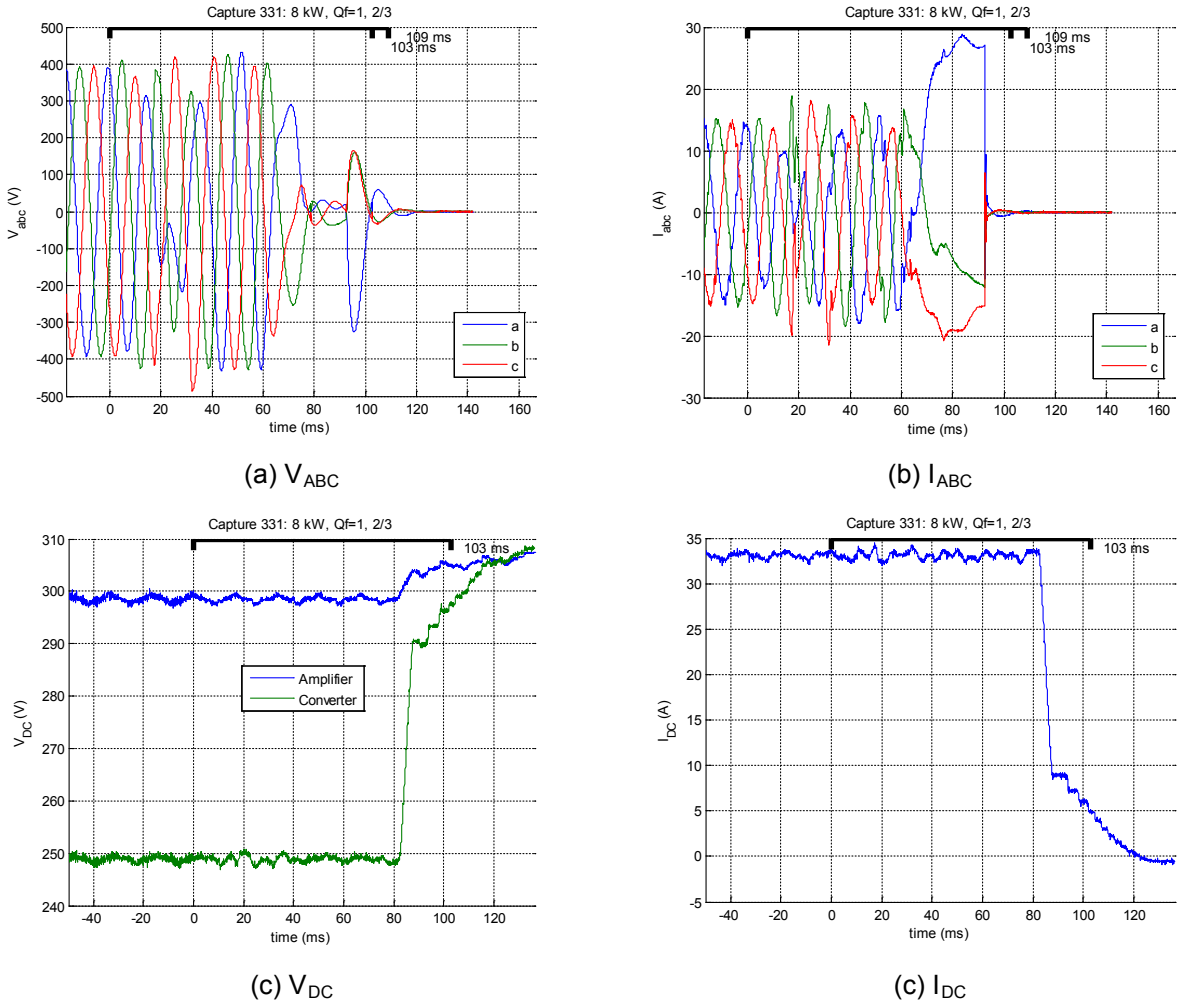
12.2 RLC Load Bank-Based Tests

This section summarizes results of unintentional islanding tests, which used RLC load bank and emulated AC grid connection (i.e., fixed voltage reference without active feedback controls). The DC amplifier was operated in controlled voltage mode, and the RLC load bank was configured for 480 V. All results were recorded using PV Inverter 2. The test setup is shown in Figure 7. On the DC-side, the series resistance values were 1.5-ohm for 8-kW (40% power level) tests and 6.5-ohm for 3-kW (15% power level) tests. The DC-amplifier was operated as voltage source with appropriate voltage set-points that yielded, after settling of the inverter's MPPT algorithm, the desired power levels.

The corresponding island detection times as derived from the measurements are listed in Table B-1 (Appendix B). A graphical representation of the timing results and a comparison to PHIL-based results is provided in Section 13.3.

Figures 15–20 depict islanding behavior observed for a small set of selected test conditions. We observed the following:

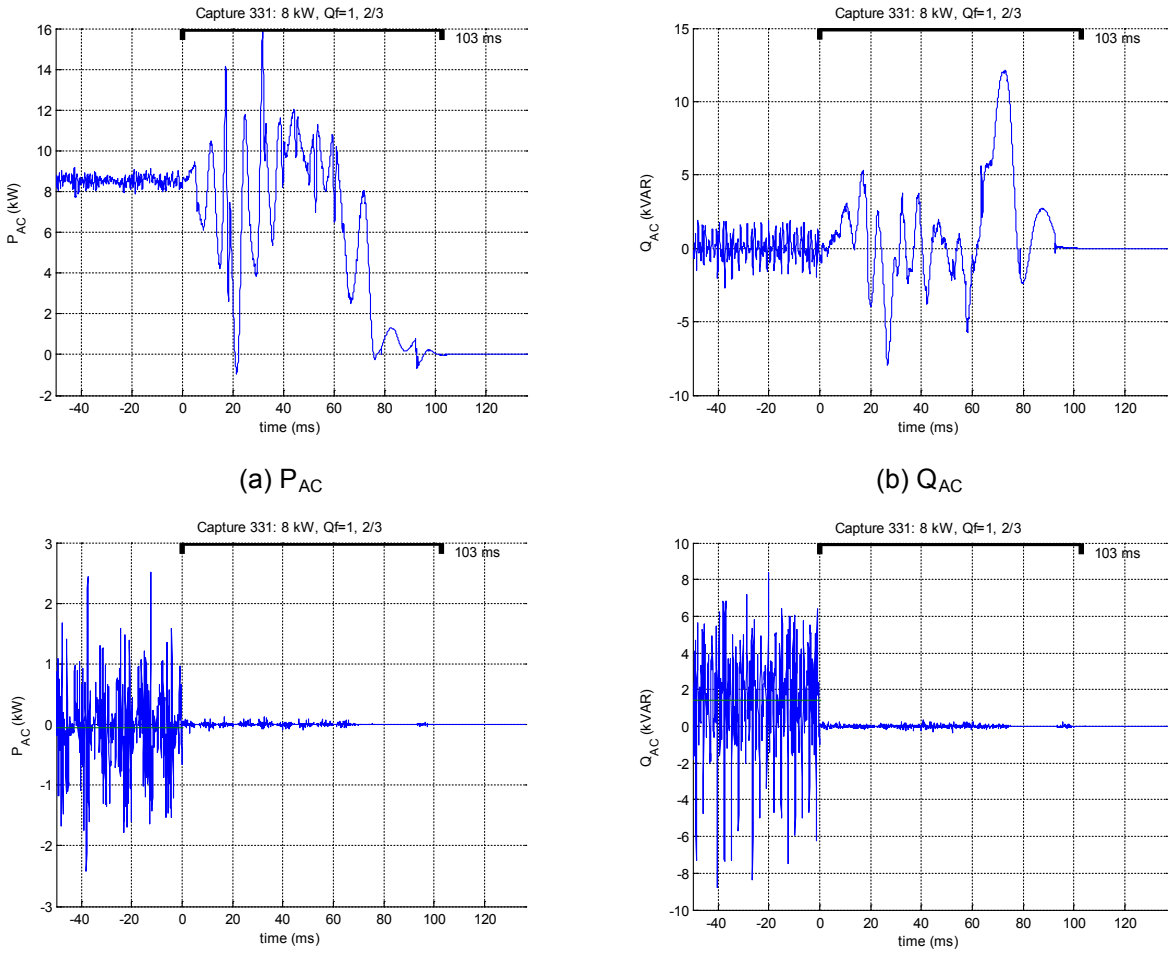
- There is a possibility of high-frequency content in currents (see Figure 18).
- There is a possibility of voltage phase reversal, i.e., an initially positive sequence system is shifted to a negative sequence (see Figure 15).
- Grid currents show a high amount of harmonic currents before islanding.



(a) V_{ABC} (b) I_{ABC}

(c) V_{DC} (c) I_{DC}

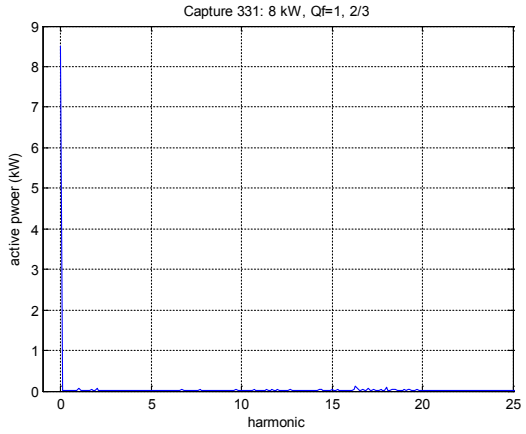
Figure 15. Inverter 2, load bank, 8 kW, Qf = 1, Capture 331 (1/3)



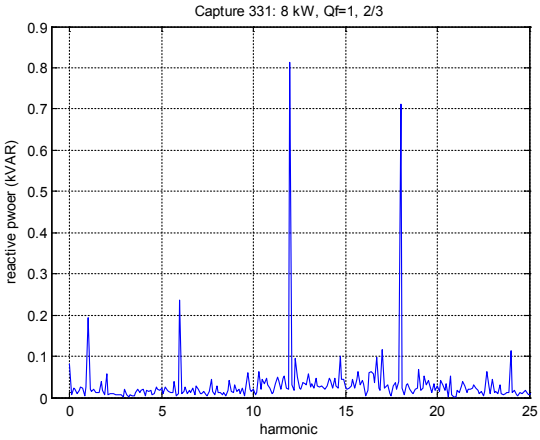
(a) P_{AC} (b) Q_{AC}

(c) Grid P_{AC} (d) Grid Q_{AC}

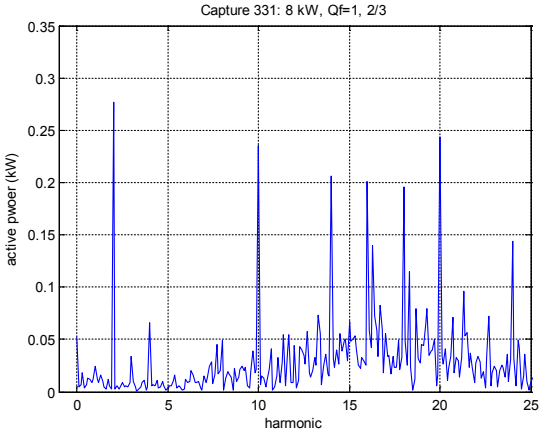
Figure 16. Inverter 2, load bank, 8 kW, Qf = 1, Capture 331 (2/3)



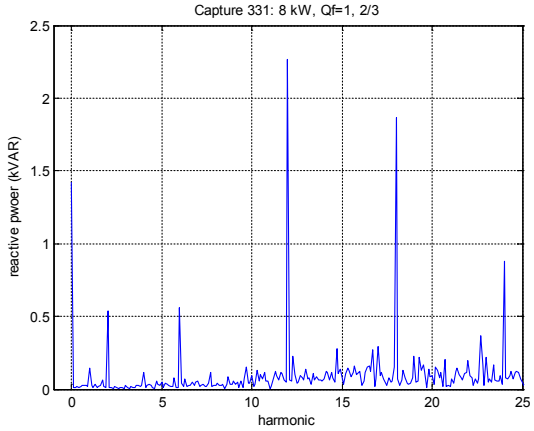
(a) P_{AC} FFT



(b) Q_{AC} FFT



(c) Grid P_{AC} FFT



(d) Grid Q_{AC} FFT

Figure 17. Inverter 2, load bank, 8 kW, Qf = 1, Capture 331 (3/3)

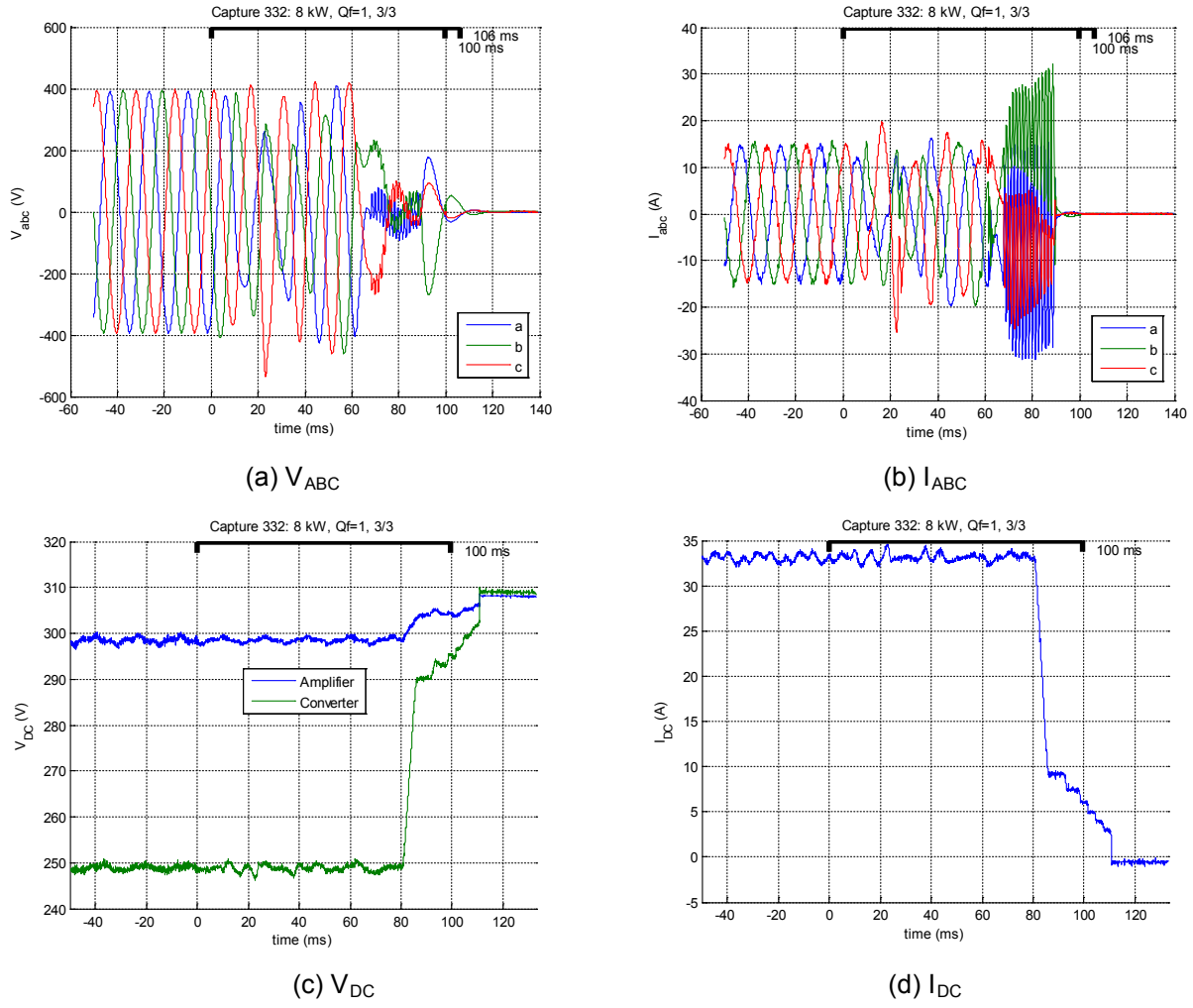


Figure 18. Inverter 2, load bank, 3.125 kW, Qf = 3, Capture 332 (1/1)

Because of the unexpectedly high dynamics in the results of the tests (i.e., dynamics in inverter current), we added a wye-connected resistive load component in parallel to the delta-connected load bank and repeated the tests. We connected the neutral point of this resistive (100 ohm/phase) load to the neutral wire (see Figure 8). Test results show a reduction in the number of prolonged high-frequency current events. Two selected test results are shown in Figures 19 and 20 for the two power levels (15% and 40%) and a quality factor of one.

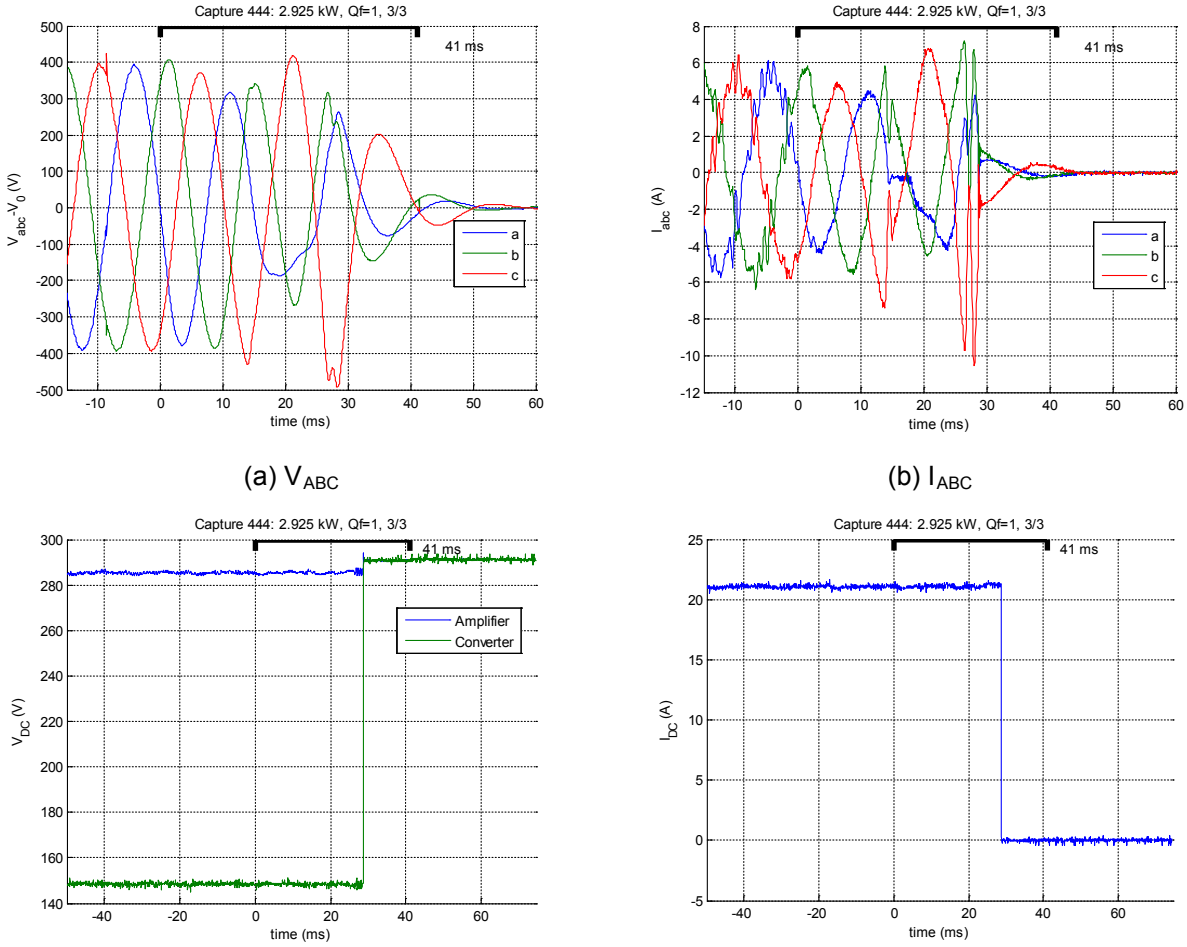
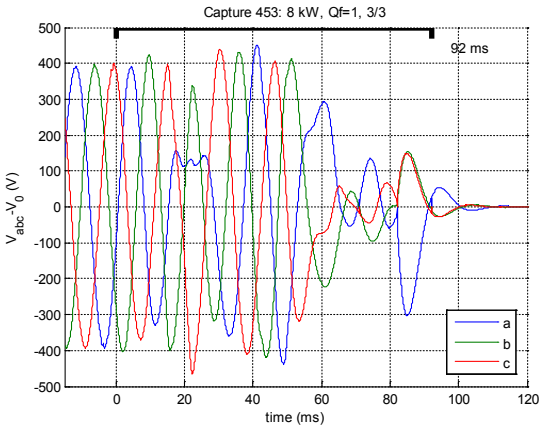
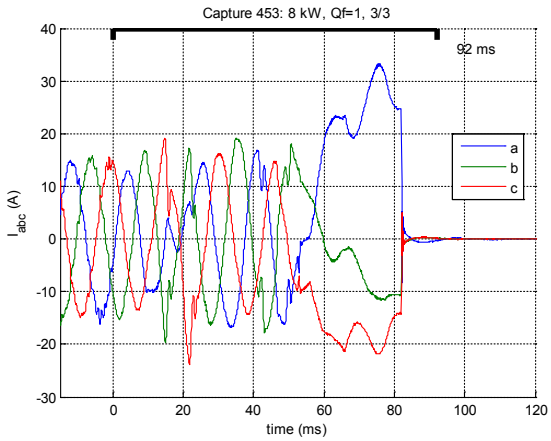


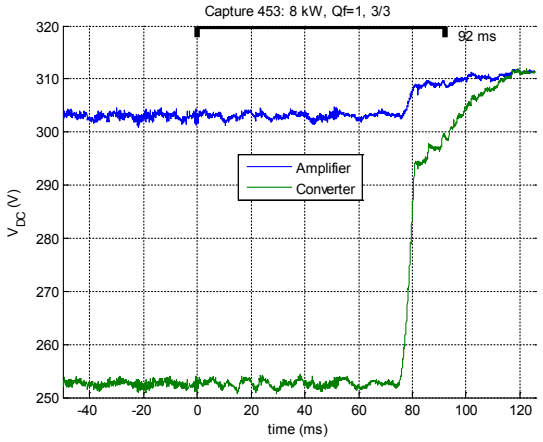
Figure 19. Inverter 2, load bank, 3 kW, Qf = 1, Capture 444



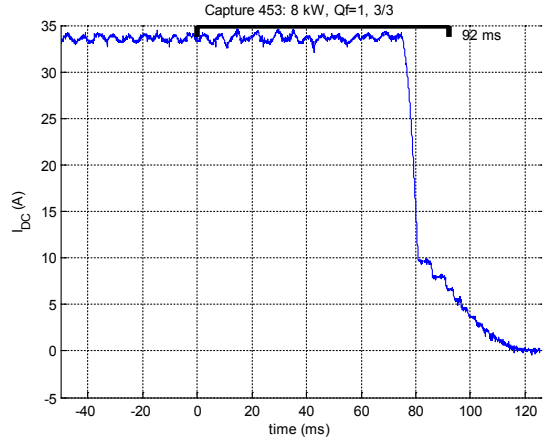
(a) V_{ABC}



(b) I_{ABC}



(c) V_{DC}



(d) I_{DC}

Figure 20. Inverter 2, load bank, 8 kW, Qf = 1, Capture 453

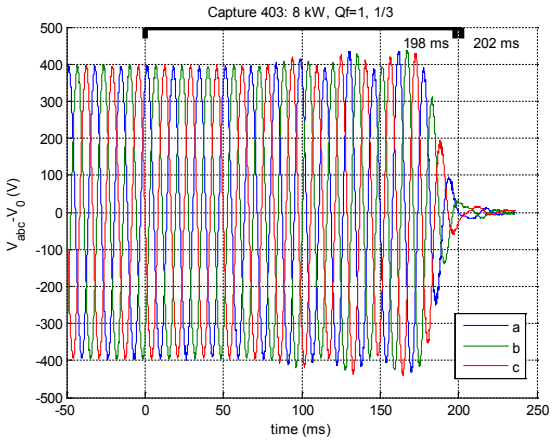
An overview of the selected test conditions for both load bank-based setups is given in Table 1. The desired test conditions are listed on the left, and the corresponding actual settings as achievable by configuring the load bank are listed on the right.

Table 1. RLC Load Bank Settings (Operating at 480 V, R_{WYE} = 100 ohm)

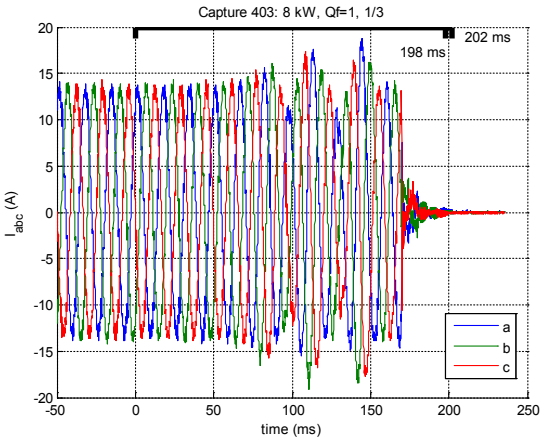
P (kW)	Q_f	Q (kvar)	P_{RLC} (kW)	P_{WYE} (kW)	Q_{RLC} (kvar)	P (kW)	Q_f
8	1	8	8	-	8.125	8	1.02
8	4	32	8	-	31.875	8	3.98
3	1	3	3.125	-	3.125	3.125	1.00
3	2	6	3.125	-	6.250	3.125	2.00
3	3	9	3.125	-	9.375	3.125	3.00
8	1	8	5.750	2.3	8.125	8.05	1.01
8	4	32	5.750	2.3	31.875	8.05	3.96
3	1	3	0.625	2.3	3.125	2.925	1.07
3	2	6	0.625	2.3	6.250	2.925	2.14
3	3	9	0.625	2.3	9.375	2.925	3.21

12.3 PHIL Simulation-Based Tests

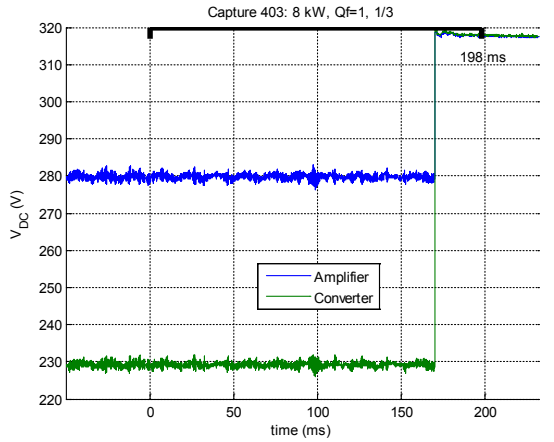
We performed unintentional islanding tests based on PHIL simulation using the same settings as in the load bank-based approach but with additional tests with variations in quality factor. The additional settings were also intended to allow probing for the stability boundaries (i.e., to determine the region in which PHIL simulation could be successfully applied). As in the load bank-based tests, two setups without and with the additional wye-connected resistors were tested. We used two different PHIL interface algorithms: reference frame-based and instantaneous ideal transformer model-based. We present selected results for the DQ-PHIL below. Though the inverter was able to detect islanding conditions, the islanding events seem to show slightly different behavior than the discrete load bank-based tests. Swings, for example in voltages, are more pronounced and last longer. Also, we estimated the AC-voltage frequency based on zero-crossings and 1-cycle FFTs. These estimated frequencies showed larger deviations from 60 Hz than those estimated by the PLL. We concluded the PLL subsystem of the PHIL interface algorithm needs to be improved. Figure 21–23 show representative test results.



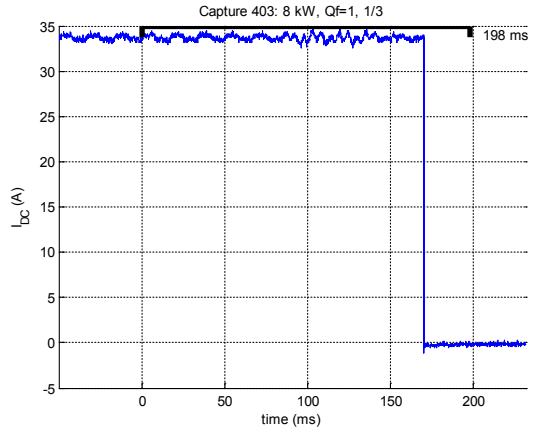
(a) V_{ABC}



(b) I_{ABC}

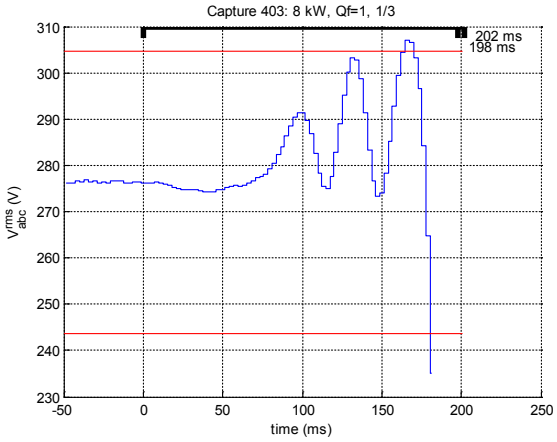


(c) V_{DC}

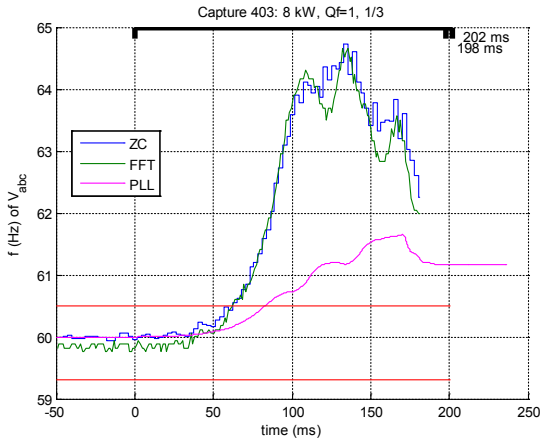


(d) I_{DC}

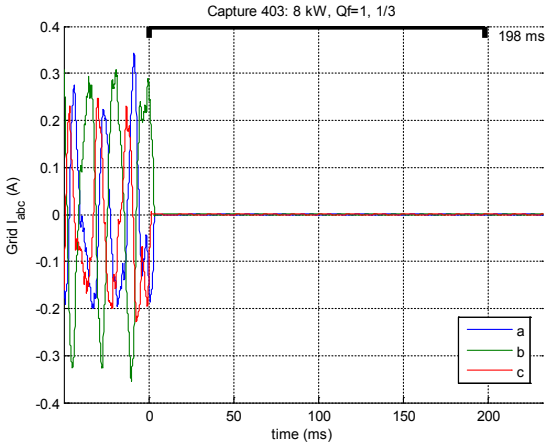
Figure 21. Inverter 2, DQ-PHIL, 8 kW, Qf = 1, Capture 403 (1/3)



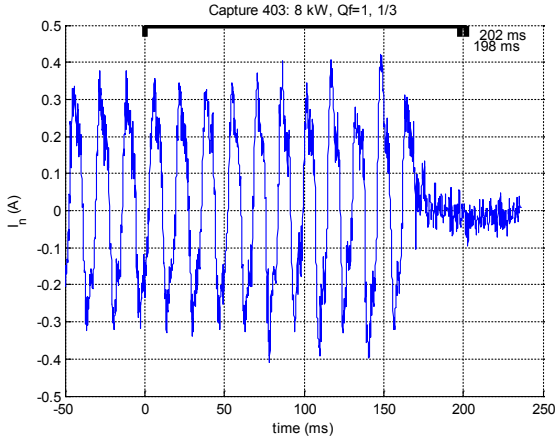
(a) $V_{ABC,\ rms}$



(b) $f_{(Hz)}$ of V_{abc}



(c) Grid I_{ABC}



(d) I_N

Figure 22. Inverter 2, DQ-PHIL, 8 kW, Qf = 1, Capture 403 (2/3)

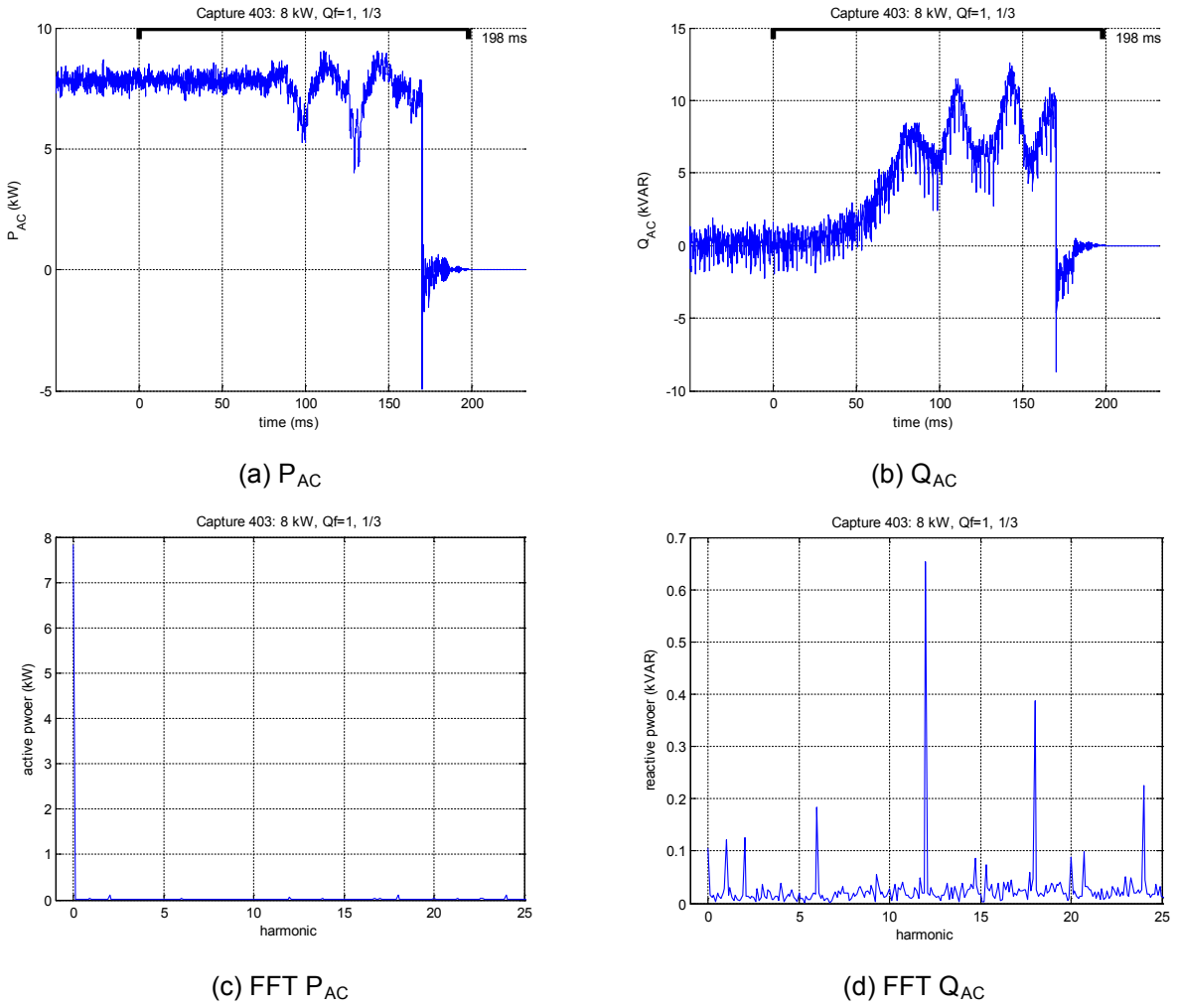


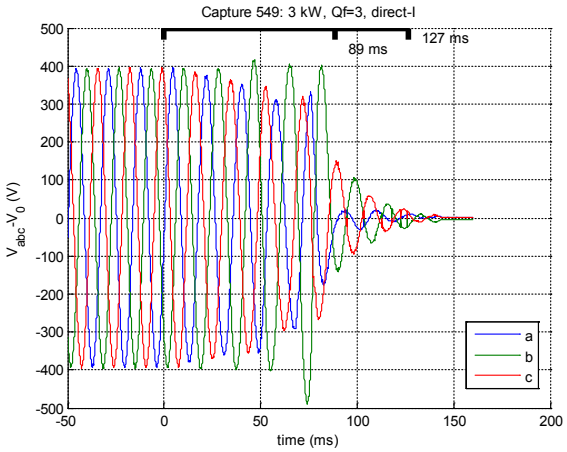
Figure 23. Inverter 2, DQ-PHIL, 8 kW, Qf = 1, Capture 403 (3/3) (H)

In an attempt to improve PHIL simulation performance, we made several modifications to the DQ-PHIL interface and the VVS control. First, we computed the VVS reference voltages considering the transformer setup and therefore not using the reference frames to compensate for phase shifts. Second, the phase-locked loop (PLL) was improved to adequately handle both positive and negative sequence voltages by considering both sequence frames separately. These improvements yielded more accurate voltage and current tracking, but dynamic performance was still limited. Third, an improved PLL scheme, now based on a second-order generalized integrator was implemented to better track frequency and phase angle in case of large negative sequence voltage components. Details on both the reference frame and PLL improvements can be found in [14]. A fourth modification in PHIL interfacing was based on using the improved DQ-PHIL for voltage commands but with direct feedback of measured current. The DQ-based approach allowed us to limit the bandwidth of interfaced signals and measurements without attenuating the fundamental quantities. Results for unintentional islanding tests based on all three improvements and in combination with the fourth modification are shown in Figures 24 and 25. In summary, these improvements resulted in additional successful test cases, an example of which is shown in Figure 24. A detailed view of corresponding AC phase A voltages and

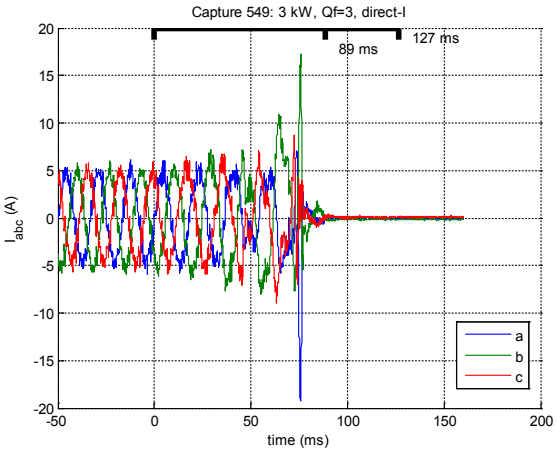
currents is shown in Figure 25. The commanded and measured voltages follow closely up to the inverter turn-off. The phase A currents shown are the measured current and the current fed back into the RoS—in this case using direct feedback. But, even with the improved interface, some tests resulted in PHIL amplifier trips.

Because of the inconsistencies in test results, we investigated the direct ideal transformer model (ITM) interface. The direct ITM interface avoids the DQ-reference frame transformations and uses unfiltered voltage output and current feedback for the PHIL-interface algorithm. Test results are shown in Figure 26 and Figure 27. The figures depict voltages and currents of both AC- and DC-subsystems. The voltages and currents in Figure 27 are measured at one of the AC phases, phase A, and they are representative of the PHIL interface used here. For example, the phase A voltage as derived from the RoS model ("reference", blue trace) is the commanded amplifier voltage, and the "VVS" voltage is the measured voltage as generated by the amplifier. The inverter current as measured (blue) is corrected for the wye-connected resistor part (shown as "mea (M)" in red), and its filtered version is fed back into the RoS model ("model", green trace), which coincides with "mea (M)" and is practically indistinguishable from the measured current.

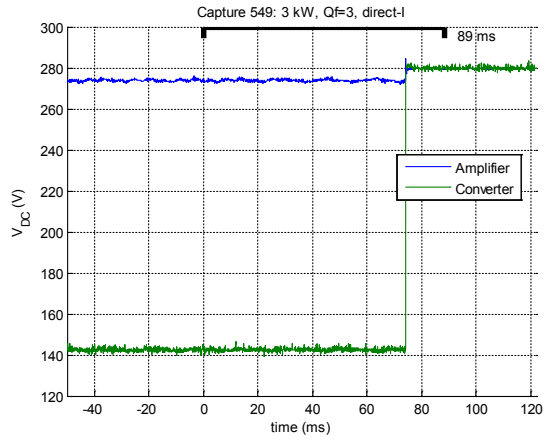
Three of the five operating conditions show that PHIL-based AI-testing can be performed successfully, though the detection pattern (timing) does not always match the load bank derived results. For the corresponding results on islanding times comparing load bank and PHIL approaches, see Section 13.3. Two of the operating conditions (3 kW and Qf = 1 and 2) yielded unstable and marginally unstable results. Another test point at Qf = 1 was chosen to narrow the range of possible operating conditions; 4.4 kW at Qf = 1 also showed an unstable event. Figure 28 shows the tested operating conditions with respect to stable, marginally stable, and unstable PHIL simulation results when using the ITM-interface algorithm.



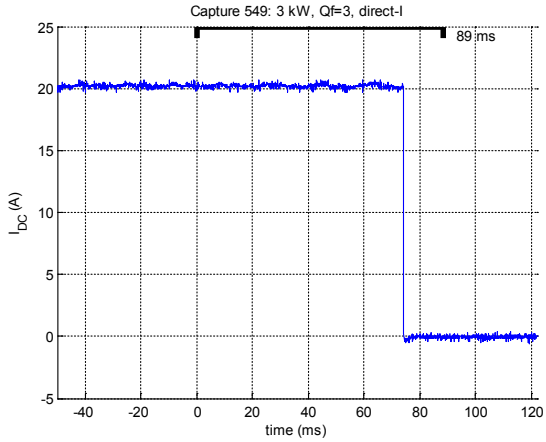
(a) V_{ABC}



(b) I_{ABC}

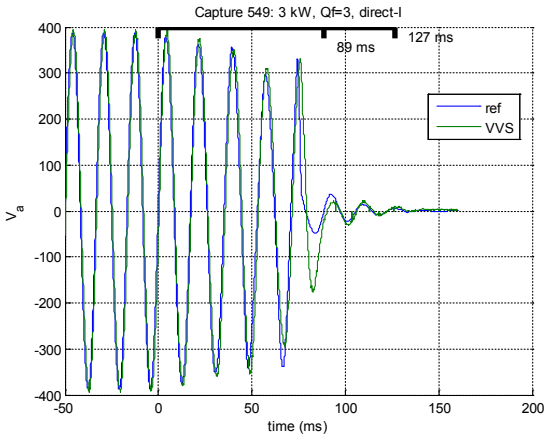


(c) V_{DC}

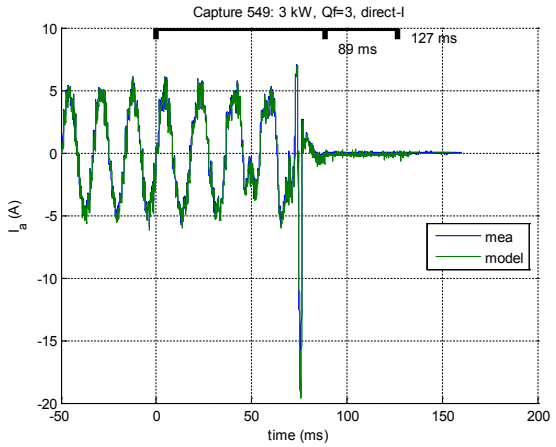


(d) I_{DC}

Figure 24. Inverter 2, modified DQ-PHIL, 3 kW, Qf = 3, Capture 549 (1/2)

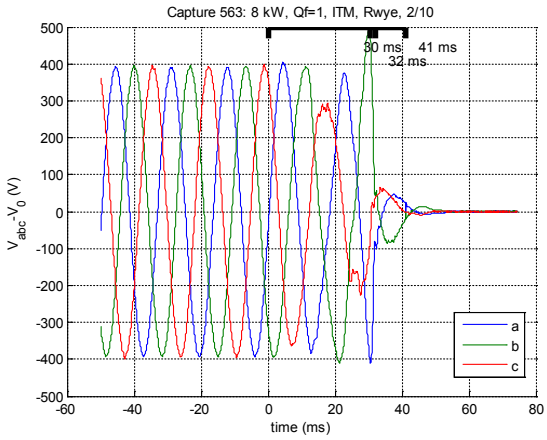


(a) Commanded and measured V_A

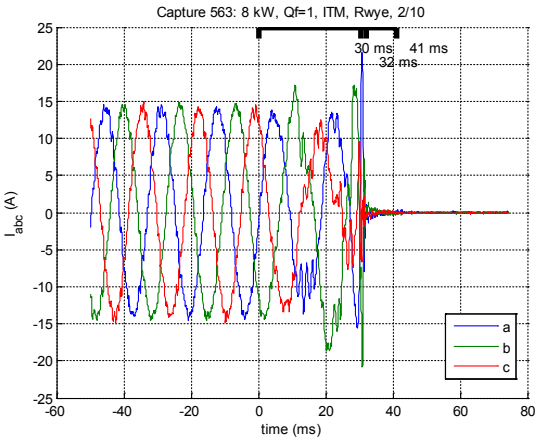


(b) Measured, corrected, and RoS model I_A

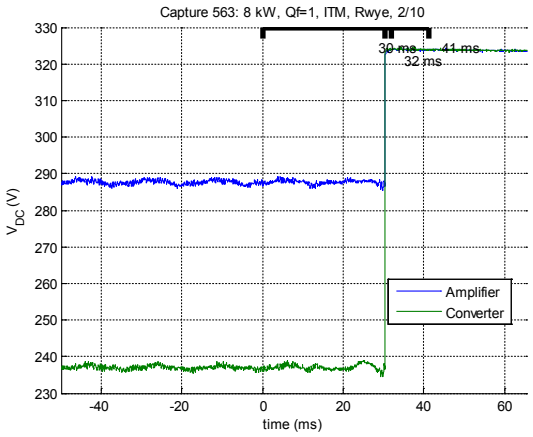
Figure 25. Inverter 2, modified DQ-PHIL, 3 kW, Qf = 3, Capture 549 (2/2)



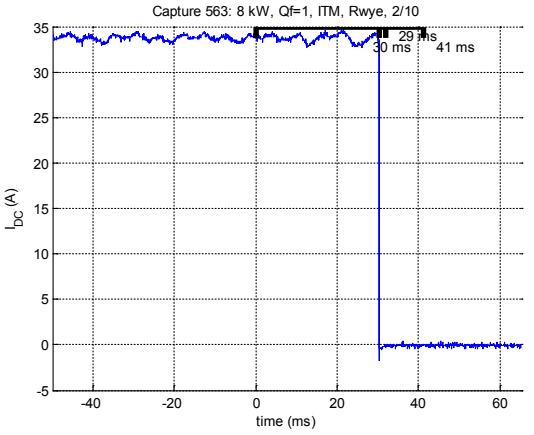
(a) V_{ABC}



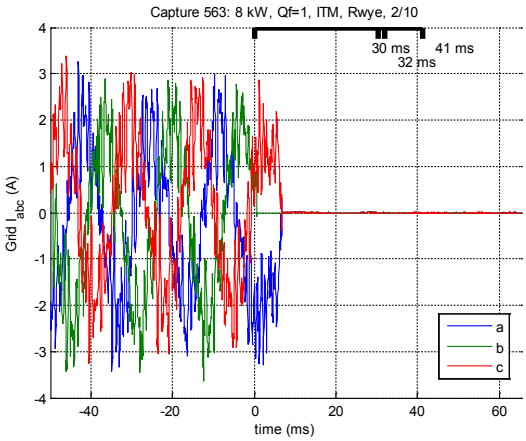
(b) I_{ABC}



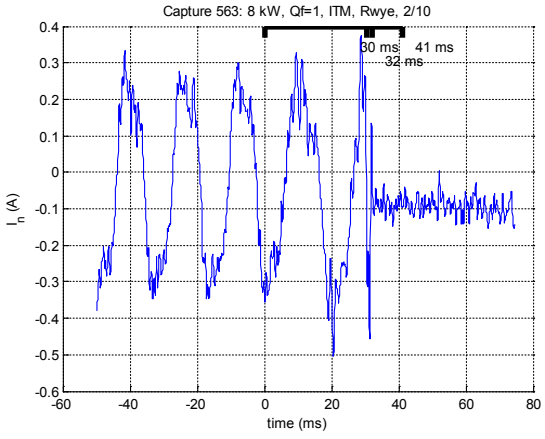
(c) V_{DC}



(d) I_{DC}

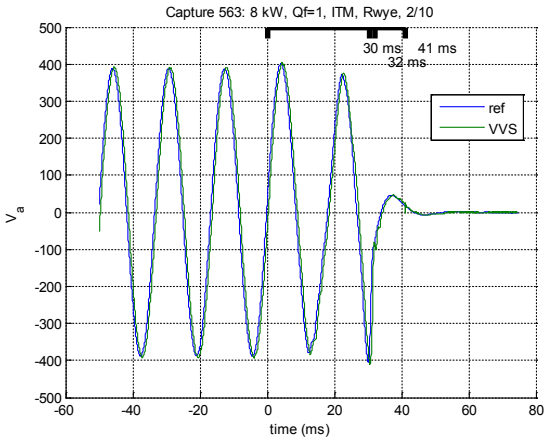


(e) Grid I_{ABC}

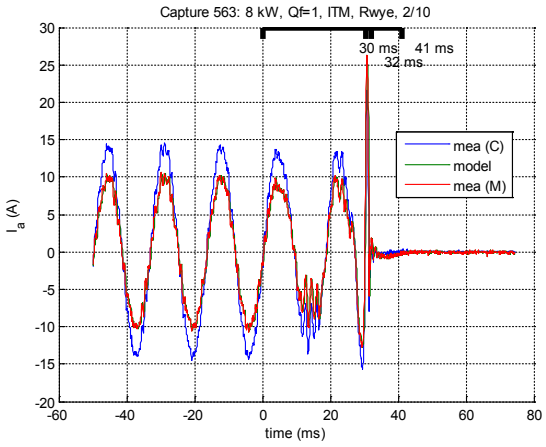


(f) I_n

Figure 26. Inverter 2, ITM-PHIL, 8 kW, Qf = 1, Capture 563 (1/2)



(a) Commanded and measured V_A



(b) Measured, corrected, and RoS model I_A

Figure 27. Inverter 2, ITM-PHIL, 8 kW, Qf = 1, Capture 563 (2/2)

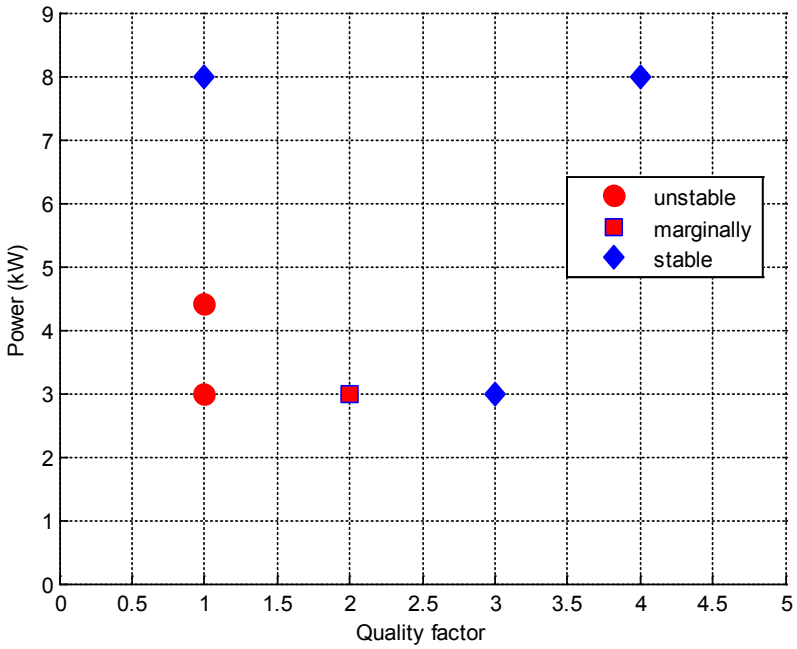
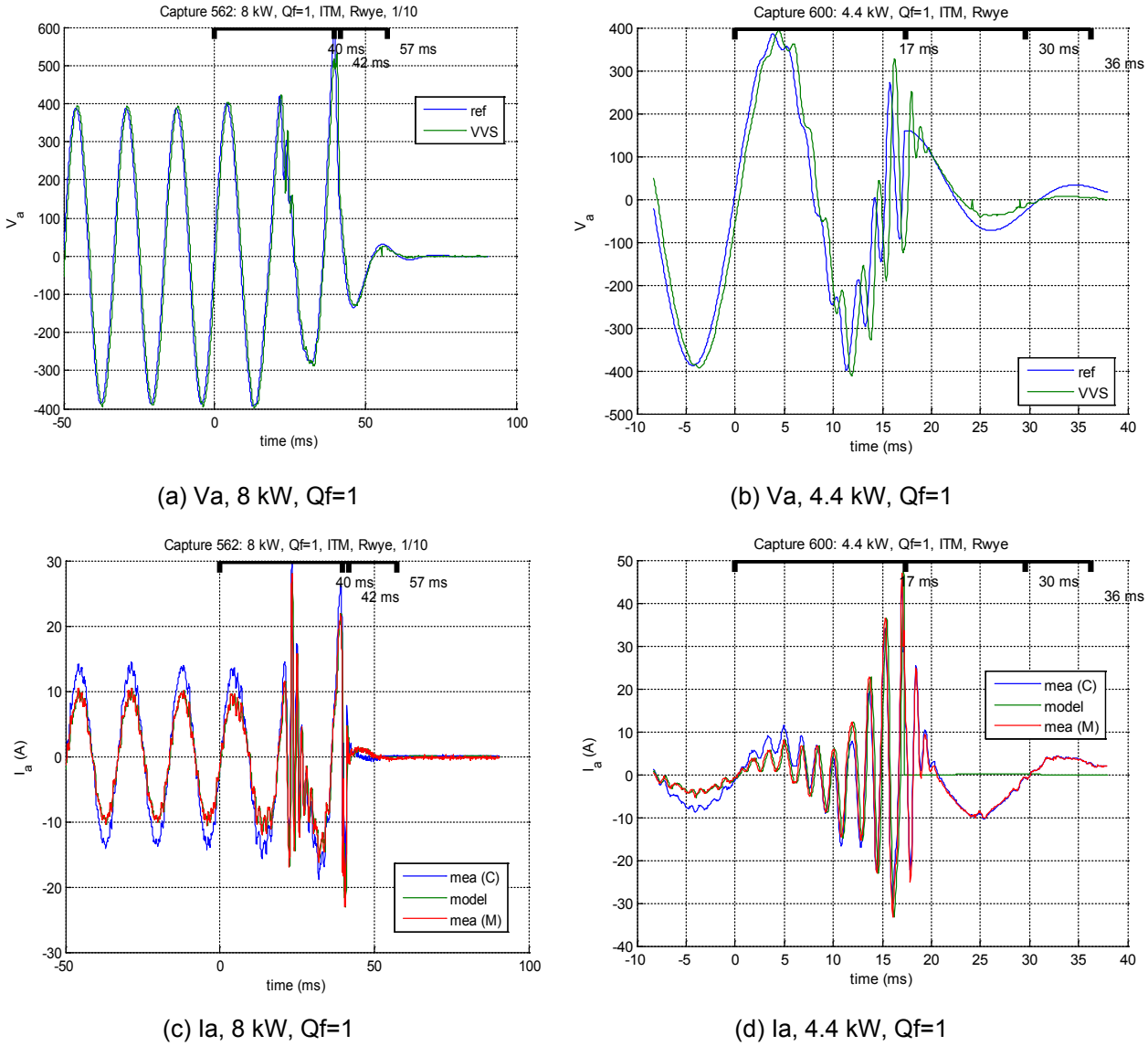


Figure 28. Operating points as classified by stability for ITM-PHIL tests

Examples of PHIL simulation-based testing for successful (stable), (i.e., where commanded voltages and feedback currents closely follow each other), and unsuccessful (unstable) conditions are shown in Figure 29.



(a) Va, 8 kW, Qf=1

(b) Va, 4.4 kW, Qf=1

(c) Ia, 8 kW, Qf=1

(d) Ia, 4.4 kW, Qf=1

Figure 29. Two ITM-PHIL cases (Phase A converter voltage and current): Stable case (left) and unstable case (right)

In the stable case, voltage disturbances are suppressed. In the unstable case, growing oscillations were observed until the experiment was halted.

12.4 Unintentional Island Timing

This section shows analysis with respect to the time that passes between when the AC grid is disconnected and when the PV inverter is turned off. As pointed in Section 12, different means of detecting the point at which the inverter detected an island and turned off are used: AC voltages, AC currents, and DC current levels. We recorded several captures for each of the stable configurations to allow us to better understand the possible distribution of islanding times. Results are plotted with respect to quality factor but with small random offsets to allow results with the same time (duration) response to be distinguished.

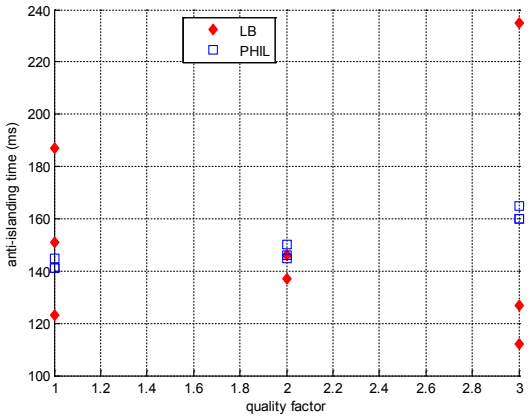
Different PHIL interface algorithms were used to establish best PHIL simulation methods, improve dynamic performance, and increase the stable region of operation. While the load bank was available for testing, unintentional islanding tests were performed for both the RLC load bank and PHIL simulation approach to allow a direct comparison. The following depicts the recorded and analyzed cases.

The first set of results shown in Figure 30 compares the load bank results to the DQ-PHIL approach (additional test points were recorded for additional quality factor settings in PHIL). The tabulated islanding times are given in Appendix B. Comparing the DQ-PHIL simulation to the load bank-derived timing results, the following observations can be made:

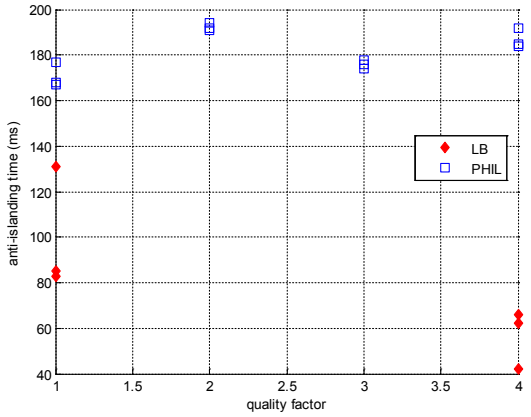
- All chosen operating conditions are stable.
- Unintentional islanding times recorded are comparable to the load bank-based results, but at the medium power level, island times are longer than expected.
- PHIL-based results are more consistent, with much smaller difference between minimum and maximum times.
- Improvements made to voltage tracking (PLL and negative sequence) improved results (i.e., shortened detection times), but performance was not consistent (not shown in the figures).

With respect to the load bank-based tests, we noted in several of the test cases that a second group of outliers in islanding duration emerges. The corresponding longer islanding times may be due to a different destabilizing driving mode of the inverter's island detection algorithm.

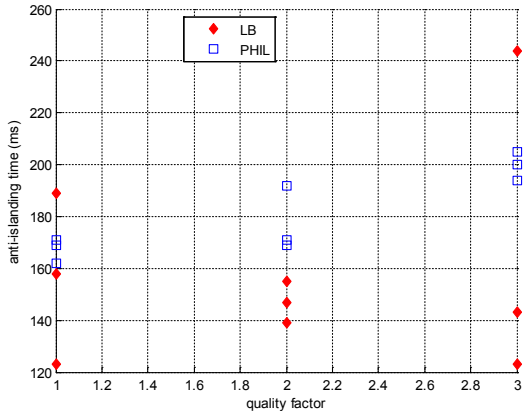
The results derived from the ITM-PHIL interface algorithm (see Figure 31) showed better agreement with the load bank results, but stability of the approach was limited (as indicated in Figure 28). Tabulated islanding times are given in Appendix B.



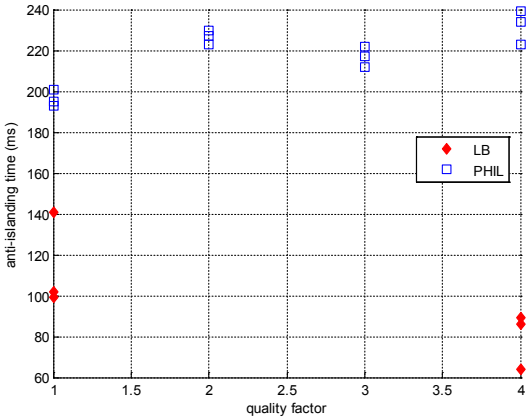
(a) t_{iDC}: 3 kW



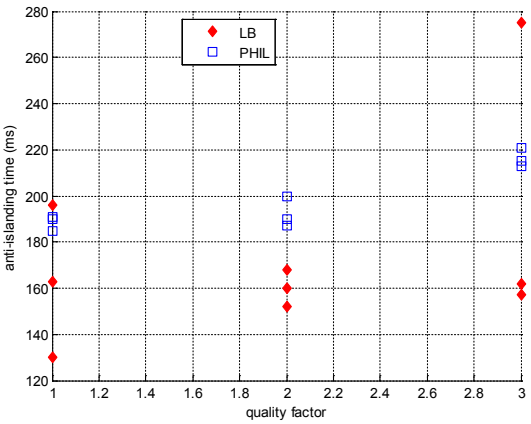
(b) t_{iDC}: 8 kW



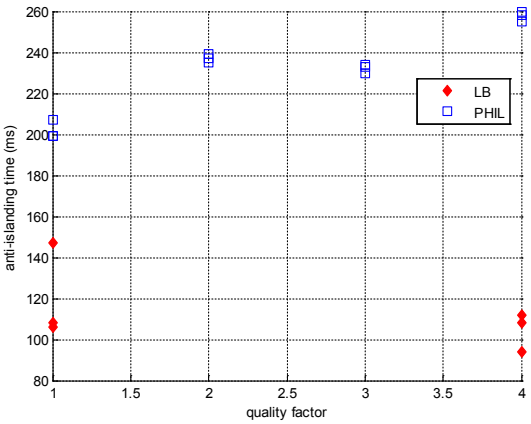
(c) t_{iAC}: 3 kW



(d) t_{iAC}: 8 kW

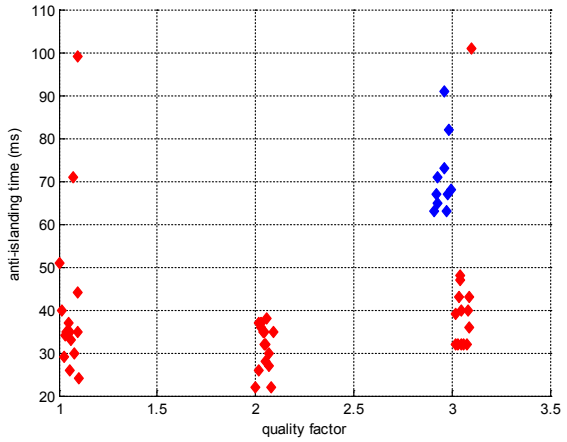


(e) t_{vAC}: 3 kW

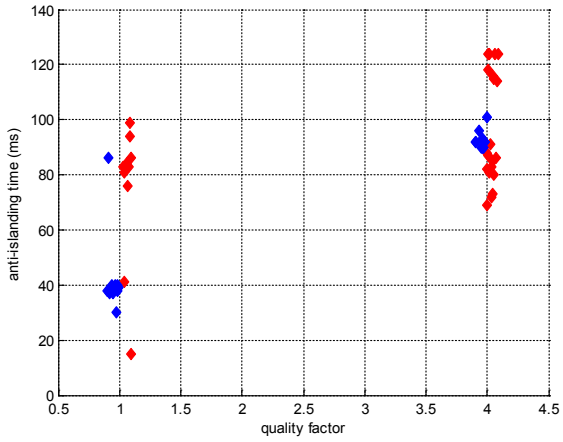


(f) t_{vAC}: 8 kW

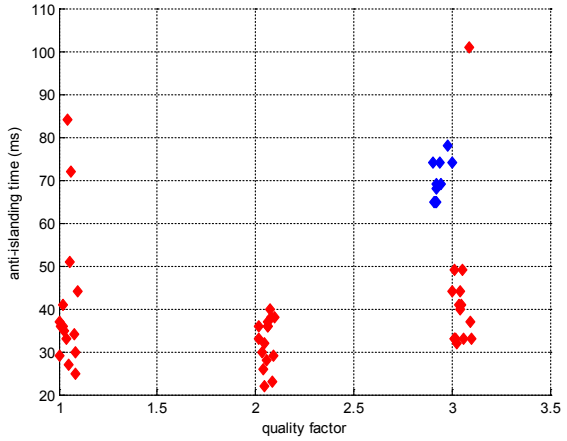
Figure 30. Load bank (red) and DQ- PHIL (blue) timing results



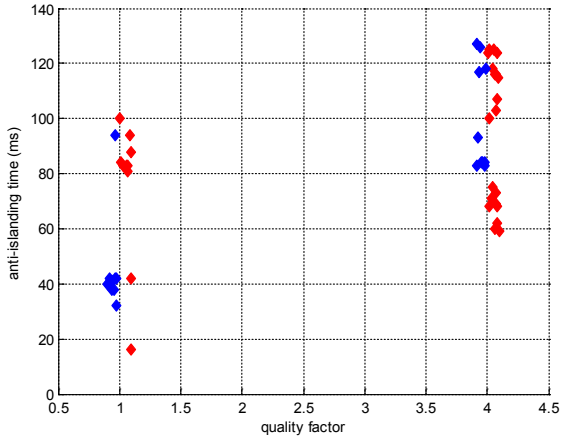
t_{iDC}: 3 kW



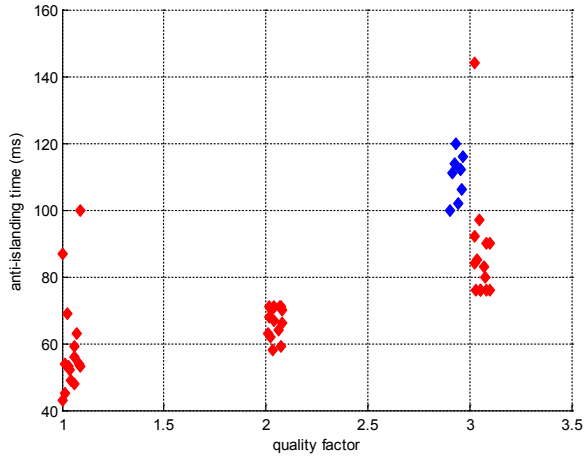
t_{iDC}: 8 kW



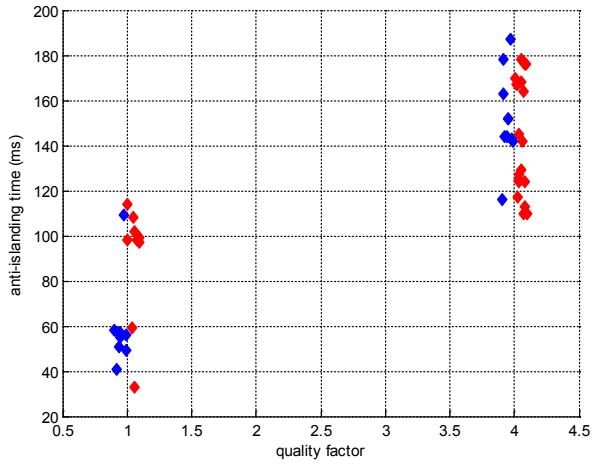
t_{iAC}: 3 kW



t_{iAC}: 8 kW



t_{vAC}: 3 kW



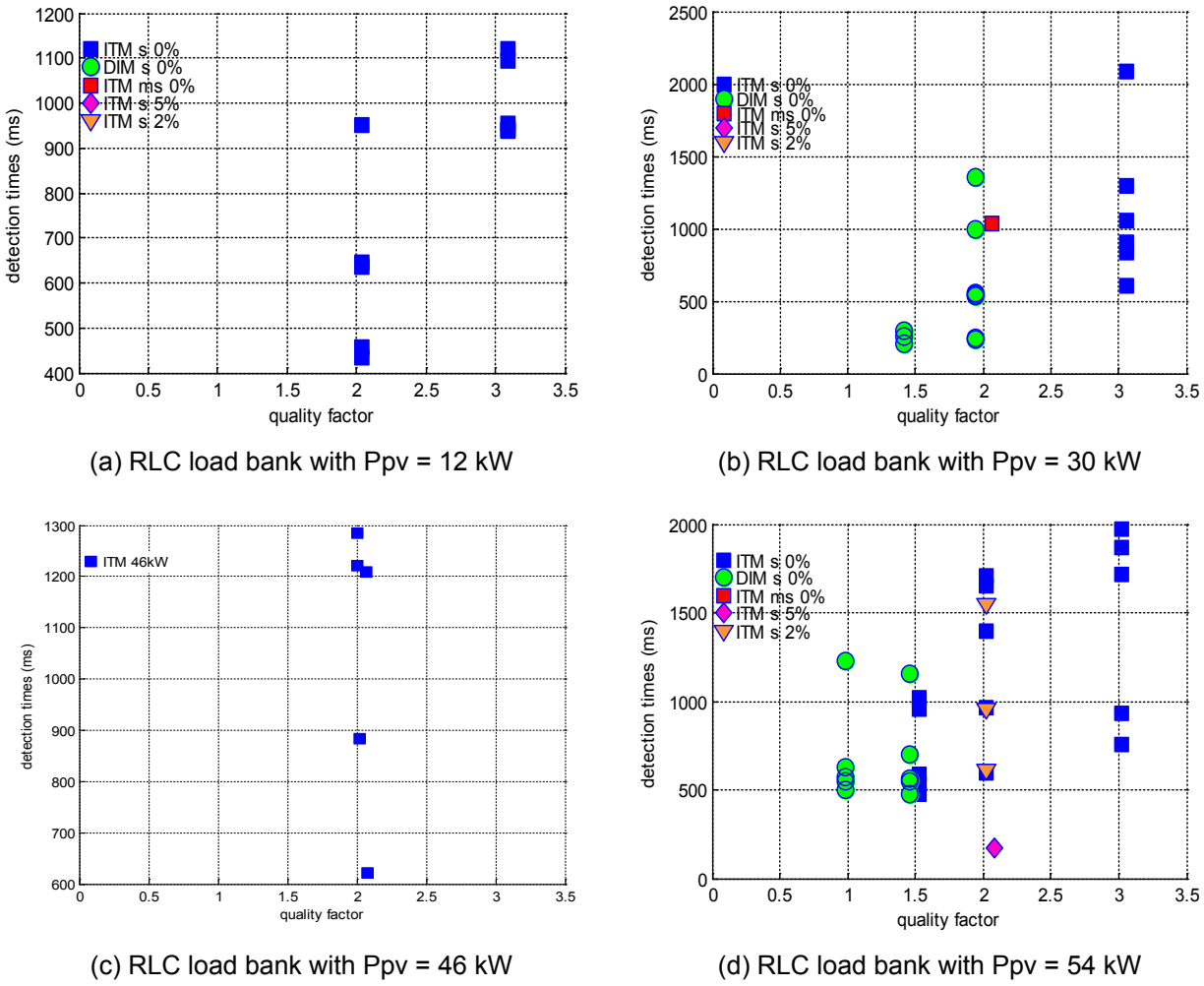
t_{iDC}: 8 kW

Figure 31. Load bank with R_{WYE} (red) and ITM-PHIL (blue) timing results

12.5 PHIL-Based Alternate Conditions

Due to the power limitation of the PV inverters used, another PV inverter was made available for testing, and the results of the subsequent testing are reported in this section. Inverter 3, which had a rating of 60-kW/480V, was used in PHIL arrangement only. It was first tested with a load bank as RoS and followed by various alternate conditions, which included induction motors and constant power injection models at various power and quality factor levels; a detailed description of selected alternate PHIL RoS conditions is given in Section 10.3 and a discussion and literature review are provided in Section 10.2. The DC-side used PHIL simulation to emulate the solar PV array characteristic using ITM as interface algorithms with voltage as output and current as feedback into the RTS model. On the AC-side, primarily the ITM was used but the DIM was applied at lower quality factors. A wide range of the PHIL tests were successful (i.e., stable and viable). At lower quality factors (especially Qf = 1), the stability of experiments was a concern and a limited number of tests could be performed.

This section presents the islanding times recorded, followed by a depiction of stability within the PHIL test regions. Figures 32–34 present details of the operating conditions and PHIL interface algorithms. The following abbreviations are used to denote stability properties: stable (s) and marginally stable (m). The percentage labels (i.e., 0% and 2%) refer to the inductive and capacitive reactive power mismatch level.



(a) RLC load bank with Ppv = 12 kW

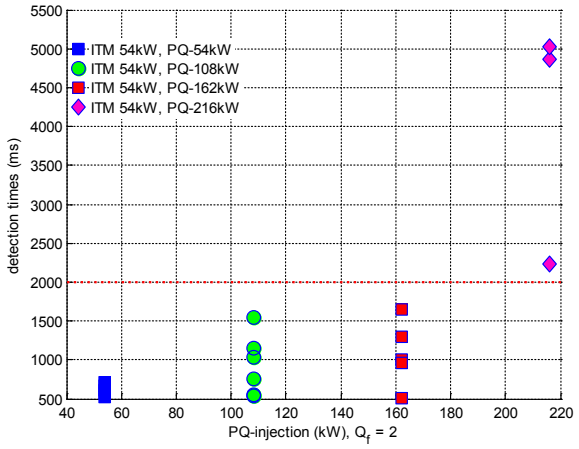
(b) RLC load bank with Ppv = 30 kW

(c) RLC load bank with Ppv = 46 kW

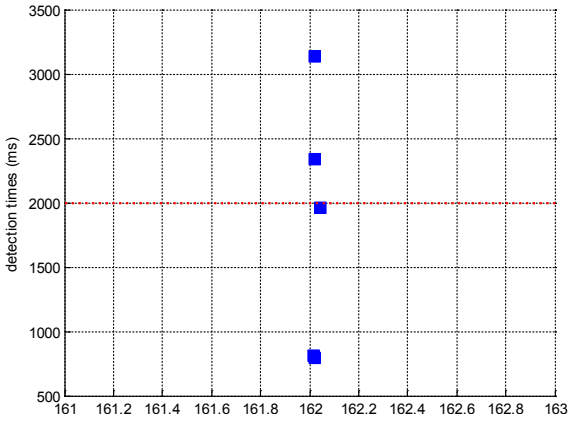
(d) RLC load bank with Ppv = 54 kW

Figure 32. Inverter 3: PHIL-based RLC load bank tests

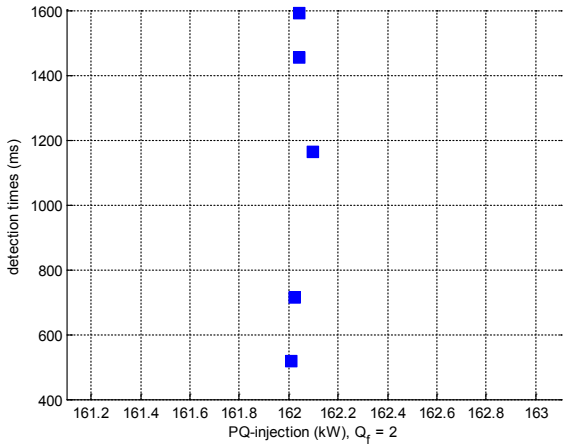
All but one of the stable load bank test conditions yielded detection times within the required 2.0 seconds (Figure 32). A slightly longer lasting island of 2.089 seconds occurred at the 50% power level (30 kW) and quality factor of 3. Some of the results based on inclusion of the PQ-injection model as part of the RoS show longer times. To allow evaluating the cases with possible longer island times, the unintentional islanding experiment timer (watchdog to halt experiments in case of run-ons) was modified from the default 2.2 seconds to 5.0 seconds. Therefore, times that are at these values indicate not that the solar PV inverter turned off but that the PHIL experiment was stopped.



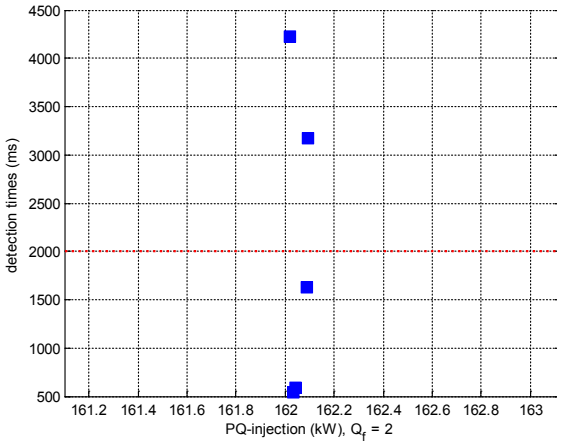
(a) PQ-injections



(b) PQ-injections with V-var: 50 kvar

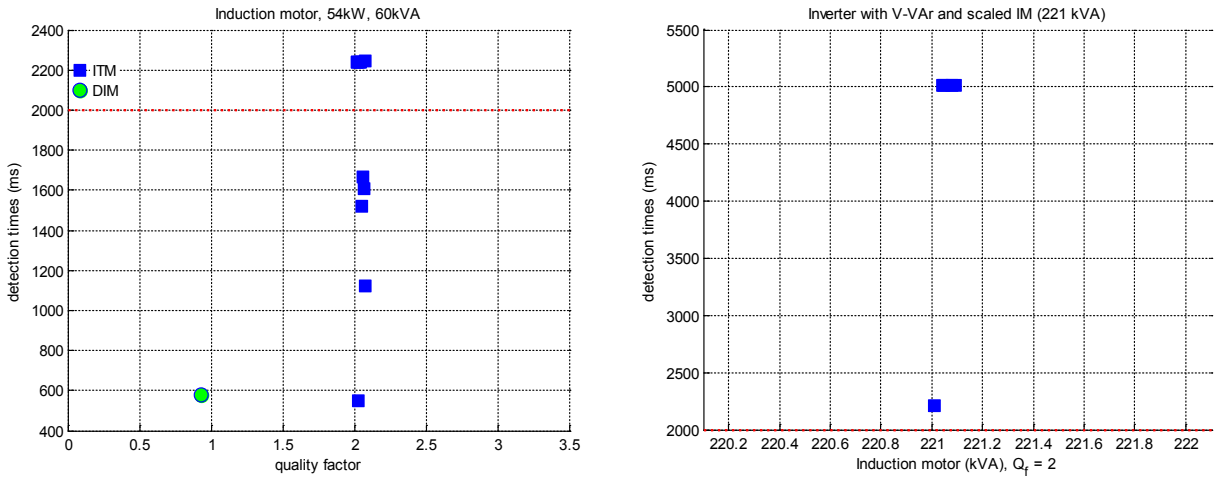


(c) PQ-injections and inverter with V-var



(d) PQ-injections with V-var: 25 kvar, 100 kvar/s

Figure 33. Inverter 3: PHIL-based constant-PQ tests (horizontal red line at 2000 ms indicates IEEE Standard 1547 upper limit)

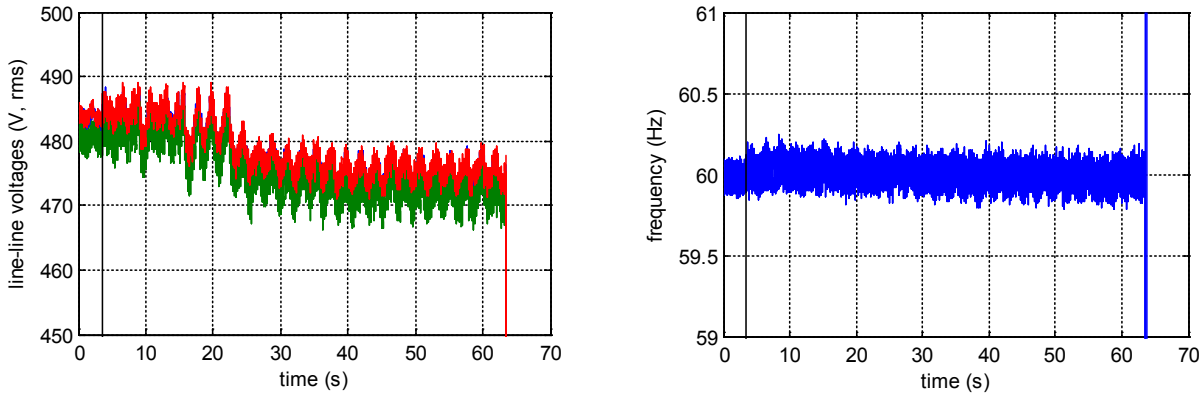


(a) Induction motor: 54 kW, 60 kVA

(b) Induction motor: 54 kW, 221 kVA

Figure 34. Inverter 3: PHIL-based induction motor tests

The induction motor-based results are shown in Figure 34. In case of the motor with nominal 60 kVA, 5 out of the 10 tests resulted in times longer than 2.0 seconds (between 2.2 and 2.3 seconds). In case of the 221 kVA rated motor, each test resulted in longer run-on times (all times shown in (b) indicate that the test was halted). Because of these results, several 60-second islanding tests were performed, and the islands were not detected. Again, it has to be noted that these tests used an equivalent quality factor of 2. The corresponding time domain measurements of rms-voltages and frequency for these cases are shown in Figure 35. The black vertical line at 3.5 seconds indicates the beginning of islanding conditions. The experiment is halted after 60 seconds.



(a) Line-Line rms-voltages

(b) Frequency

Figure 35. Inverter 3: PHIL-based induction motor tests, rms-voltages and frequency for an extended island case (54 kW, 221 kVA)

Figure 36 presents an overview of the conditions tested, including annotations of stability and parameter settings. The stability boundary for the Inverter 3 tests seems to be more influenced by the quality factor than by the power level. The DIM extended the stable operation to Qf = 1 for the 90% power level and load bank RoS model

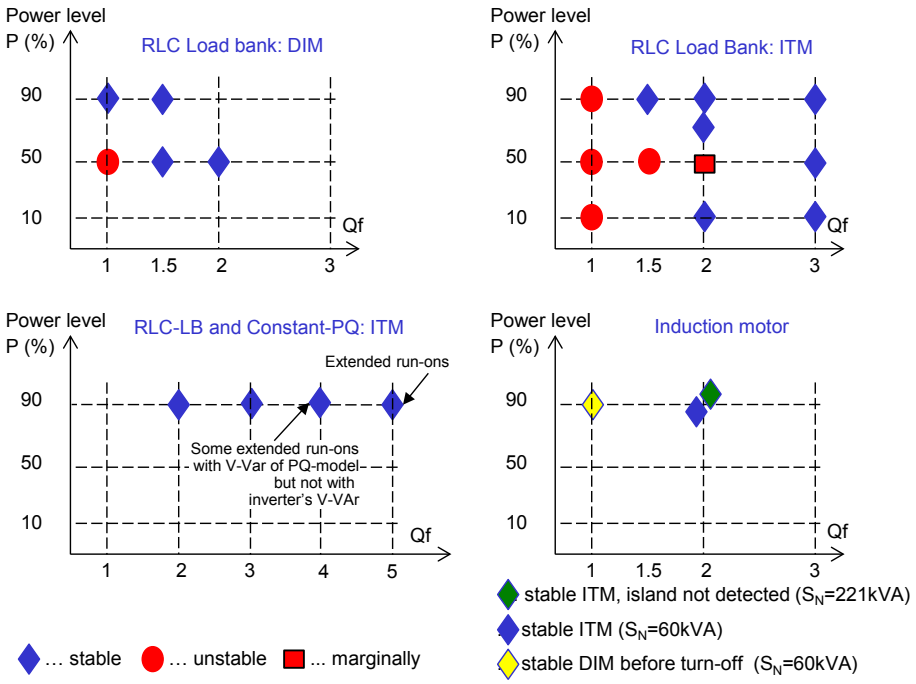


Figure 36. Inverter 3: Test conditions and stability overview

We have drawn the following conclusions from the experiments with the alternate conditions:

- RLC load bank tests were successful and repeatable for quality factors above Qf = 1.5 for ITM. DIM was stable at Qf = 1 for the higher power level (90%). Tests using lower quality factors were hindered by stability issues. Only one test (30 kW, Qf = 3) yielded a detection time longer than 2.0 seconds (2.089 s).
- ***Induction motor tests, equivalent rating*:** This test configuration indicated a 50% possibility for prolonged run-on times. The quality factor used (Qf = 2) was higher than the IEEE Standard1547 testing requirement (Qf = 1).
- ***Scaled induction motor and V-var control active*:** All tests with an induction motor of 221 kVA (about four times PV-power output and rating and Qf = 2) showed prolonged run-on times. Several 60-second islanding tests were performed and the island was not detected.
- ***Constant PQ-model*:** This model represents other constant power injections such as PV inverters but without active unintentional islanding algorithms. Some of the tests resulted in prolonged run-on times at higher power levels (i.e., at four times the tested PV inverter's rating. When V-var control actions were included in the power injection models, the required power level was reduced (to three times PV rating) but detection times varied greatly and no conclusion with respect to island detection issues could be drawn.
- ***Constant PQ-model and inverter with active V-var controls*:** Tests with constant PQ-injections were repeated at three times the PV-power level but with the PV inverter's V-var controls active. No islanding detection issues were observed.

13 Discussion

The unintentional islanding test methods present several general concerns and challenges specific to the PHIL simulation approach:

1. To detect an islanding condition the PV inverter perturbs the interconnected electric system. These perturbances tend to destabilize the electric system. Therefore, the test system is inherently unstable, and test results cannot be reproduced in a truly repeatable fashion. Only patterns of behavior may emerge that allow comparison of the load bank and PHIL approaches.
2. The resonant RLC load bank is prone to cause high levels of harmonic currents if the supply voltage waveform is not ideal or contains harmonic components. Furthermore, if using a grid supply, the supply voltage harmonic content may depend on the day and time of the day (i.e., dependent on system loading), and therefore cause different levels of harmonic current to be recorded in experiments (before islanding, which complicates zeroing-out the grid current component).
3. Variations due to tolerances in the discrete RLC load bank inductors and capacitors will lead to mismatched resistive and reactive power components.
4. The PHIL approach can allow for perfectly matched ideal inductive and capacitive components, and it even allows the user to change inductor and capacitor values while the test is operating. Nevertheless, changing any component, especially the inductance, can cause sustained oscillations that may need to be intermittently counteracted through a resistive damping component.
5. Instability is an issue with the ITM interface algorithm for these types of tests. The stability of this algorithm is largely based on the ratio of the impedance of the RoS and the impedance of the DUT. Thus, the abrupt change in the impedance of the RoS when opening the islanding switch poses a challenge for this algorithm. The DIM algorithm has been successfully employed to widen the region of stability, but stability limits were also encountered with this approach.

As this project demonstrated, the PHIL simulation approach for testing unintentional islanding conditions shows significant promise. A wide range of load bank-based RoS conditions and various alternate conditions could be implemented as part of the real-time emulated island. Only this flexibility in implementation and its repeatability—as the models can be appropriately documented and shared—will support the studies required to identify the need and appropriateness of alternate test conditions. The efficacy and possibility for automation of PHIL simulation testing will reduce costs and make advanced test conditions feasible.

As outlined above, several challenges remain and warrant further investigations:

1. **Improvements in PHIL simulation interface algorithms:** From a PHIL simulation perspective, interface methods such as the modified DIM [15], [16], [17] in which the damping impedance is adapted online based on the measured impedance of the DUT, may allow further widening the region of stability and improvement in accuracy. The online impedance identification would avoid the need to know the inverter's impedance characteristics explicitly.
2. **Determinations of alternate test conditions:** Both the increased deployment of distributed generation resources and the varying mix of loads on today's distribution feeders complicates finding a unique, best RoS model that appropriately reflects the worst case conditions to be expected and detected. We are uncertain whether a passive load model sufficiently reflects circuit behavior, even when limited to narrow voltage and frequency ranges as the amount of controlled equipment steadily increases. Because of the rapid expansion of distributed resources, high-penetration situations are already becoming a reality for several electric utilities. Even though the burden of detecting islands in more difficult conditions may not be with inverters alone; current protection practices are prone to missing islanding condition initiation when, for example, the distribution circuit to which the inverter is connected includes induction motors. Investigations should be performed to derive RoS models that better reflect a range of known and projected system configurations.
3. **Determinations of non-detection zones:** The tests reported herein were based on matching solar PV output power to RoS conditions (i.e., zero net active and reactive power flows from the grid). It is important to test the possibility of extended island situations in conditions that do not match those at the time the island occurs (i.e., to determine the non-detection zones for the alternate RoS conditions). For example, a parametric study of an islanded system that includes induction motors under conditions of unmatched active and reactive power levels. We feel this would provide valuable input to future test design, and it would help researchers understand the risks involved—especially with the possibility of more advanced inverter functions, such as volt-var controls, being actively used in the near future.
4. **Standardized modeling and simulation:** When combined with current utility distribution feeder planning and analysis, modeling and simulation have an important role in developing and implementing new technology. Nevertheless, no current standardization efforts are underway to support best practices in modeling or simulating equipment and systems. For example, integration of PV inverters as components of distributed resource is handled in a case-by-case fashion, with individual non-disclosure agreements signed by the parties involved. This approach will become intractable in the near future and standardized means of exchanging model structure, parameters, and corresponding assumptions made and applicability will become important. We suggest initiation efforts be made within standardization bodies to develop modeling and simulation requirements and guidelines, including PHIL-based methods in those standards.

14 Conclusions

This project investigated the use of PHIL simulation to test a crucial safety aspect of today's solar PV inverters: their capability to detect the need to cease feeding power into the distribution feeder. The relevant U.S. standards for interconnection of distributed resources—IEEE Standards 1547 and 1547.1—require that tests be performed using discrete RLC load banks. The costs of providing properly sized load banks for every possible power rating, as well as the rapidly growing system sizes feasible with advanced power electronics, makes this approach both rigid and expensive. Any improvement in the test scenario, or associated cost reductions, could yield enormous benefits to both the inverter manufacturing and the electric utility industries.

The PHIL simulation-based approach has been used to demonstrate the capabilities and possibilities it provides in subjecting a power system apparatus to conditions that could otherwise be achieved only in the field. Examples of PHIL simulation-based tests performed with respect to solar PV inverters include testing steady-state operating conditions, abnormal voltage and frequency conditions, and advanced inverter control functions while emulating feeder characteristics at the inverter's terminals. These tests have been performed with inverters rated up to one MW. The unintentional island tests are challenging due to the inherent instability of test conditions, resulting in tests that are very difficult to accurately reproduce.

In this project, we succeeded in applying the PHIL approach to unintentional islanding tests in a wide range of selected rest-of-system model cases. PHIL simulation setups were stable for qualify factors above one, but tests were less successful when performed at low quality factors and low power levels. We were able to partially improve stable operating regions by altering aspects of the PHIL interfacing algorithms, but not all limitations could be overcome. The difficulties encountered are due to inherent limitations imposed by the hardware (i.e., primarily the power amplifiers, communication delays, and control bandwidth limitations).

One of the benefits of PHIL simulation-based testing is its flexibility and efficiency in establishing alternate test conditions. Consequently, the PHIL simulation approach opens the door to cost effectively probe for proper islanding mechanisms and explore whether conditions other than RLC load bank-based RoS conditions are of concern and should be considered. In the case scenarios tested herein, we confirmed the possibility of extended run-ons in cases that include larger induction machines as part of the island.

The positive outcomes of this first attempt to systematically explore the possibility to test for unintentional islanding using the PHIL simulation approach are encouraging. As the current standard requirement in unintentional islanding testing concerns quality factors of and about one—which could not be reached in a broad enough set of test scenarios—further investigations into improving PHIL interface algorithms and requirements on power amplifiers are warranted.

Selected tested conditions have shown that models other than RLC load bank RoS models do make it more difficult to detect island situations. These conditions were based on assumptions for models of other power electronic devices and motors connected to the islanded system. We feel four additional investigations should be conducted to address the concerns raised. First, determine the risk of extended islanding conditions—and test for viable alternate conditions—under conditions of unmatched active and reactive power levels. Second, identify corresponding RoS models that unify and standardize test conditions. Third, improve PHIL simulation

technology and interface algorithms. Fourth, initiate modeling and simulation standardization efforts that incorporate and support requirements for PHIL simulation-based modeling.

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Appendix A. Data for Salient Hardware Components

The tables in this appendix summarize the most important hardware components used during the various project stages.

Table A-1. List of Main Equipment Used

Function	Device(s)	Description	Data, Rating, and Limits
DC amplifier	VVS-DC	DC chopper; four-quadrant operation capable; voltage or current mode; effective 10 kHz switching frequency	max. 1,150 V, 1.25/2.5 M**W**
AC amplifier	VVS-AC	Voltage-source converter; four-quadrant operation capable; effective 10 kHz switching frequency	maximum 4.16 kV, 1.25/2.5 MW; variable frequency of about 45-75 Hz (with reduced voltages depending on transformer)
DC amplifier	Three AE Techron 7780	Linear amplifiers in series; two-quadrant operation	20 A/V amplifier gain, 37.8 $A_{DC,max}$, 350 $V_{DC,max}$, 20 A_{DCmax} at 300 V
Transformer (T)		4.16 kV Delta/480-V Wye	1.5 MVA, x=5.21%, 60 Hz
Real-time simulator (RTS)	RTDS	Experiment controls, monitoring, protection, simulation	RTS simulation time step of 50 µs
DC series resistance	Resistor	High-power resistors, possibly used resistors between VVS-DC-side and PV inverter	3.4 ohm / 80 A, 12 available
DC parallel resistance	Resistor	High-power resistors, possibly used in parallel to VVS-DC	39 ohm
DC bus diode	High-current diode	Blocking reverse current	n/a
RLC load bank	Simplex custom load bank	Thirteen discrete, switchable elements each (R, L, and C)	436 kVA, 480 V, three-phase, 60 Hz, delta-connected

Table A-2. Inverter 1 Data

Aspect	Property	Value
Input (DC)	Max. DC power (@ cos φ=1)	17,410 W
	Max. input voltage	1,000 V
	MPP voltage range / rated input voltage	400 V – 800 V / 600 V
	Min. input voltage / initial input voltage	150 V / 188 V
	Max. input current input A / input B	33 A / 11 A
	Number of independent MPP inputs / strings per MPP input	2 / A:5; B:1
Output (AC)	Rated power (@ 230 V, 50 Hz)	17,000 W
	Max. apparent AC power	17,000 VA
	Nominal AC voltage	3 / N / PE; 220 / 380 V 3 / N / PE; 230 / 400 V 3 / N / PE; 240 / 415 V
	Nominal AC voltage range	160 V – 280 V
	AC power frequency / range	50 Hz, 60Hz / -6 Hz − +5 Hz
	Rated grid frequency / rated grid voltage	50 Hz / 230 V
	Max. output current	24.6 A
	Power factor at rated power	1
	Input-side disconnection device	yes
	Ground-fault monitoring / grid monitoring	yes / yes

Table A-3. Inverter 2 Data

Aspect	Property	Value
Input (DC)	Max. DC power (@ cos φ=1)	20,400 W
	Max. input voltage	1,000 V
	MPP voltage range / rated input voltage	380 V – 800 V / 695 V
	Min. input voltage / initial input voltage	150 V / 188 V
	Max. input current input A / input B	33 A / 33 A
	Number of independent MPP inputs / strings per MPP input	2 / A:1; B:1
Output (AC)	Rated power (@ 277 V, 60 Hz)	20,000 W
	Max. apparent AC power	20,000 VA
	Nominal AC voltage	3 / N / PE; 480/277V WYE
	Nominal AC voltage range	243.7 V – 304.7 V
	AC power frequency / range at 60 Hz	59.3 Hz – 60.5Hz
	Rated grid frequency	60 Hz
	Max. output current	24.1 A
	Power factor at rated power	1
	Ground-fault monitoring / grid monitoring	yes / yes
	DC surge arrester Type II (can be integrated)	opt.
	DC reverse-polarity protection / AC short-circuit current capability / galvanically isolated	diode / current control / no
	All-pole sensitive residual current monitoring unit	yes

Table A-4. Inverter 3 Data

Aspect	Property	Value
Input (DC)	Max. input voltage	600 V
	MPP voltage range	230 V – 500 V
	Initial input voltage	265 V
	Max. input current	280 A
	Max. array short circuit current	420 A
	DC insulation warning shutdown	< 500 kOhm
	DC circuit breaker	integrated
	Galvanically isolated (DC-side from grid)	yes
Output (AC)	Rated power (@ 277 V, 60 Hz)	60 kW
	Max. AC power	60 kW
	Nominal AC voltage	3 / N / PE; 480/277V WYE
	Nominal AC voltage range	243.7 V – 304.7 V
	AC current at 244V	90 A
	AC power frequency / range at 60 Hz	59.3 Hz – 60.5Hz
	Rated grid frequency	50-60 Hz
	Nominal output current	87 A
	Max. output fault current / duration	1,020 A / 510 us
	Insulation monitoring / grid monitoring	yes / yes

Table A-5. Simplex RLC Load Bank Element Data

Property	Value(s)
13 resistors[a]	[50 50 25 17 10 5 2 1 1 0.5 0.250 0.125 0.125] kW @ 480 V [13.8 13.8 27.6 40.7 69.1 138.2 345.6 691.2 691.2 1382.4 2764.8 5529.6 5529.6] ohm
13 inductors[a]	[125 125 62.5 42.5 25 12.5 5 2.5 2.5 1.25 0.625 0.3125 0.3125] kVA @ 480 V [14.7 14.7 29.3 43.1 73.3 146.7 366.7 733.4 733.4 1466.8 2933.5 5867.1 5867.1] mH
13 capacitors[a]	Power rating: same as for inductors [479.7 479.7 239.9 163.1 95.9 48.0 19.2 9.6 9.6 4.8 2.4 1.2 1.2] µF

[a] Thirteen individual components yield a total of 2^{13}-1 = 8,191 combinations, of which 1,296 combinations are unique. All RLC values shown are based on nominal voltage/power and delta-connection. Actual load bank design is different and uses multiple components to implement individual power levels.

Appendix B. Timing Data for Unintentional Islanding Tests

B.1 RLC and PHIL-Based Tests (Inverter 2)

Tables B-1 through Table B-9 summarize the test results for two of the test sets performed while using Inverter 2. The results listed are for both RLC load bank (LB) and PHIL simulation methods.

Table B-1. Timing Results for Load Bank and DQ-PHIL-Based Testing (Inverter 2)

P (kW)	Q_f	Type	Capture	$t_{AID,V\ ac}$ (ms)	$t_{AID,Iac}$ (ms)	$t_{AID,Idc}$ (ms)
8.000	1.0	PHIL	403	199	195	167
8.000	1.0	PHIL	404	207	201	177
8.000	1.0	PHIL	405	199	193	168
8.000	2.0	PHIL	409	235	223	191
8.000	2.0	PHIL	410	237	230	192
8.000	2.0	PHIL	411	239	227	194
8.000	3.0	PHIL	412	234	222	178
8.000	3.0	PHIL	413	233	217	176
8.000	3.0	PHIL	414	230	212	174
8.000	4.0	PHIL	406	260	239	192
8.000	4.0	PHIL	407	255	223	184
8.000	4.0	PHIL	408	258	234	185
3.125	1.0	PHIL	392	185	162	141
3.125	1.0	PHIL	393	191	169	145
3.125	1.0	PHIL	394	190	171	141
3.125	2.0	PHIL	395	187	169	145
3.125	2.0	PHIL	396	200	192	150
3.125	2.0	PHIL	397	190	171	146
3.125	3.0	PHIL	398	215	205	160
3.125	3.0	PHIL	399	221	200	165
3.125	3.0	PHIL	400	213	194	160
8.000	1.0	LB	330	147	141	131
8.000	1.0	LB	331	108	102	85
8.000	1.0	LB	332	106	99	83
8.000	4.0	LB	334	112	89	66
8.000	4.0	LB	335	108	86	62
8.000	4.0	LB	336	94	64	42
3.125	1.0	LB	338	196	189	187

P (kW)	Q_f	Type	Capture	$t_{AID,V\ ac}$ (ms)	$t_{AID,Iac}$ (ms)	$t_{AID,Idc}$ (ms)
3.125	1.0	LB	339	130	123	123
3.125	1.0	LB	340	163	158	151
3.125	2.0	LB	342	160	147	146
3.125	2.0	LB	343	152	139	137
3.125	2.0	LB	344	168	155	146
3.125	3.0	LB	346	157	123	112
3.125	3.0	LB	348	275	244	235
3.125	3.0	LB	350	162	143	127

Table B-2. Timing Results for Load Bank with R_{WYE} (Inverter 2): 8 kW, Qf=1

P (kW)	Q_f	Type	Capture	$t_{AID,V\ ac}$ (ms)	$t_{AID,Iac}$ (ms)	$t_{AID,Idc}$ (ms)	Angle (deg)
8.000	1.0	LB	451	108	94	94	212
8.000	1.0	LB	452	114	100	99	246
8.000	1.0	LB	453	98	83	81	345
8.000	1.0	LB	476	102	88	83	26
8.000	1.0	LB	477	98	83	84	329
8.000	1.0	LB	478	99	84	86	138
8.000	1.0	LB	479	97	81	76	90
8.000	1.0	LB	480	59	42	41	63
8.000	1.0	LB	481	98	83	83	342
8.000	1.0	LB	482	33	16	15	208

Table B-3. Timing Results for Load Bank with R_{WYE} (Inverter 2): 8 kW, Qf=4

P (kW)	Q_f	Type	Capture	$t_{AID,V\,ac}$ (ms)	$t_{AID,Iac}$ (ms)	$t_{AID,Idc}$ (ms)	Angle (deg)
8.000	4.0	LB	454	117	68	80	332
8.000	4.0	LB	455	167	116	115	269
8.000	4.0	LB	456	127	71	83	283
8.000	4.0	LB	483	170	118	118	206
8.000	4.0	LB	484	177	125	124	212
8.000	4.0	LB	485	164	107	87	171
8.000	4.0	LB	486	168	116	116	249
8.000	4.0	LB	487	125	69	82	136
8.000	4.0	LB	488	176	124	124	235
8.000	4.0	LB	489	178	124	124	343
8.000	4.0	LB	490	110	59	69	201
8.000	4.0	LB	491	176	125	124	225
8.000	4.0	LB	492	145	103	91	85
8.000	4.0	LB	493	129	73	85	41
8.000	4.0	LB	494	124	68	81	332
8.000	4.0	LB	495	142	100	88	166
8.000	4.0	LB	496	124	75	86	152
8.000	4.0	LB	497	110	60	72	329
8.000	4.0	LB	498	167	115	114	92
8.000	4.0	LB	499	113	62	73	284

Table B-4. Timing Results for Load bank with R_{WYE} (Inverter 2): 3 kW, Qf=1

P (kW)	Q_f	Type	Capture	$t_{AID,V\,ac}$ (ms)	$t_{AID,Iac}$ (ms)	$t_{AID,Idc}$ (ms)	Angle (deg)
3.000	1.0	LB	442	100	84	99	284
3.000	1.0	LB	443	56	37	37	284
3.000	1.0	LB	444	48	29	29	89
3.000	1.0	LB	500	54	36	35	105
3.000	1.0	LB	501	87	72	71	284
3.000	1.0	LB	502	53	35	35	221
3.000	1.0	LB	503	49	30	30	259
3.000	1.0	LB	504	43	25	24	296
3.000	1.0	LB	505	63	44	44	341
3.000	1.0	LB	506	45	27	26	12
3.000	1.0	LB	507	54	36	35	104
3.000	1.0	LB	508	59	41	40	340
3.000	1.0	LB	509	69	51	51	20
3.000	1.0	LB	510	53	34	34	182
3.000	1.0	LB	511	52	33	33	61

Table B-5. Timing Results for Load Bank with R_{WYE} (Inverter 2): 3 kW, Qf=2

P (kW)	Q_f	Type	Capture	$t_{AID,V\,ac}$ (ms)	$t_{AID,Iac}$ (ms)	$t_{AID,Idc}$ (ms)	Angle (deg)
3.000	2.0	LB	448	67	32	32	40
3.000	2.0	LB	449	71	36	35	289
3.000	2.0	LB	450	64	29	28	98
3.000	2.0	LB	524	68	33	32	27
3.000	2.0	LB	525	71	40	38	43
3.000	2.0	LB	526	63	28	27	123
3.000	2.0	LB	527	58	22	22	67
3.000	2.0	LB	528	59	23	22	235
3.000	2.0	LB	529	62	26	26	322
3.000	2.0	LB	530	71	36	35	121
3.000	2.0	LB	531	71	37	36	101
3.000	2.0	LB	532	70	36	35	127
3.000	2.0	LB	533	66	30	30	220
3.000	2.0	LB	534	70	38	37	218
3.000	2.0	LB	535	70	38	37	39

Table B-6. Timing Results for Load Bank with R_{WYE} (Inverter 2): 3 kW, Qf=3

P (kW)	Q_f	Type	Capture	$t_{AID,V\ ac}$ (ms)	$t_{AID,Iac}$ (ms)	$t_{AID,Idc}$ (ms)	Angle (deg)
3.000	3.0	LB	445	76	33	32	165
3.000	3.0	LB	446	76	33	32	341
3.000	3.0	LB	447	76	32	32	88
3.000	3.0	LB	512	90	44	43	247
3.000	3.0	LB	513	76	33	32	87
3.000	3.0	LB	514	92	49	47	5
3.000	3.0	LB	515	83	40	39	220
3.000	3.0	LB	516	144	101	101	14
3.000	3.0	LB	517	97	49	48	60
3.000	3.0	LB	518	85	41	40	317
3.000	3.0	LB	519	76	33	32	340
3.000	3.0	LB	520	90	44	43	244
3.000	3.0	LB	521	80	37	36	256
3.000	3.0	LB	522	76	33	32	161
3.000	3.0	LB	523	84	41	40	309

Table B-7. Timing Results for ITM-PHIL with R_{WYE} (Inverter 2): 8 kW, Qf=1

P (kW)	Q_f	Type	Capture	$t_{AID,V\ ac}$ (ms)	$t_{AID,Iac}$ (ms)	$t_{AID,Idc}$ (ms)	Angle (deg)
8.000	1.0	PHIL	562	57	42	40	351
8.000	1.0	PHIL	563	41	32	30	352
8.000	1.0	PHIL	564	109	94	86	352
8.000	1.0	PHIL	565	57	41	39	352
8.000	1.0	PHIL	566	51	42	40	352
8.000	1.0	PHIL	567	58	42	40	352
8.000	1.0	PHIL	568	49	38	37	351
8.000	1.0	PHIL	569	55	40	38	351
8.000	1.0	PHIL	570	56	38	37	351
8.000	1.0	PHIL	571	56	40	38	352

Table B-8. Timing Results for ITM-PHIL with R_{WYE} (Inverter 2): 8 kW, Qf=4

P (kW)	Q_f	Type	Capture	$t_{AID,V\ ac}$ (ms)	$t_{AID,Iac}$ (ms)	$t_{AID,Idc}$ (ms)	Angle (deg)
8.000	4.0	PHIL	573	116	84	90	352
8.000	4.0	PHIL	574	163	127	101	352
8.000	4.0	PHIL	575	152	117	92	351
8.000	4.0	PHIL	576	144	83	93	351
8.000	4.0	PHIL	577	142	84	90	352
8.000	4.0	PHIL	578	144	84	92	352
8.000	4.0	PHIL	579	187	126	92	352
8.000	4.0	PHIL	580	152	93	96	352
8.000	4.0	PHIL	581	178	118	92	352
8.000	4.0	PHIL	582	143	83	90	352

Table B-9. Timing Results for ITM-PHIL with R_{WYE} (Inverter 2): 3 kW, Qf=3

P (kW)	Q_f	Type	Capture	$t_{AID,V\ ac}$ (ms)	$t_{AID,Iac}$ (ms)	$t_{AID,Idc}$ (ms)	Angle (deg)
3.000	3.0	PHIL	587	111	74	68	351
3.000	3.0	PHIL	588	116	74	73	352
3.000	3.0	PHIL	589	112	74	71	351
3.000	3.0	PHIL	590	102	69	67	352
3.000	3.0	PHIL	591	120	78	91	352
3.000	3.0	PHIL	592	114	65	65	351
3.000	3.0	PHIL	593	114	65	63	352
3.000	3.0	PHIL	594	106	65	63	352
3.000	3.0	PHIL	595	112	69	82	351
3.000	3.0	PHIL	596	100	68	67	352

B.2 Tests with Inverter 3

Tables B-10 through B-19 provide the timing results for all recorded unintentional islanding experiments while using Inverter 3 in PHIL simulation setups.

Table B-10. RLC Load Bank with P_{PV} = 12 kW (Inverter 3)

P (Kw)	Q_f	PHIL Type	Mismatch %-var	IM (kVA)	Const.-P (kW)	Capture	$t_{AID,Idc}$ (ms)	Stability
12	3.0	ITM	0	-	-	662	940	stable
12	3.0	ITM	0	-	-	663	1,093	stable
12	3.0	ITM	0	-	-	734	1,120	stable
12	3.0	ITM	0	-	-	735	955	stable
12	3.0	ITM	0	-	-	736	937	stable
12	2.0	ITM	0	-	-	666	455	stable
12	2.0	ITM	0	-	-	667	950	stable
12	2.0	ITM	0	-	-	668	435	stable
12	2.0	ITM	0	-	-	732	636	stable
12	2.0	ITM	0	-	-	733	644	stable

Table B-11. RLC Load Bank with P_{PV} = 30 kW (Inverter 3)

P (kW)	Q_f	PHIL Type	Mismatch %-var	IM (kVA)	Const.-P (kW)	Capture	$t_{AID,Idc}$ (ms)	Stability
30	3.0	ITM	0	-	-	639	910	stable
30	3.0	ITM	0	-	-	640	838	stable
30	3.0	ITM	0	-	-	641	610	stable
30	3.0	ITM	0	-	-	642	1,059	stable
30	3.0	ITM	0	-	-	643	2,089	stable
30	3.0	ITM	0	-	-	644	1,299	stable
30	2.0	ITM	0	-	-	646	1,035	marg.
30	2.0	DIM	0	-	-	727	2,49	stable
30	2.0	DIM	0	-	-	728	240	stable
30	2.0	DIM	0	-	-	720	1,002	stable
30	2.0	DIM	0	-	-	721	533	stable
30	2.0	DIM	0	-	-	722	561	stable
30	2.0	DIM	0	-	-	723	1,358	stable
30	2.0	DIM	0	-	-	724	546	stable
30	1.5	DIM	0	-	-	685	252	stable
30	1.5	DIM	0	-	-	686	209	stable
30	1.5	DIM	0	-	-	687	301	stable

Table B-12. RLC Load Bank with P_{PV} = 54 kW (Inverter 3)

P (kW)	Q_f	PHIL Type	Mismatch %-var	IM (kVA)	Const.-P (kW)	Capture	$t_{AID,Idc}$ (ms)	Stability
54.000	3.0	ITM	0	-	-	655	1,969	stable
54.000	3.0	ITM	0	-	-	656	935	stable
54.000	3.0	ITM	0	-	-	657	1,870	stable
54.000	3.0	ITM	0	-	-	659	1,713	stable
54.000	3.0	ITM	0	-	-	715	758	stable
54.000	2.0	ITM	0	-	-	671	1,707	stable
54.000	2.0	ITM	0	-	-	672	1,650	stable
54.000	2.0	ITM	0	-	-	673	596	stable
54.000	2.0	ITM	0	-	-	713	964	stable
54.000	2.0	ITM	0	-	-	714	1,399	stable
54.000	1.5	ITM	0	-	-	676	1,022	stable
54.000	1.5	ITM	0	-	-	677	585	stable
54.000	1.5	ITM	0	-	-	678	474	stable
54.000	1.5	ITM	0	-	-	711	530	stable
54.000	1.5	ITM	0	-	-	712	955	stable
54.000	1.5	DIM	0	-	-	705	472	stable
54.000	1.5	DIM	0	-	-	706	566	stable
54.000	1.5	DIM	0	-	-	707	1,159	stable
54.000	1.5	DIM	0	-	-	708	703	stable
54.000	1.5	DIM	0	-	-	709	549	stable
54.000	1.0	DIM	0	-	-	690	1,229	stable
54.000	1.0	DIM	0	-	-	691	499	stable
54.000	1.0	DIM	0	-	-	692	550	stable
54.000	1.0	DIM	0	-	-	702	572	stable
54.000	1.0	DIM	0	-	-	703	629	stable
54.000	2.0	ITM	5	-	-	738	175	stable
54.000	2.0	ITM	5	-	-	739	173	stable
54.000	2.0	ITM	5	-	-	740	172	stable
54.000	2.0	ITM	2	-	-	741	957	stable
54.000	2.0	ITM	2	-	-	742	610	stable
54.000	2.0	ITM	2	-	-	743	1,545	stable

Table B-13. RLC Load Bank with P_{PV} = 46 kW (Inverter 3)

P (kW)	Q_f	PHIL Type	Mismatch %-var	IM (kVA)	Const.-P (kW)	Capture	$t_{AID,Idc}$ (ms)	Stability
46.000	2.0	ITM	0	-	-	771	1,221	stable
46.000	2.0	ITM	0	-	-	772	1,285	stable
46.000	2.0	ITM	0	-	-	773	884	stable
46.000	2.0	ITM	0	-	-	774	1,210	stable
46.000	2.0	ITM	0	-	-	775	621	stable

Table B-14. Induction Motor, 54-kW load, 60 kVA with P_{PV} = 54 kW (Inverter 3)

P (kW)	Q_f	PHIL Type	Mismatch %-var	IM (kVA)	Const.-P (kW)	Capture	$t_{AID,Idc}$ (ms)	Stability
54.000	2.0	ITM	-	60	-	749	2,240	stable
54.000	2.0	ITM	-	60	-	750	1,522	stable
54.000	2.0	ITM	-	60	-	751	552	stable
54.000	2.0	ITM	-	60	-	752	1,121	stable
54.000	2.0	ITM	-	60	-	753	2,240	stable
54.000	2.0	ITM	-	60	-	754	1,608	stable
54.000	2.0	ITM	-	60	-	755	2,238	stable
54.000	2.0	ITM	-	60	-	756	2,239	stable
54.000	2.0	ITM	-	60	-	757	1,665	stable
54.000	2.0	ITM	-	60	-	758	2,244	stable
54.000	1.0	DIM	-	60	-	762	581	stable

Table B-15. Inverter with Volt-var Control and Scaled Induction Motor, 54-kW Load, 221 kVA with P_{PV} = 54 kW (Inverter 3)

P (kW)	Q_f	PHIL Type	Mismatch %-var	IM (kVA)	Const.-P (kW)	Capture	$t_{AID,Idc}$ (ms)	Stability
54.000	2.0	ITM	-	221	-	836	2,214	stable
54.000	2.0	ITM	-	221	-	837	5,014	stable
54.000	2.0	ITM	-	221	-	838	5,014	stable
54.000	2.0	ITM	-	221	-	839	5,014	stable
54.000	2.0	ITM	-	221	-	840	5,014	stable

Table B-16. RLC Load Bank and PQ-Injection Model, P_{PV} = 54 kW (Inverter 3)

P (kW)	Q_f	PHIL Type	Mismatch %-var	IM (kVA)	Const.-P (kW)	Capture	$t_{AID,Idc}$ (ms)	Stability
54.000	2.0	ITM	-	-	54	784	564	stable
54.000	2.0	ITM	-	-	54	785	664	stable
54.000	2.0	ITM	-	-	54	786	610	stable
54.000	2.0	ITM	-	-	54	787	712	stable
54.000	2.0	ITM	-	-	54	788	517	stable
54.000	2.0	ITM	-	-	216	791	2,229	stable
54.000	2.0	ITM	-	-	216	792	4,858	stable
54.000	2.0	ITM	-	-	216	793	5,026	stable
54.000	2.0	ITM	-	-	216	794	5,027	stable
54.000	2.0	ITM	-	-	216	795	5,030	stable
54.000	2.0	ITM	-	-	108	796	1,548	stable
54.000	2.0	ITM	-	-	108	797	758	stable
54.000	2.0	ITM	-	-	108	798	552	stable
54.000	2.0	ITM	-	-	108	799	1,037	stable
54.000	2.0	ITM	-	-	108	800	536	stable
54.000	2.0	ITM	-	-	108	801	1,144	stable
54.000	2.0	ITM	-	-	162	802	1,301	stable
54.000	2.0	ITM	-	-	162	803	1,653	stable
54.000	2.0	ITM	-	-	162	804	1,003	stable
54.000	2.0	ITM	-	-	162	805	955	stable
54.000	2.0	ITM	-	-	162	806	503	stable

Table B-17. RLC Load Bank and PQ-injection + Volt-var Model (50 kvar), P_{PV} = 54 kW (Inverter 3)

P (kW)	Q_f	PHIL Type	Mismatch %-var	IM (kVA)	Const.-P (kW)	Capture	$t_{AID,Idc}$ (ms)	Stability
54.000	2.0	ITM	-	-	162	809	2,340	stable
54.000	2.0	ITM	-	-	162	810	793	stable
54.000	2.0	ITM	-	-	162	811	811	stable
54.000	2.0	ITM	-	-	162	812	3,139	stable
54.000	2.0	ITM	-	-	162	813	1,964	stable

Table B-18. RLC Load Bank and PQ-Injection + Volt-var (25 kvar, 100 kvar/s), P_{PV} = 54 kW (Inverter 3)

P (kW)	Q_f	PHIL Type	Mismatch %-var	IM (kVA)	Const.-P (kW)	Capture	$t_{AID,Idc}$ (ms)	Stability
54.000	2.0	ITM	-	-	162	820	536	stable
54.000	2.0	ITM	-	-	162	821	3,172	stable
54.000	2.0	ITM	-	-	162	822	591	stable
54.000	2.0	ITM	-	-	162	823	4,228	stable
54.000	2.0	ITM	-	-	162	824	1,625	stable

Table B-19. RLC Load Bank, Inverter in Volt-var Mode, P_{PV} = 54 kW (Inverter 3)

P (kW)	Q_f	PHIL Type	Mismatch %-var	IM (kVA)	Const.-P (kW)	Capture	$t_{AID,Idc}$ (ms)	Stability
54.000	2.0	ITM	-	-	162	829	1,163	stable
54.000	2.0	ITM	-	-	162	830	1,454	stable
54.000	2.0	ITM	-	-	162	831	519	stable
54.000	2.0	ITM	-	-	162	832	714	stable
54.000	2.0	ITM	-	-	162	833	1,590	stable