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*Semiconductor Measurement Technology:*

# Evolution of Silicon Materials Characterization: Lessons Learned for Improved Manufacturing

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W. Murray Bullis

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<sup>1</sup>At Boulder, CO 80303.

<sup>2</sup>Some elements at Boulder, CO 80303.

# **Evolution of Silicon Materials Characterization: Lessons Learned for Improved Manufacturing**

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*Semiconductor Measurement Technology:*  
**EVOLUTION OF SILICON MATERIALS CHARACTERIZATION:  
LESSONS LEARNED FOR IMPROVED MANUFACTURING**

Based on a paper presented at the 1992 U.S. Workshop on the Physics and Chemistry of Mercury-Cadmium-Telluride,  
Danvers, Mass., October 16, 1992  
with additional supplementary information

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**ABSTRACT**

The growth of the silicon device and integrated circuit industry has been closely coupled with the development of materials characterization technology. This paper traces this development from the beginning, when the industry was young and each manufacturer had to grow its own materials, develop its processes, assemble its measurement systems from component instruments, and fabricate its processing equipment, to the present, when a complex infrastructure supports the industry. It also describes examples of both successful and unsuccessful developments in connection with other electronic materials. The critical factors in the widespread standardization and application of silicon characterization technology are: shared results and common goals among industry, government, and universities; an efficient mechanism for development of consensus standards with adequate expertise; standardization of parameters needed for orderly flow of materials in manufacturing together with standardized terminology, test methods, and formats to support detailed purchase specifications; and refinement of the measurement technology as the industry develops and becomes more sophisticated. Finally, a good methodology for process diagnosis and control is an essential feature for applying test procedures to the manufacturing environment. The successes and failures which occurred during the course of developing metrology tools for silicon can provide some insights into similar developments for the special needs of other electronic materials. In addition, many of the test procedures and standards developed for silicon materials and supporting technologies can be applied directly.

Key words: ASTM; characterization techniques; materials characterization; NIST; SEMI; silicon; standards; wafer dimensions

**INTRODUCTION**

The growth of the silicon device and integrated circuit industry has from its inception been closely coupled with the development of characterization technology for silicon materials. We have to recognize that silicon enjoys a major advantage over compound semiconductors in that the single element matrix provides considerable simplification in both preparation and analysis. The material is an excellent vehicle for probing the inner workings of the solid state as well as being abundant, relatively inexpensive, and the backbone of a major industry. Nevertheless, the lessons learned during the long evolution of

metrology for the silicon industry may help in defining efficient paths for metrology development in connection with other, more specialized electronic materials.

However, there is also a nontechnical factor which must be taken into account when trying to apply the experience gained in silicon to other materials. Relative to the various electronic materials, electronic-grade silicon enjoys a very large market, and thus the industry is able to support a substantial infrastructure. Nevertheless, the size of the electronic-grade silicon market is tiny when considered in terms of markets for commodity materials such as steel, aluminum, chemicals, and the like. In fact, much more silicon — of course, of metallurgical grade — is used in the aluminum and steel industries than is used for semiconductor devices and integrated circuits.

The requirements for purity, uniformity, and dimensional control of electronic-grade silicon are severe and have from the beginning taxed the metrological and contamination control capabilities of supporting industries. Because of the relatively small volumes involved, it has proved to be quite difficult to encourage these supporting industries to develop their capabilities to the degree necessary for advancing silicon technology. Materials with even smaller markets would be expected to encounter similar difficulties, but may be able to utilize much of the infrastructure established for the silicon industry.

This paper is not intended to be a complete history of the development of silicon material metrology and standards. Such a history would require a rather large volume to include all the myriad of significant contributions to the field. Rather, it focuses on issues which show the impact of metrology development and standardization efforts on the growth of the silicon industry. We first review the early history of silicon materials characterization. At this time, the industrial base was highly customized and each major manufacturer of devices made its own equipment and grew its own materials. Then we consider the beginnings of test procedure standardization about 30 years ago. This led to standardization of the dimensional properties of silicon wafers in the mid-seventies which enabled the development of the merchant equipment industry which now supports the silicon device industry.

As time went on, the precision and sensitivity requirements of various test procedures increased and new characteristics had to be determined. This trend continues today as metrology development evolves to meet the requirements of advanced sub-micrometer ultra-large scale integrated (ULSI) circuit technology; however, the environment for these developments has changed markedly from that which existed in the early days of the industry. Finally, we identify the critical factors in the widespread application and standardization of silicon characterization technology and draw some conclusions regarding extensions to the development of metrology for other materials.

## EARLY DEVELOPMENTS

In the decade following the invention of the transistor in the late forties, there was a period of intense materials characterization which laid the foundations for our current knowledge of the electronic, optical, and mechanical properties of silicon. In particular, the group at the Bell Telephone Laboratories published prolifically during the early fifties — journal articles, technical papers, and books — on all aspects of semiconductor technology from basic theory to practical application, from measurement techniques to process technology. In addition, a variety of groups from other major companies, universities, and government laboratories made important contributions to this effort. During this period, the fundamental aspects of semiconductor behavior were established firmly, and basic metrology tools were demonstrated. It was a very exciting time as new ideas and theories were subjected to experimental scrutiny.



The great advances made during this period unfortunately led to a degree of complacency regarding the completeness of the state of knowledge of silicon technology by 1960. Nevertheless, the importance of the widespread dissemination of the basic technologies cannot be overemphasized. The flow of information throughout the young industry fueled rapid advances in both technology and applications and set the stage for future development and growth.

The concept of doping (which had been first articulated in connection with semimetals in the U.K. during the thirties) and the one-to-one correspondence between the dopant atom density and the free carrier density were experimentally demonstrated. Minority carrier transport properties and *p-n* junction characteristics were modeled and controlled. Photoconductivity and optical absorption characteristics were demonstrated. Surface states were analyzed and basic models established. Both modified Czochralski and floating zone techniques were developed for growing "large" single crystals, and the process for growing dislocation-free silicon crystals (now routinely expected when silicon is mentioned) was developed and introduced into production. Chemical vapor deposition techniques for producing silicon films on silicon and other substrates were introduced. Theoretical and experimental band structure investigations led to an understanding of transport phenomena in both silicon and germanium.

On the metrology side, the four-point probe was rediscovered and applied to the measurement of resistivity of semiconductor crystals and slices. Extensive application of the Hall effect allowed determination of carrier densities and mobilities over a wide temperature range leading to basic knowledge about impurity energy levels in the forbidden band gap. Photoconductivity decay was introduced as a direct measure of minority carrier recombination lifetime. The infrared absorption band at a wavelength of about 9  $\mu\text{m}$  was used to determine the oxygen content of silicon crystals. Both x-ray diffraction and optical techniques were used for orienting wafer surfaces. The thermoelectric effect and point-contact rectification were applied to the determination of conductivity type. Various preferential chemical etchants were developed to expose dislocations and crystal defects which intersected wafer surfaces.

During the initial phase of these developments, interest was focused on germanium materials and devices. Because of its relatively low melting point, this material was easy to prepare and process. However, because of its narrow band gap, devices could be operated only at room temperature; even the heat generated in a car parked in the sun was sufficient to cause germanium transistors to become inoperative. Hence, in the mid-fifties, the major emphasis shifted from germanium devices to silicon devices. An elemental semiconductor like germanium, silicon was much more abundant. In fact, silicon is the second most abundant element on Earth. Not only did silicon permit the operation of devices at higher temperatures because of its wider band gap and good thermal conduction characteristics, but also it had the inherent strength to withstand handling during manufacture and use. In addition, it was possible to passivate the surface with thermal oxide. Although this characteristic was soon to have far reaching implications with regard to process standardization and the development of integrated circuits, the device industry at this time remained in its custom mode with each major manufacturer designing and building its own equipment, growing its own materials, and developing its own process technology. Device technologies evolved rapidly from grown junction to alloy junction to diffused junction, from mesa to planar. Standardization was yet to come.

## BEGINNINGS OF STANDARDIZATION

By the early sixties, the two basic concepts which have fueled the growth of the microelectronics age were established. The viability and advantages of planar technology for device fabrication and the

feasibility of placing multiple components on a single chip to form an integrated circuit were both demonstrated. But all was not completely rosy. A fledgling merchant materials industry was growing up and attempting to supply silicon wafers to device manufacturers. Measurement conditions and procedures were imprecisely defined and there were many disagreements over material properties as measured by supplier and user. This is a classic example of the fact that the demands on definitions and metrology made by the manufacturing environment are much more severe than those made by the research environment which seeks to demonstrate a scientific principle rather than to replicate nominally identical products [1].

These disagreements at the supplier-user interface demonstrated a need to standardize the applicable measurement techniques. This need was met through the American Society for Testing and Materials (ASTM) Committee F-1 on Electronics. In 1955, this Committee had evolved as the first "end-use" committee in ASTM from a subcommittee on non-ferrous metals for vacuum tube application. Its scope covered development of standards for materials for all types of electron devices. By 1960, through the visionary leadership of its early chairmen, Sid Standing of Raytheon and Frank Biondi of Bell Telephone Laboratories, the Committee had made a rapid transition to cover semiconductors [2].

### GROWTH OF ASTM COMMITTEE F-1

Over the next decade, standardized methods were developed for the basic parameters by which silicon is specified. These included all the techniques reported during the fifties: the four-point probe method for measuring resistivity and radial resistivity variation; the photoconductivity decay method for minority carrier recombination lifetime (also developed by the Institute of Electrical and Electronic Engineers - IEEE); x-ray and optical methods for crystallographic orientation; chemical etching to reveal dislocations, stacking faults, and other crystallographic defects; various methods for conductivity type determination; Hall effect for carrier density and mobility; and infrared methods for the determination of oxygen content and epitaxial layer thickness.

These methods were the result of intensive efforts at major industrial laboratories, particularly Bell Labs, IBM, RCA, and GE, and at the National Bureau of Standards.<sup>1</sup> Not only did these organizations provide the research necessary to develop the methods to a state suitable for use in production environments, but they also provided the leaders for the standardization activities. Without this intensive refinement of measurement methods during the sixties, the pace of development of metrology for the industry would not have been so rapid.

The successful development of test methodology for silicon materials was due in large part to the rigorous procedure by which consensus was reached and the efficacy of the method demonstrated [3] as outlined in the flow chart in Figure 1. Two blocks of this flow chart are emphasized. The first indicates the people required to carry out the activity; we will consider the effect of this factor later. The second identifies the interlaboratory evaluation of test methods. Despite the fact that this rigorous process was indeed time-consuming, the results afforded significant benefits to the participants. In particular, these cooperative experiments allowed participating organizations to determine their abilities to carry out important measurements and frequently highlighted difficulties in one location or another which could then be corrected using the new information derived from the experiment. One frequently heard

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<sup>1</sup> The National Bureau of Standards was renamed the National Institute of Standards and Technology (NIST) in 1988.

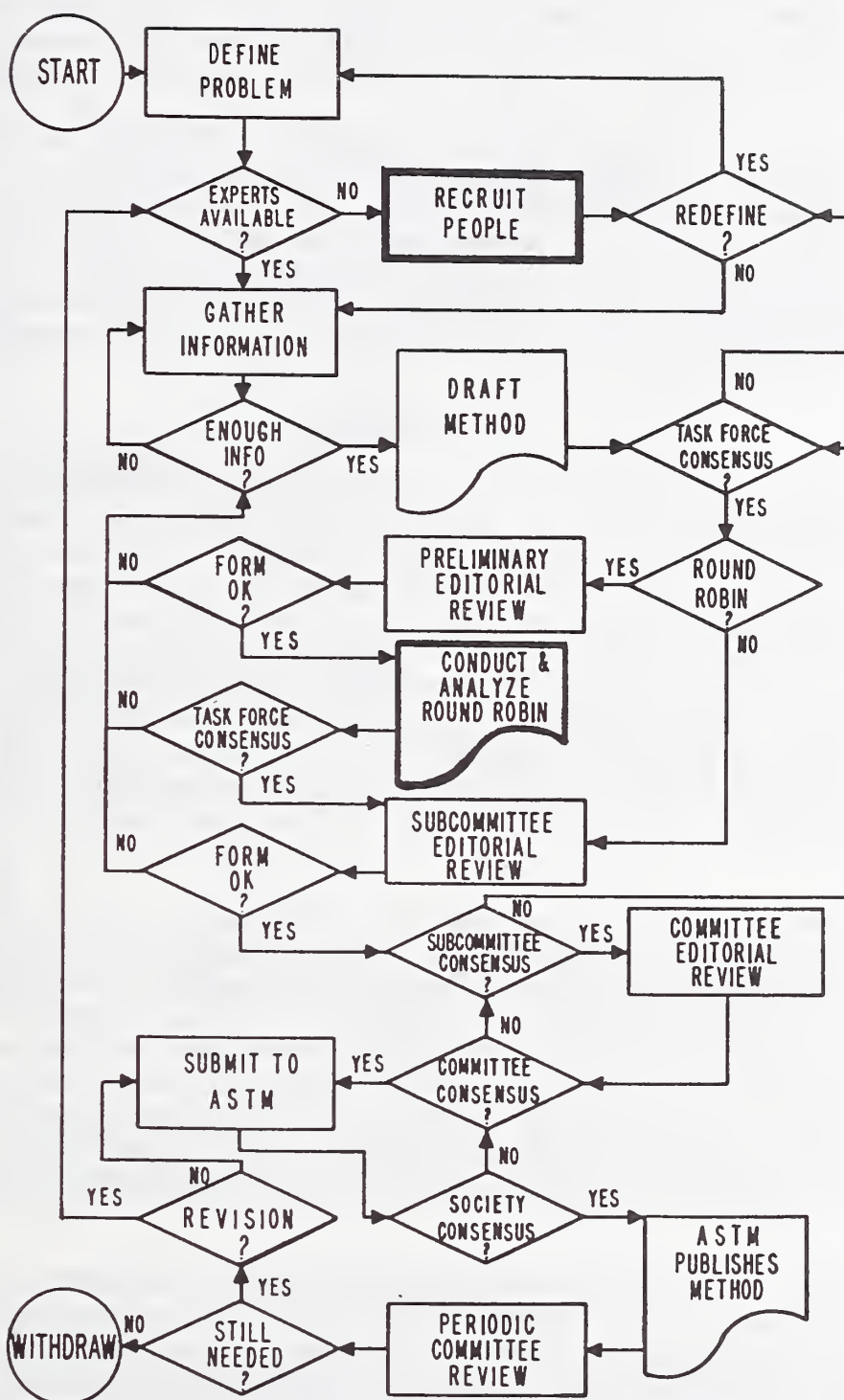


Figure 1. Flow chart showing creation of an ASTM standard test method. (From Ref. 3.)

complaint about this procedure is that it is unduly time-consuming. Experience over the years has indicated that if there is a real, well-understood need for the test method, the entire procedure from



conception to publication, including completion of preliminary testing, can be completed in less than 2 years. This is, however, not the norm; average development time is 3 to 5 years. Nevertheless, a more rapid and effective procedure has yet to be demonstrated. Efforts to speed up the process by short-circuiting important elements of the developmental process have frequently led to additional delays.

There was also intensive development of methods to control contamination levels in air, chemicals, and other fluids, and on surfaces. A subcommittee on this topic was organized at the time Committee F-1 was established. It conducted a series of landmark symposia which defined the industry requirements for contamination control and led to the development of nearly 20 standards. Many of these early ASTM Test Methods were incorporated into the initial Federal Standard on Clean Rooms [4]. This standard has evolved over the years and several updated editions have been published; it is now being further revised to accommodate the more rigorous contamination control requirements associated with ULSI technologies.

### SOME PROBLEMS

At the same time that the Committee was having considerable success with developing standards for silicon substrates and contamination control, it failed to duplicate these successes in several other areas. There were two notable examples of this. One instructive example of F-1 failure occurred in the area of trace analysis. It was broadly recognized that trace analysis was a critical aspect of semiconductor technology because the properties of the materials are controlled by minute amounts of foreign atoms — some of which are intentionally introduced and some of which are not. The Committee attempted to establish a group to refine chemical and physical methods so that they could achieve the sensitivities required. In this case, it proved impossible to attract analytical specialists to participate actively in a group with highly specialized and very demanding goals. Some related activities were subsequently conducted in other ASTM committees, notably Committee E-42 on Surface Analysis, but standardization of these analytical methods in the regimes appropriate to silicon material and device technologies has lagged to this day.

The second example occurred in the area of standards for testing phosphor materials used for cameras and displays. Although there was general agreement that such standards would be beneficial to the industry, the effort to develop them failed because common ground could not be established. The procedures for preparing the phosphors were considered to be highly proprietary; since different procedures required different properties in the starting materials, even discussing starting material properties was considered to be off-limits because they might reveal some aspect of the subsequent processing. Further, there was the feeling in some quarters that the properties of the starting materials were not so very important after all because of the changes made during processing. Thus, no useful dialogue between suppliers and users of the materials could be established and the effort did not achieve any results.

Since the mid-sixties, we have learned a great deal about establishing common ground for standards, and it is possible that if the effort had been conducted with the benefit of this knowledge, we might have made more progress. Among the issues which can be discussed at the outset are definitions of commonly used terms. Although good definitions reduce the ability of suppliers to play "specsmanship" games, there is usually enough interest in commonality in this area to get some useful dialogue begun. The second area is in test methodology for very basic properties such as composition or geometry. Once rapport is established in these areas, it is sometimes possible to extend the effort to more controversial areas. This approach is now being used with modest success in connection with testing for magnetic disk technologies.



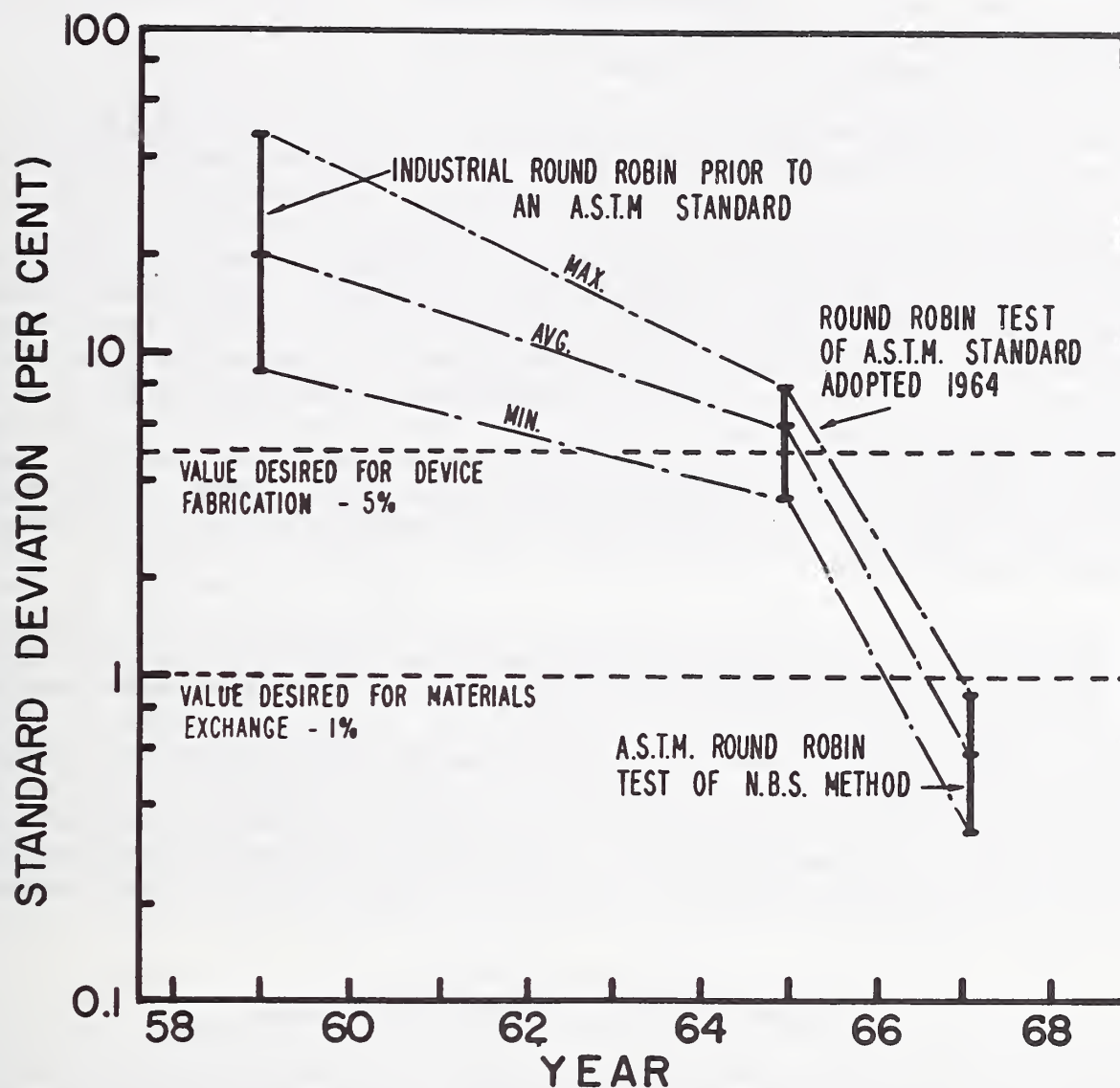


Figure 2. History of the interlaboratory precision of the measurement of silicon resistivity in the range 0.01 to 100  $\Omega \cdot \text{cm}$  by the four-point probe method. (The vertical bars represent the range in sample standard deviation obtained in the interlaboratory (round robin) tests.) (From Ref. 5.)

### U.S. GOVERNMENT ACTIVITIES

Early in the history of ASTM Committee F-1, a relationship was established with the National Bureau of Standards. Around 1960, the Bureau's Tube Laboratory began a shift toward semiconductor technology. This grew in concert with the growth of ASTM Committee F-1, and in the late sixties, the semiconductor effort was formalized into a major program under the direction of Charles Marsden and Judson French. This program was largely supported by Defense Department, Energy Department, and NASA funds. One of the major accomplishments of the early phase of this program was a significant improvement in the precision of four-point probe resistivity measurements, as shown in Figure 2. This

effort is a classic example of measurement method development. It involved not only considerable refinement of the measurement conditions but also a great deal of industrial cooperation. The results were validated by interlaboratory testing in Committee F-1 [5].

During this same period, two highly significant developments occurred within the military and space agencies of the U.S. Government. First, Joe Brauer's group at Rome Air Development Center developed a revolutionary procedure for qualification of integrated circuits for military application. When it was first introduced in 1968, MIL-STD-883 was considered by many to be too difficult and unnecessary; many vendors sought and obtained waivers from its rigid testing procedures. Its most obvious limitation was that it continued the philosophy of "testing-in" rather than "building-in" quality. Nevertheless, the discipline imposed by the testing hierarchy, particularly when combined with efforts to trace causes of testing failures, provided a methodology which could be applied to process control and improvement. Although many in the United States failed to take advantage of this opportunity, it was not lost on the young, but rapidly developing, Japanese semiconductor industry. Within a few years following its introduction, the principles of MIL-STD-883 were being **strictly** applied to good advantage in Japan. Coupled with the principles of quality through statistical process control as espoused by Deming and others, MIL-STD-883 became a formidable weapon in the efforts of the Japanese to improve both quality and manufacturing efficiency.

The NASA approach was different from, but complementary to, the more traditional approach taken by the Air Force. In the late sixties, Dr. A.M. Halliday and his group at the Marshall Space Flight Center established a program known as the Line Certification Program, specifically directed toward integrated circuit fabrication. This program focussed on control of the incoming materials (such as silicon, chemicals, gases, and parts), the clean room environment, and fabrication processes (such as oxidation, patterning, ion implantation, diffusion, metallization, and passivation). Although far from perfect, this program, when applied, provided process control features similar in many ways to those found in the Deming approach. Significant improvements in both quality and manufacturing efficiency could be realized when the techniques of this program were applied, but frequently they were viewed as too costly and complex to be practical.

## STANDARDIZATION OF WAFER DIMENSIONS

In the early seventies, the industry was expanding rapidly and silicon material was in short supply. At this time, wafers were being manufactured with a great variety of geometrical characteristics to respond to the myriad of requirements of the various device lines. This required vast inventories of materials of similar, but not interchangeable, geometries.

Initial standardization efforts were undertaken on an *ad hoc* basis by silicon suppliers [6]. A limited number of values for wafer diameter, flat length, thickness, and thickness variation was proposed in order to reduce the proliferation of wafer sizes and improve manufacturing efficiency. It should be noted that although a system of flats on the periphery of the wafer was developed to differentiate wafer conductivity type and surface orientation, values of electrical and crystallographic properties, which cover a wide range and are generally specific to a particular device process were not included in the specifications. In fact, this concept, the standardization of geometrical properties while allowing flexibility in application-specific material characteristics, is a key element in the successful industrial application of the silicon metrology development and standardization activities.

## GROWTH OF SEMI STANDARDS

These wafer specifications were formalized by the Semiconductor Equipment and Materials Institute (SEMI)<sup>2</sup> in 1973 [7] and within a few years became generally accepted throughout the free world [8]. The SEMI specifications were not only successful in helping to alleviate the material supply crisis which had precipitated their development; they also had several other significant impacts.

First, they were instrumental in increasing industry awareness of the ASTM Test Methods which were continuing to be produced by Committee F-1. There was a general awareness that standardized test procedures were necessary to support the specifications. By the end of the seventies the Committee had developed test methods for the dimensional properties covered by the SEMI specifications as well as many of the other properties which had to be specified in individual purchase documents; all applicable test methods were referenced in the SEMI silicon wafer specifications.

Second, although the SEMI specifications were introduced at about the time the industry was shifting to 76.2-mm (3-in.) diameter wafers, they were extended periodically to cover larger diameter wafers and so facilitated the orderly production of 100-, 125-, and 150-mm wafers as the industry evolved. The concept of dimensional standardization became widely accepted and expected as the specifications for these larger diameters were introduced.

Third, the existence of standardized geometries for wafers made it possible to design and construct wafer handlers, transport systems, and processing equipment on an interchangeable basis. This, together with the almost universal adoption of the planar process for fabricating devices and circuits, allowed the establishment and orderly growth of a merchant semiconductor process equipment industry. No longer did each device manufacturer have to design and build its own processing equipment on a custom basis; it is now possible to obtain such equipment commercially. In fact, merchant equipment suppliers now provide a great deal of the process development activity in the industry, frequently in partnership with Semiconductor Manufacturing Technology (SEMATECH) or a major device house.

## INTERNATIONALIZATION

Fourth, the worldwide acceptance of the SEMI standards for silicon wafers accelerated the internationalization of the standardization efforts [9]. ASTM Committee F-1 had established informal liaison with Committee FNM A9 (now NMP 221) of the Deutsches Institut für Normung (DIN) in Germany in the late sixties. This cooperation grew and was formalized in 1976. During this period, technical differences between ASTM and DIN test methods for silicon characterization were virtually eliminated so that test methods generated by either organization are cited in and can be used in support of the SEMI silicon wafer specifications.

Late in the seventies, initial contacts were made with the Japan Electronic Industry Development Association (JEIDA) which was developing standard test methods for characterizing silicon wafers in Japan. These contacts developed into an active partnership in the early eighties. Although significant differences exist in geometrical characteristics of silicon wafers in Japan and in the United States, cooperative activities are continuing in an effort to reduce these differences.

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<sup>2</sup> The Semiconductor Equipment and Materials Institute was renamed the Semiconductor Equipment and Materials International in 1987 to reflect the global nature of the industry.



## OTHER DEVELOPMENTS

During this period, the NBS program on semiconductor measurement technology was expanded significantly with major funding from the Defense Advanced Research Projects Agency (ARPA) and the Defense Nuclear Agency (DNA). In-house work on wire bonding, microelectronic test structures, and linewidth measurements responded to a number of critical needs. Under the ARPA program, more than 20 contracts were awarded to industry, academic, and government laboratories over a six-year period to support the development of a wide range of innovative measurement techniques. Topics covered included development of micrometer-scale imaging for acoustic microscopy, detailed investigation of the Si-SiO<sub>2</sub> interface, study of the transfer of metal ions from solutions to wafer surfaces, surface quality tests for sapphire substrates, development of specialized microelectronic test structures, and determination of electron and hole mobilities in silicon as a function of dopant density and temperature. Some of these were immediately successful and were applied directly in the industry; others were somewhat ahead of their time and did not meet with wide acceptance [10]. Overall, however, this program provided a very useful boost to the development of measurement technology for state-of-the-art integrated circuit fabrication.

NBS also introduced Standard Reference Materials (SRMs<sup>®3</sup>) specifically for the semiconductor industry during the early seventies. The first of these was a set of two wafers certified for resistivity as measured by the standard four-point probe method [11]. Other resistivity SRMs were issued later in the decade. This program was expanded during the eighties to include SRMs for linewidth measurement on photomasks, spreading resistance calibration, and oxide film thickness. A key point is that, in most cases, the certified value is based on measurements made in accordance with a consensus procedure developed and tested by interlaboratory experiment in ASTM Committee F-1. Despite the fact that absolute standards for these measurements do not exist, and so the bias of the certified value cannot be estimated, these SRMs provide a common basis for calibration and control of test equipment in the industry and thus facilitate supplier-user exchange.

At the same time, ASTM Committee F-1 extended its activities into other areas. Building on the work in the NBS program, a number of ASTM specifications and test methods were developed for interconnection bonding wire and bond testing. Later the work on bonding broadened to include tape-automated bonding, a current major activity of the Committee. A second successful area of activity was in radiation hardness, also undertaken with the initial assistance of DNA and NBS. The cornerstone of this activity is cooperation and coordination with many other governmental and industrial groups concerned with device quality and radiation hardness assurance. The subcommittee has developed more than 30 standard test methods, practices, and guides and continues to produce several new and revised standards each year.

Groups addressing gallium arsenide, gadolinium gallium garnet, and passive microwave devices were also established in Committee F-1. Of these, only the gallium arsenide group now remains active. However,

this group has developed only a few standards. There are two reasons for this. First, many of the relevant test procedures, especially those for dimensional properties, are the same for gallium arsenide

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<sup>3</sup> The term "SRM" is a Federally registered trademark of the National Institute of Standards and Technology and the U.S. Government.



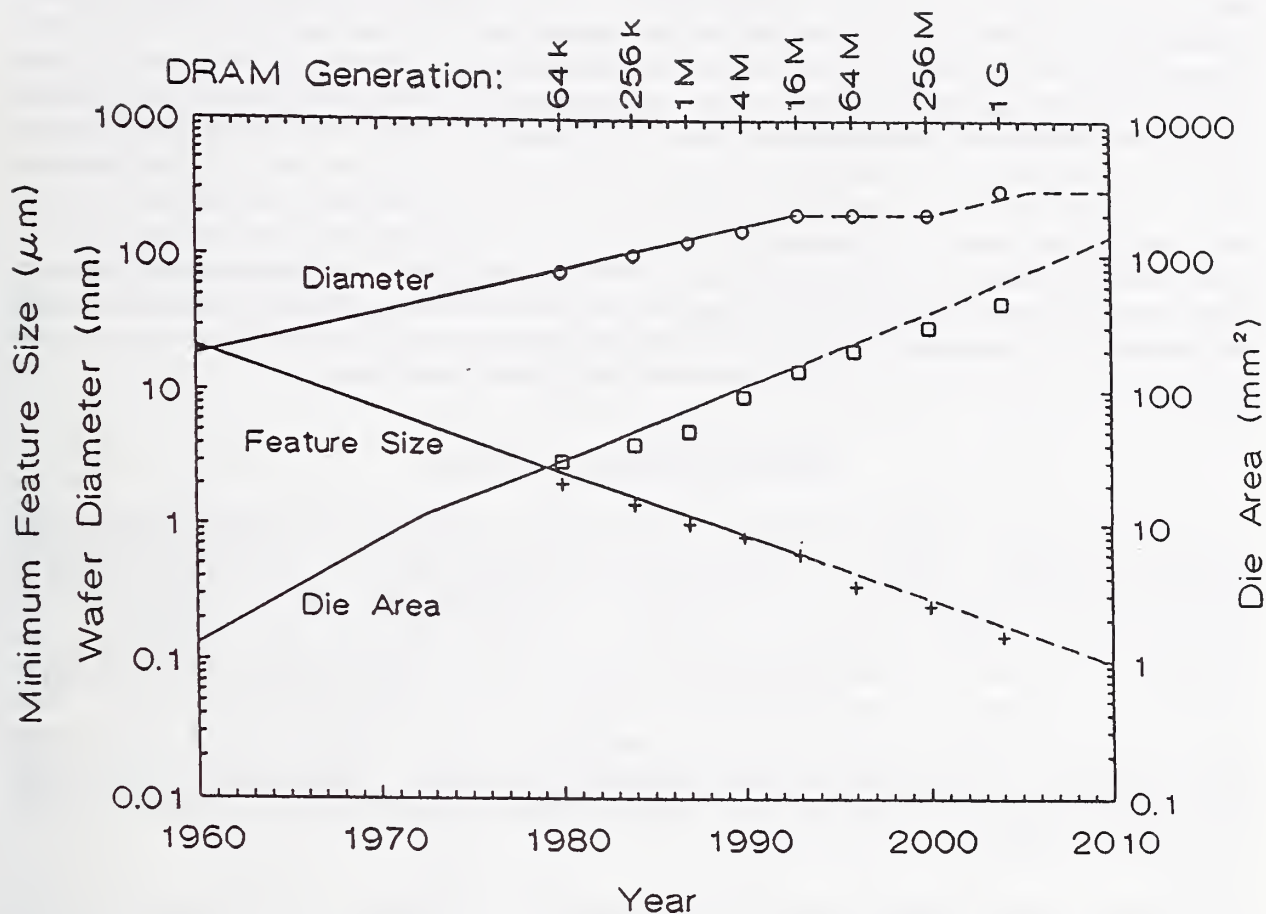


Figure 3. Trends in minimum feature size, die area, and wafer diameter. (Data shown are from Ref. 12.)

as for silicon; consequently they did not have to be reinvented. Second, the dominant commercial activity in III-V compound semiconductors is in Japan rather than in the United States; thus the U.S. group is hampered by sub-critical size.

### A MOVING TARGET

Throughout the eighties, silicon technology continued to advance. Dynamic random access memory (DRAM) density quadrupled roughly every 3.2 years. To support this increase in circuit density, not only were new design and process technologies developed but also the reductions in feature sizes and increases of die area and wafer diameter continued to progress along their historical exponential trends: minimum feature size was halved every 6.4 years, die area doubled every 5.4 years, and wafer diameter doubled every 9.5 years. These trends, illustrated in Figure 3 together with historical data and future projections [12], placed more severe requirements on silicon materials, particularly in regard to control of bulk defect properties, surface particulate and metal contamination, and wafer flatness. Precision and sensitivity requirements of traditional measurements steadily increased, and new characteristics had to be measured.

Early in the eighties, U.S. device manufacturers began to understand that meaningful two-way communication and cooperation with their silicon material and equipment suppliers is essential for efficient production of quality parts. Whereas once the material, equipment, and device operations had all been part of the same organization, the rise of the merchant material and equipment industries tended to build barriers between the various functions. It is instructive to note that this lesson was learned earlier in Japan than in the United States, contributing to the earlier Japanese success in building high-quality semiconductor devices and circuits. Major U.S. device companies began cooperative programs with their suppliers, which were extremely effective for their participants in advancing the performance, quality, and consistency of silicon materials. Also during this period, the Semiconductor Research Corporation (SRC) and later SEMATECH fostered cooperative interactions between various portions of the industry on a somewhat wider scale. SRC focused on university research programs while SEMATECH emphasized unit processes and process equipment development.

### SILICON STANDARDS ACTIVITIES

To respond to the new demands being made of silicon wafers, both SEMI and ASTM expanded their standards development activities. SEMI developed specifications for silicon and silicon-on-sapphire epitaxial wafers, solar-grade silicon, silicon test wafers, and polycrystalline silicon. The specifications for many of the dimensional tolerances on silicon wafers were tightened, and a specification was developed for 200-mm wafers with a notch fiducial instead of a flat. Specifications for gallium arsenide wafers for both optoelectronic and integrated circuit applications were developed and published. These followed the same pattern as the silicon wafer specifications, with standard values for dimensional parameters and flexibility for electrical and crystallographic parameters. It is also instructive to note that the standard test procedures cited in support of these gallium arsenide specifications were all initially developed for silicon.

New ways of measuring many parameters were introduced by a number of relatively small instrument houses. In general, these involved computer-controlled instruments, frequently with positioning and scanning capabilities. Although the repeatability of such instruments was usually better than that of the previously available techniques, comparisons between measurements made with different instruments were often difficult because of differences in their construction or algorithms, not all of which are readily apparent to the user. Thus the instrument behaves as a sealed "black box" with stipulated inputs and automatic outputs. Nevertheless, standardization of test methods has continued into this environment, even though frequently the instruments are not sufficiently defined. There are three possible choices for standardization under such conditions:

1. Generate a referee method based on a complete description of the instrument and the associated procedure which is usually based on manual data acquisition and analysis. Use this referee method to generate calibration and verification standards for use with the black-box technique.
2. Describe the procedure in terms of the data to be collected and the mathematical relationships to be used for analysis, allowing variety in the actual implementation of the algorithms. If desired, instrument verification procedures may be included to evaluate the suitability of the instrument, and standard sample data sets can be provided to test the software routines.
3. Describe only a skeleton of the method, relying on the manufacturer's instructions for the actual procedure. Such a method provides little real information; however, it is also possible to include instrument verification routines and standard sample data sets as in case 2.



All of these procedures have been employed in various silicon related test methods standardized by ASTM. Case 2 is generally the preferred one because it provides the greatest amount of information to the user and facilitates valid comparisons between competing systems while allowing the instrument designer maximum flexibility in implementing the method. Nevertheless, there are circumstances in which one of the other cases may be all that can be agreed upon. Sometimes, agreement cannot be reached at all.

An example of a case in which it has not yet been possible to determine an acceptable standardization procedure for a test based on black-box instrumentation can be found in the area of wafer inspection. Inspection of silicon wafers for particles and other surface contamination has long been a key quality control tool. For many years, this has been accomplished by means of visual inspection under controlled illumination in a darkened environment. As critical particle sizes and counts became smaller, automated particle detection systems were rapidly introduced into research and production. However, development of standards for these systems proved to be an elusive task because these instruments are essentially computer-controlled black boxes, the detailed workings of which are generally unknown to the user. Differences in design from one system to another result in differences in results obtained. Further, the physics of the process is both extremely complex and incompletely understood. Although test artifacts based on latex spheres or lithographed patterns are widely used, the relationship between these surrogates and “real” particles is also not well established. Consequently, there is no “right” way to perform the determination, and so there is no technical basis for a “standard” procedure. The silicon standards community is still wrestling with this issue, both in SEMI and ASTM.

Improperly executed and continuously revised standards can confuse as well as clarify. Early in the eighties, there was renewed interest in more precise control of the oxygen content in silicon wafers because of the influence of the oxygen on both the gettering capabilities and mechanical strength. Up to this point, there had been considerable confusion in both the industry and research communities because of the adoption of conflicting values for the calibration factor relating the 9- $\mu\text{m}$  absorption coefficient to the oxygen concentration. ASTM had adopted three different values between 1964 and 1980; the last of these was the one which had been adopted by DIN. Still a fourth value was adopted by JEIDA in the early eighties. The largest of these four factors was nearly twice the smallest. With the resurgence of interest in this topic, many different individual research studies were carried out; these led to additional values for this factor which tended to converge in the neighborhood of 6 ppma/cm<sup>-1</sup>. These results are summarized in Figure 4. To resolve the issue, an extensive international experiment was conducted jointly by ASTM, JEIDA, SEMI, DIN, and Academia Sinica, with the cooperation and participation of numerous government and industrial organizations around the world [13]. This experiment brought harmony to the community since all major standards bodies have adopted its result. Certified reference materials for oxygen determinations referenced to this calibration factor are available from both JEIDA in Japan and the Community Bureau of Reference (BCR) in Europe. Soon, they will also be available in the United States from NIST. Although the final result appears to be the most nearly correct, the circuitous path which led to it was most undesirable. Some revision of standard test methods and specifications is essential to maintain technical currency and to strive for the best possible solutions, but too frequent change is very unsettling to the user community. Thus timing is seen to be a critical factor in issuance of standards. If they are issued too early, the chances of selecting incorrect values and inappropriate procedures are greater, but if they are delayed too long, there are too many different choices already available in the marketplace and standardization becomes difficult. Even if standardization occurs eventually in the latter case, the long delay may cause loss of some of the economic benefits.

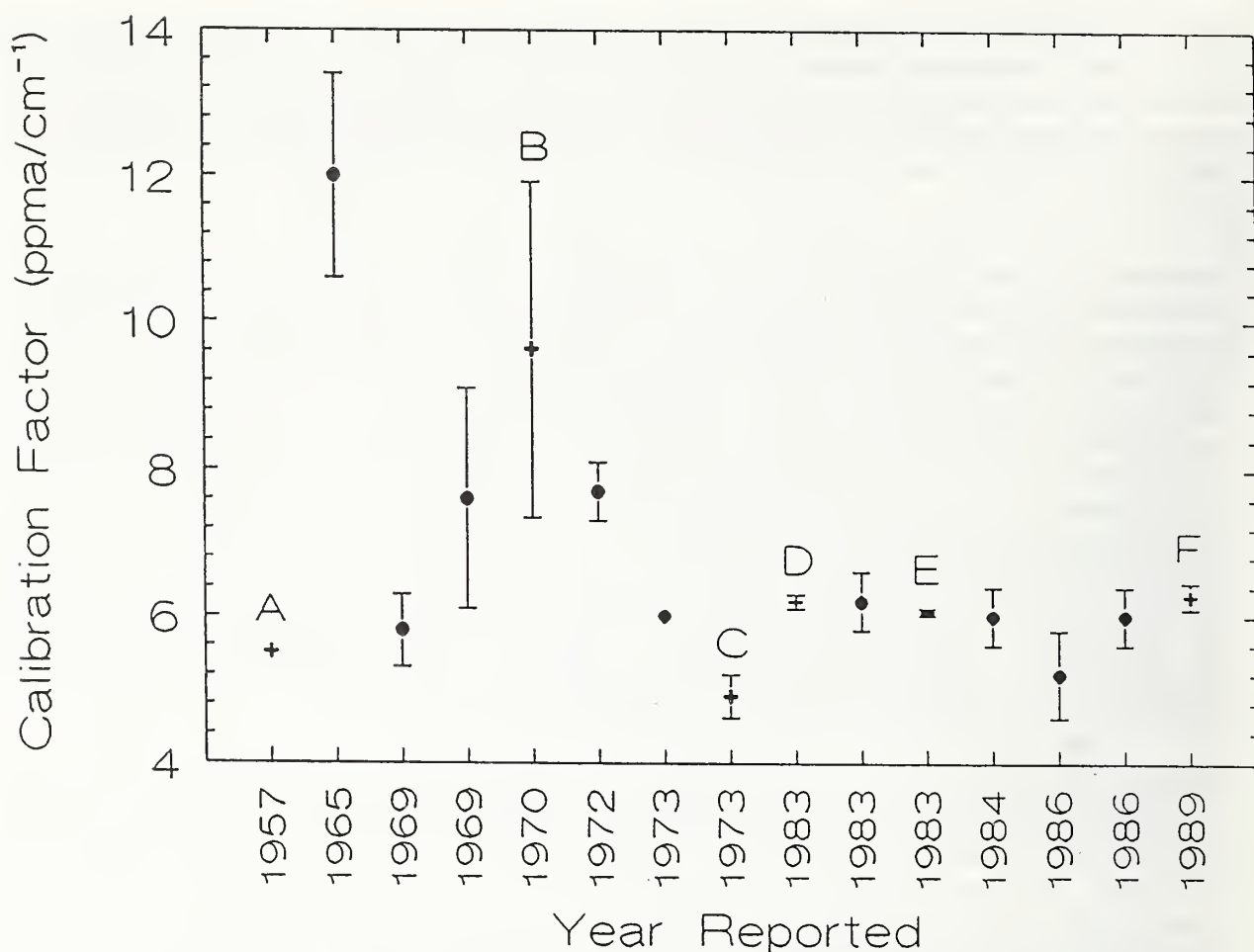


Figure 4. History of the calibration factor for oxygen in silicon by infrared absorption. Values shown as + were adopted by various standards organizations as follows: A: "Kaiser & Keck" used in original ASTM test method (F 45) from 1964 to 1970; B: "Old ASTM" used in ASTM test method (F 121) from 1970 to 1980; C: "DIN" or "New ASTM" used in DIN test method (50438/1) from 1974 and in ASTM test method (F 121) from 1980; D: "Guo Biao" used in Guo Biao test method (Peoples Republic of China) from early 1980s; E: "JEIDA" value used widely in Japan from early 1980s; F: "IOC-88" value being adopted by all standards organizations. (Data are taken from Table III of Ref. 13; see this reference for the origins of values and relevant citations.)

Toward the end of the eighties, another major trend became evident in the semiconductor industry. There was a resurgence of interest in improved quality which led to the **reintroduction** of statistical process control procedures and related quality systems in U.S. industry. Responding to this change, too, has proved to be a challenge for the silicon standards community. A small, but very important, initial step was taken when SEMI shifted the silicon wafer specifications from "goal post" type upper and lower specification limits to a target value with tolerance. From this point it is not too great a transition to go to true distributional specifications — in-process statistical distributions based on process or product measurements over time — with the goal of continuously reducing the variability of the process. Another factor in the quest for ever-decreasing variability in manufacturing processes is the increased need for more precise in-line control measurements, many of which do not even exist. In addition, although there has been great progress in development of process models, these are still in a rudimentary stage and need further refinement.



## **BEYOND SILICON WAFER SPECIFICATIONS**

The SEMI standards program also broadened its scope during the eighties in response to the needs of the industry. It formally became an international organization with active standards development groups in Japan and Europe as well as in the United States. Whereas in the early days the silicon materials activity had driven the program, the growth of the equipment industry led to a major shift in emphasis. Equipment automation became a dominant factor in driving the standards program in response to issues such as wafer transport, machine compatibility, communications, and contamination control. This was a logical direction for the program to take because wafer standardization alone, which had opened up the possibilities, could not drive the development beyond a certain point.

SEMI also began standards development activities in other areas such as pure chemicals and gases, facilities, safety, and packaging to serve the broader needs of the industry. These activities provide standards for the infrastructure which is essential for efficient manufacturing of semiconductor devices and integrated circuits. Many of these standards can be expected to be directly applicable to the production of electronic materials and devices other than silicon.

## **TODAY'S ENVIRONMENT**

The environment in which the challenges of silicon metrology development are being met has changed significantly from that of the early days. The resources available for development of metrology for silicon today are significantly fewer than those which had been available before. Most of the large user companies no longer support extensive metrology research and development and government programs on silicon materials technology are very limited. Instead, the main driving forces for development of standardized test methods are coming from both silicon suppliers themselves and relatively small measurement equipment manufacturers, each of which wants to get its "better" characterization tool to market.

Nevertheless, the demands on the metrology for silicon wafers continue to be very great. These have been clearly documented in several recently issued reports based on a number of sources: a JEIDA study [14], a workshop co-sponsored by SEMATECH, ASTM, SEMI, and NIST [15], a SEMI/JEIDA joint technical conference [16], and a study at the National Institute for Standards and Technology [17]. In response to this need, SEMI, ASTM Committee F-1, and NIST all are continuing active development of metrology and standards.

In the past few years, the SEMI Silicon Wafer and Silicon Epitaxial Wafer Standards Committees have developed several new specifications. These include a specification for a defined wafer coordinate system, a specification for assigning addresses to specific points on an unpatterned silicon wafer, a specification for 100-mm-diameter dielectrically isolated wafers, and a specification for 300-mm-diameter wafers to assist in guiding the development of equipment and processes which will be needed in the latter half of this decade.

## **SILICON WAFER SPECIFICATION FORM**

One of the most significant recent SEMI developments is a standard format for silicon wafer specifications [18] which collects all the parameters which might be specified and provides a common

vocabulary for commercial transactions. This document is a very useful adjunct to the conventional wafer specifications [7] and is intended to assist purchasing agents and specification writers in understanding the complex world of silicon specifications. It was first published in 1990 after several years of intensive development with inputs from both Japan and the United States. The 1993 edition of the standard is reproduced as Appendix A. The standard is in three parts: a brief introductory text; the form itself; and a supporting table of references. The introductory text provides some guidance as to how to use the form. It is intended to be used in conjunction with the SEMI polished wafer [7] or epitaxial wafer [19] specifications which provide complete references to acceptable test methodology, standardized definitions of parameters (such as flatness, resistivity, bow, warp, *sori*, etc.), and standard values for many parameters. The table of references provides information as to whether (and in which standard or standards) the value of the parameter is standardized, location (if any) of a definition or description of the item, and standard test methods for the parameter as developed by ASTM, DIN, or JEIDA. Note that some JEIDA test methods have been issued as Japan Industrial Standards (JIS) while others have not. In general, the test methods listed are technically equivalent, although in some cases there are choices to be made between methods which may yield different results. It is always important when specifying a parameter to specify the test procedure by which its value is to be verified.

The form itself is in four sections. The first contains general information about the order to identify the particular material being described. The second contains parameters appropriate to polished wafers, including epitaxial substrates. The third contains parameters necessary for specification of epitaxial layers. The fourth and newest section contains parameters appropriate for specification of epitaxial wafers with buried layers. Although most buried layer work in the United States is performed by the device manufacturer, the material suppliers are expected to provide such products in Japan. This may indicate the emergence of another trend: device manufacturers in Japan are beginning to expect their material suppliers to perform more of the front end processing, even including some initial patterning steps.

The specification items are grouped according to the type of characteristic. The following groups are identified for polished wafers: general, electrical, chemical, structural, special features (added during wafer manufacture), mechanical, and front and back surface visual inspection. There is a place to insert the specified value for each item or to cite a standardized value. In addition, there are columns to indicate the level of testing required and whether the testing is to be carried out on the product wafer or on a test piece.

Some items are identified as being required when ordering **any** silicon wafer; these include crystal growth method, crystal orientation, dopant, conductivity type, resistivity, and certain mechanical dimensions, including diameter, flat or notch dimensions and locations, thickness, surface orientation, and edge profile contour. These represent the minimum specification list for obtaining any type or quantity of silicon wafers. Something must be entered for each of these items, even though any particular item (such as edge contour or resistivity value) may not be important for the intended application. In such cases, either a very wide range (e.g., 0.1 to 99  $\Omega\cdot\text{cm}$  for resistivity) or “any” may be entered.

Parameters which are most commonly specified are listed in Table 1. Those which are required are indicated by superscript diamonds ( $\diamond$ ). One of the purposes of the format is to provide a standard method for indicating specifications for other parameters which are not yet so well understood and widely utilized. These include minority carrier lifetime, metal contamination level, surface organics, swirl, shallow pits, oxide precipitation, roughness and brightness of the back surface, and special features added in wafer manufacture such as wafer identification marking, extrinsic gettering, backseal characteristics, and the like. In many cases, the test methods for these parameters are not standardized; in some cases,



Table 1. Parameters Most Commonly Specified for Polished Silicon Wafers

Group	Parameter	Standardized Value
General	Growth Method ♦ and Crystal Orientation ♦	No
	Conductivity Type ♦ and Dopant ♦	No
	Nominal Edge Exclusion for Fixed Quality Area	No
Electrical	Resistivity ♦ and Radial Resistivity Variation	No
Chemical	Oxygen and Radial Oxygen Variation	No
	Carbon	No
Structural	Dislocation Etch Pit Density	No
	Slip, Lineage, Twin	No
	Oxidation Induced Stacking Faults	No
Special Features		
Mechanical	Diameter, ♦ Thickness, ♦ and Thickness Variation	Yes
	Flat or Notch Dimensions and Locations ♦	Yes
	Edge Profile ♦	Yes
	Surface Orientation ♦	Yes
	Shape: Bow, Warp, or <i>Sori</i>	Yes
	Flatness	No
Visual Inspection	Front Surface	Yes
	Back Surface	Yes

♦ These items must be specified when ordering silicon wafers.

adequate test methods do not even exist. An example is the case of surface metal contamination levels where the desired specification limit is about the same as the sensitivity of the test method technology.

To describe epitaxial wafers, additional parameters must be specified. Required parameters include wafer description (conductivity type of layer and substrate) together with the dopant, net carrier density, net carrier density variation, thickness, and thickness variation of the layer. Optionally specified items are silicon source gas and growing method, transition width and flat zone (definitions for which are still under development), and post-epi mechanical properties and visual inspection characteristics.

As noted above, the format, like other standards, is continually subject to revision as requirements change. At present, SEMI is considering tighter tolerances on wafer dimensions, limits for surface metal concentrations, specifications for surface microroughness, definitions for flat zone and transition width of epitaxial layers, and ways of detecting surface contamination by particles of size 0.1  $\mu\text{m}$  and smaller. As these items are developed and approved, they will be incorporated into future editions of the wafer specifications and the specification form format.

## OTHER DEVELOPMENTS

ASTM Committee F-1 is developing new procedures to address both the statistical process control and black-box measuring equipment issues as well as developing more precise test methods for wafer geometrical and electrical parameters and new methods for surface metal contamination. It is also beginning to develop consensus reference materials based on the results of interlaboratory testing for other parameters such as flatness, sheet resistance, and net carrier density of epitaxial layers.

NIST is developing new SRM sets for resistivity determination which will have a precision better than that of the previously issued sets, and SRMs for oxygen in silicon are expected to become available later this year. Work is also continuing on a long standing program of developing microelectronic test structures. These structures provide a basis for characterizing the results of a device fabrication process. They are useful both in the design and manufacturing phases of device fabrication, and provide a much-needed tool for evaluating the products of microelectronic foundries. The emergence of these foundry operations is resulting in another split in the industry. Where once device houses did all the work from growing the silicon to designing and processing the devices, the day of the "fabless" device house has arrived. This effectively separates the device design and processing functions. As with the other interfaces in the industry, good communications and stable relationships across this boundary are essential for good results.

Thus, despite the limited resources and a slower rate of production than the heady days of the sixties, considerable progress is being made in developing the metrological tools for silicon material and process technologies required for fabrication of high density circuits with sub-micrometer design rules.

## IN-PROCESS METROLOGY

These activities, while essential, all relate to supplier-user interfaces. However, today the need is also for in-line control of wafer and device manufacturing processes. Significant reductions in cycle time and direct labor hours together with increases in output and equipment uptime can be achieved by increased use of in-line sensors and data links [17]. This topic has received attention from both SRC and SEMATECH. Both have conducted numerous workshops and SRC has established a university center on metrology.

To focus more attention on the issue of in-process metrology, ASTM and SEMI joined with JEIDA, JESSI,<sup>4</sup> NIST, SEMATECH, and SRC to conduct an international workshop in November 1992 [20]. This workshop was charged to formulate and publish a plan for the development of measurement tools, techniques, and standards for qualifying process equipment and for controlling and improving unit processes. This plan will provide guidance and motivation for metrological research, development, and standardization activities in the industry.

Nearly 75 individuals representing manufacturers of materials, process equipment, metrology instruments, and devices; universities; and government agencies participated in the workshop. There were seven working groups which covered film deposition (including epitaxy), contamination, implantation, etching, oxidation and diffusion (both furnace and rapid thermal processing), lithography, and materials. The

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<sup>4</sup> JESSI — Joint European Submicron Silicon Initiative.



most heavily represented category was metrology instrument manufacturers; otherwise, the representation in most of the working groups was reasonably well balanced, except that process equipment manufacturers were not represented in several of the groups.

Each working group met three times. The first session was a brainstorming session in which measurement issues and requirements were developed. In the second session, the groups prioritized the requirements and, in the final session, developed a set of recommendations for specific metrology development and standardization activities.

In carrying out their discussions, the groups employed the following proposed definitions:

*in-situ metrology* — metrology in which the sensor is embedded in the process tool, monitoring directly and in real time the effects of the process on product or process variables, thus providing a real-time measure of the result of process conditions with the possibility of active control.

*in-line metrology* — metrology in which a metrology tool is integrated into the process line with all of the product flowing through it, thus providing data, which can be used for both statistical modeling and feedback/feed forward process control, for up to 100% of the product on the effects of the preceding processes on the product.

*on-line metrology* — metrology in which a metrology tool is attached to the process line and automatically receives transferred product at a predetermined sampling rate (up to 100%), thus providing data, which can be used for both statistical modeling and feedback-feed forward process control, for up to 100% of the product on the effects of the preceding processes on the product.

*off-line metrology* — metrology in which product samples are brought to the metrology tool which is located remotely from the process line, thus providing diagnostic product data that are useful in understanding, modeling, or troubleshooting a process but do not provide a mechanism for feedback/feed forward control of a process.

Although the report of the workshop is yet to be issued, a number of critical technical issues were identified in the preliminary summaries of the working group deliberations which were presented at the end of the workshop. These included both material characteristics (such as surface microroughness, thickness and resistivity of very thin films, and surface metal concentrations) and measurement technology (such as *in-situ* particle detection in process tools, including those introduced by the process itself; *in-situ* surface temperature measurement; patterned wafer inspection and analysis; and applications of test element groups, or microelectronic test patterns). There was much discussion of P/T ratios, the ratio of the precision of a test procedure to the specification limit for the parameter being tested. As a rule of thumb, the P/T ratio should be  $\leq 10\%$ ; for normal distributions, this implies that

$$\frac{6\sigma}{USL-LSL} \leq 0.1$$

where  $\sigma$  is the standard deviation of the measurement result, USL is the upper specification limit and LSL is the lower specification limit. Thus, for this case, the standard deviation of the measurement tool must be 1/60th of the desired specification range, or less. Not many measurements today have this kind of precision, even on a single-instrument basis.

Detailed recommendations on specific topics were made by each of the working groups. The following items suggest the common threads of many of these recommendations. The report of the workshop should be consulted for the detailed recommendations.

- Develop improved modes of communication between disciplines and between suppliers and users.
- Improve accuracy of critical test measurements to support both material specifications and process control requirements, or, alternatively, adjust specification limits so that they conform with the P/T ratios of available measurement technology.
- Improve process models in order to improve the prediction capabilities of in-process measurements.
- Develop a cost-of-ownership model for metrology tools.
- Develop a wide range of *in-situ* measurement techniques.
- Improve spatial resolution and sensitivity of measurement techniques.
- Develop systems for efficiently converting raw data into useful information.

Increased focus on in-process metrology and control will diminish the current emphasis on testing of materials to a particular specification, but in no way diminishes the need for materials characterization. Until process models are significantly improved, it will be virtually impossible to control most processes solely with *in-situ* or in-line measurements of process parameters, such as temperature, flow rates, and time. Nondestructive *in-situ* and in-line measurements on product samples (which may be as great as 100%) will continue to be required for the foreseeable future. If anything, the demands on characterization techniques will become more severe in terms of both sensitivity and repeatability, because assurance that the level of "out-of-spec" units is in the parts-per-million range requires great measurement precision. First, as discussed above, P/T ratios must be improved. Secondly, the sensitivity of many measurements is not adequate, as noted in the example of surface metals contamination on silicon wafers. Thus, considerable improvement in most materials characterization measurements remains a requirement.

The problems and issues discussed above are not unique to silicon and silicon-based devices. Many of them apply equally well to other materials and device families. The ability to control the device process and to trace specific device structures back to the starting material and the various elements of the process by which they were made is critical to the improvement of both device performance and manufacturing efficiency. The importance of the ability to make this connection is greater, the more direct the relationship between material characteristics and device performance.

### INDUSTRY-WIDE PLANNING

Also, in November 1992, the Semiconductor Industry Association (SIA) conducted a workshop to lay out the technological roadmap that the silicon device and integrated circuit industry will follow into the next century. The SIA Semiconductor Technology Workshop [21] involved 180 invited experts from all aspects of silicon device development and manufacturing, from the materials and equipment industrial infrastructure, and from universities and Government laboratories having related programs. The participants were devised in advance into 11 working groups. Each working group addressed a carefully defined subject area chosen so that no significant area of device design or manufacture was left uncovered.

The workshop dealt specifically with mainstream silicon metal-oxide-semiconductor (MOS) integrated circuit technology. It sought to identify the technical directions and accomplishments needed to make



succeeding generations of devices at 2-year intervals over the next 15 years. This was a heroic objective. The outcome was a comprehensive and detailed plan which resulted from careful planning and substantial pre-work activity by each participant. Nevertheless, the results were necessarily incomplete. For example, equipment developments are for the most part implied rather than clearly defined. Similarly, metrological needs must be inferred from the context. The plan will be fleshed out by independently sponsored specialist workshops and maintained technically current through periodic reviews by the SIA.

Of particular relevance to the subject of this report is the fact that metrology was identified by the workshop as one of the seven pervasive technology competencies essential to the successful execution of the roadmap. The work of ASTM, SEMI, and NIST (as outlined in the foregoing sections) was acknowledged. Strong recommendations were made regarding the necessary course of measurement development, and a target budget for metrology (5% of die cost, exclusive of packaging, test, and design) was established. SEMI has already revised its U.S. standards development program plans to reflect the needs identified by the workshop. NIST is doing the same with its metrology R&D plans.

The importance of standardization of wafer diameter (also discussed earlier in this report) was reaffirmed by many of the workshop working groups. Reference to Figure 3 shows that wafer diameters have increased with each DRAM generation since the early eighties. The introduction of large volumes of 200-mm wafers was delayed past its expected date because of both technical and economic issues. It appears that the transition to the next larger wafer diameter will be even more difficult than the transition to 200-mm wafers has been. The workshop concluded that identification of the next wafer size was one of seven key industry structure issues affecting the technology environment. Previous transitions have been justified by balancing the larger number of available die per wafer against the larger cost of process equipment and facilities; costs of development of the new process technologies has not so far been significant compared to other process evolution costs. However, the workshop concluded that "for wafer diameters of greater than 200 mm, wafer size conversion issues cannot be ignored," and recommends that a working group be established to develop more detailed models to evaluate the economic benefits of moving to larger wafer sizes so that the wafer size evolution can be predicted in a timely manner.

The occurrence of this workshop is evidence of the increasing maturing of the semiconductor industry. This event defined the needs of a major U.S. industry to an extent never before achieved for any industry, and in doing so, the industry has expressed its needs for measurements, materials, and manufacturing tools far more clearly than at any previous time. As noted in the earlier sections, measurement developments in past years have occurred with much less guidance from the device industry. This clearer pathway and greater cooperation among the interested parties (another workshop recommendation) will perhaps lead to significant improvements in the way measurement science and technology are developed and delivered.

## **CONCLUSIONS AND RECOMMENDATIONS**

In drawing the various threads of the silicon metrology development together, we find that there have been a number of key factors which led to successful results. Many of these would appear to apply to similar developments in connection with other materials.

### **KEY FACTORS**

It all began with freely shared basic research results which provided a solid foundation for future development and growth. After some time, there was a widely recognized need for standardization of



test procedures to facilitate orderly exchange of materials in the marketplace; without this recognition, the development of standards stagnates. Along with the recognition of the need, there was available an organizational vehicle, ASTM Committee F-1, which was richly supported by major corporations and NBS. The cornerstone of standard test method development in this organization was direct involvement of both suppliers and users in experimental verification of the validity and precision of the test procedures — to the ultimate benefit of the participants, document quality, and the industry at large.

The need for common ground and a willingness to share relevant information was amply demonstrated by the failure of Committee F-1 to develop standards for phosphor materials. Also, the need for the involvement of experts in the field was demonstrated by the difficulties encountered in the attempts to develop standards for trace analytical methods. Although the presence of these items cannot ensure success, their absence is certain to produce failure.

A turning point in the application of standardized test methodology for silicon material properties occurred with the standardization of silicon wafer dimensions in the early seventies. The key point here was the specification of a limited set of dimensional parameters coupled with considerable flexibility in application-sensitive parameters. Not only did this increase awareness of the standardized test procedures (even those for which parameter values were not standardized), it also provided for orderly growth as wafer diameters increased, laid the foundations for the development and growth of the merchant semiconductor equipment industry, and accelerated the internationalization of wafer standardization.

Although the demands on silicon metrology continued to increase as a result of decreases in feature size and increases in circuit complexity, die area, and wafer diameter, the driving force in standards development gradually shifted from the material itself to process equipment. In addition, the main burden for developing improved, publicly available test methodology shifted from the major device and systems houses to relatively small producers of measurement equipment. Test method standardization is complicated by the widespread existence of black-box instruments which contain the essence of the measurement technique imbedded within their software; often this software is inaccessible to the user. To the need for increased sensitivity and reproducibility of both traditional and new measurements has been added the need for increased in-process measurement capability in a total quality system environment. These issues are currently posing severe challenges for the metrology and standards communities in the silicon industry.

A good methodology for process diagnosis and control is an essential feature for applying test procedures to the manufacturing environment. This was provided in the early days of integrated circuit manufacture by the combination of MIL-STD-883 and the NASA Line Certification Program, but their effectiveness was diluted by resistance to their application and the widespread use of waivers. Not until many years later were statistical quality control procedures reintroduced into U.S. manufacturing environments, but they are now being implemented throughout the semiconductor industry.

Finally, close cooperation between device and materials manufacturers, first evidenced in the successful Japanese VLSI development in the early seventies and most recently recommended by the SIA Semiconductor Technology Workshop, is necessary for efficient production of quality devices. Such cooperation facilitates effective resolution of technological problems and provided definition for future materials and metrology developments.

## RECOMMENDATIONS

Most of the developments we have discussed provide direct or indirect guidance for application to other materials. For materials with small, specialized markets, the basics are most critical:

1. Establish common ground and a willingness to share relevant information; develop consensus standards for terminology, test methods for basic properties, and specification formats to ensure that individually developed specifications are meaningful and understood.
2. Involve experts in the development of standards; feed back the experience gained in standards development to R&D groups for them to build further improvements.
3. Generate specifications with standardized values for parameters needed for orderly flow of materials in manufacturing.
4. Assure that the measurement technology supports the necessary specifications with regard to sensitivity and repeatability.
5. Apply statistical process control tools in a total quality system, using all available in-process control metrology for both product and process parameters.

Finally, the issue of market size cannot be overlooked; for maximum effectiveness, no matter what else is done, it is essential to take advantage of developments made by the silicon industry whenever they can be applied, either unchanged or with modest modifications.

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**APPENDIX A**

**SEMI M18-93**

**FORMAT FOR SILICON WAFER SPECIFICATION FORM FOR ORDER ENTRY**

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## SEMI M18-93

# FORMAT FOR SILICON WAFER SPECIFICATION FORM FOR ORDER ENTRY

### 1. Scope

1.1 This format provides a standard form for specifying several classifications of silicon wafers, as follows:

1.1.1 Polished Silicon Wafers.

1.1.2 Epitaxial Silicon Wafers.

1.1.3 Epitaxial Silicon Wafers with Buried Layer.

1.2 The form is designed to be used in conjunction with other SEMI specifications where details of the dimensional, physical, electrical, and chemical properties are defined or specified. However, the form includes many items that are not currently included in the SEMI specifications. Also, many items are not now commonly specified, but may find increased importance in the future. The intention is to provide for flexibility and expansion of the technology.

1.3 This format provides for specifying and ordering silicon wafers with varying levels of complexity. The minimum level of completeness is shown in each case, with additional options included to allow for customization of the wafer to the specific processing requirements of the user. If a particular item is not of interest, no entry is required. The only required entries are those marked as such for the purpose of minimal specification (diameter, orientation, dopant, resistivity, etc.).

1.4 Values for many items are listed either in the polished silicon wafer standards in SEMI M1 or in the defect limits tables in SEMI M1, SEMI M2, or SEMI M11. If these standard specifications are sufficient for defining the wafers, only a single entry is required in each section of the form.

1.5 For referee purposes, U.S. Customary units shall be used for wafers of 2- and 3-inch diameters, and SI (System International, commonly called metric) units for 100-mm and larger diameter wafers.

### 2. Applicable Documents

#### 2.1 SEMI Specifications

SEMI M1	Specifications for Polished Monocrystalline Silicon Wafers
SEMI M2	Specifications for Silicon Epitaxial Wafers

SEMI M11      Specifications for Silicon Epitaxial Wafers for Advanced Applications

SEMI M12      Specification for Serial Alphanumeric Marking of the Front Surface of Wafers

SEMI M13      Specifications for Alphanumeric Marking of Silicon Wafers

SEMI M20      Specification for Establishing a Wafer Coordinate System

2.2 Test methods referenced in Table 1 are cited in SEMI M1, SEMI M2, or SEMI M11.

### 3. Definitions

3.1 The items listed in the form are referenced and defined in various documents. A reference for most items in Parts 2 and 3 of the form is listed in Table 1. The entries in the table are keyed to the form by item number. Because terms related to epitaxial wafers with buried layer are defined in this standard and because no standardized test methods for the buried layer parameters exist, Table 1 does not include line items from Part 4 of the form.

3.2 General term used in this standard:

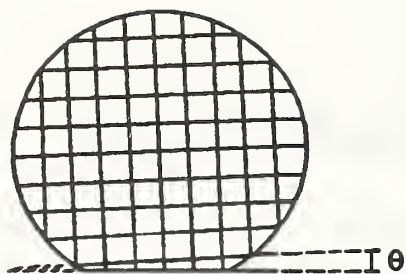
*required (req. or req'd)* - when applied to a parameter listed in the order form, a user supplied value is necessary to minimally define the material for manufacture.

3.3 Terms related to epitaxial wafers with buried layers:

*alignment precision* - pattern displacement in first mask photolithography process.

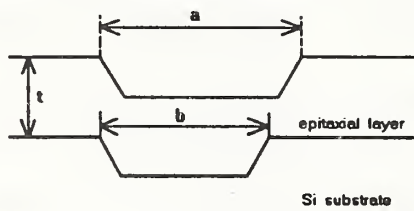
NOTE 1 - Alignment precision is specified by maximum values of X and Y, the displacement of the center of the pattern from a reference position defined in the wafer specification in terms of the wafer coordinate system defined in SEMI M20, and the maximum value of  $\theta$ , the angle between the x-axis of the pattern and the primary orientation flat, see Figure 1.

*pattern distortion ratio* - Absolute magnitude of the quotient of the (1) difference between the width of the pattern on the substrate and the width of the pattern on the top surface of the epitaxial layer and (2) the thickness of the epitaxial layer.



**Figure 1**

First mask pattern showing angular displacement,  $\theta$ .



**Figure 2**

Cross sectional view of epitaxial layer showing the pattern widths,  $a$ , at the epi surface, and  $b$ , at the layer-substrate interface.

NOTE 2 - Pattern distortion ratio is specified by a maximum value of  $Y$ , a dimensionless quantity given by the quotient:  $Y = c/t$ ,

where

$$c = |a - b|,$$

$a$  = width of the pattern on the top surface of the epitaxial layer, in  $\mu\text{m}$ ,

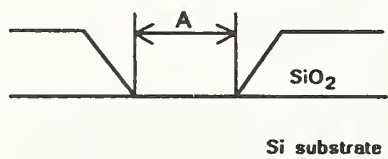
$b$  = width of the pattern on the top of the substrate wafer, in  $\mu\text{m}$ , and

$t$  = the thickness of the epitaxial layer, in  $\mu\text{m}$ .

See Figure 2.

**pattern line width tolerance** - allowed variation in pattern line width on substrate surface.

NOTE 3 - Pattern line width is specified as  $A = X \pm Y$ , where  $X$  is the nominal value in mm and  $Y$  is the tolerance in  $\mu\text{m}$ . See Figure 3.

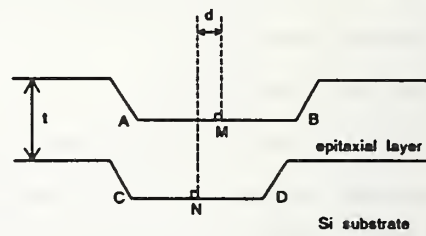


**Figure 3**

Schematic diagram showing line width,  $A$ , of pattern on substrate wafer.

**pattern shift ratio** - lateral distance between the center point of the pattern on the surface of the substrate and the center point of the pattern on the surface of the epitaxial layer divided by the epitaxial layer thickness.

NOTE 4 - Pattern shift ratio,  $d/t$  (see Figure 4), is specified in terms of a nominal value,  $X$ , and a tolerance,  $\pm Y$ , both of which are dimensionless because both  $d$  and  $t$  are in  $\mu\text{m}$ .

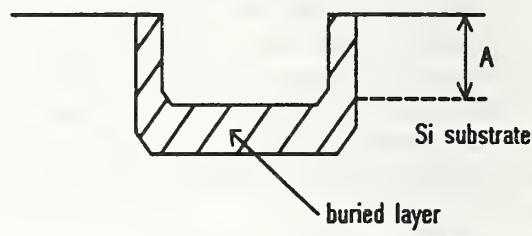


**Figure 4**

Cross sectional view of epitaxial wafer showing the pattern shift,  $d$ . Not to scale:  $AM=MB$  and  $CN=ND$ .

**pattern step height** - difference in vertical position of the diffused (buried layer) surface and the original substrate surface, after removal of oxide.

NOTE 5 - Pattern step height,  $A$ , is specified as a nominal value,  $X$ , and a tolerance  $\pm Y$ , both in nm. See Figure 5.



**Figure 4**

Cross sectional view of epitaxial substrate after oxide removal but before deposition of the epitaxial layer showing the pattern step height,  $A$ .

## 4. Use of the Form

4.1 If this form is used in conjunction with purchase orders for silicon wafers, Parts 1 and 2 shall be completed. For epitaxial wafers, Parts 1, 2, and 3 shall be completed. For epitaxial wafers with buried layer, Parts 1, 2, 3, and 4 shall be completed.

4.2 In all cases, items listed as required must have a value or choice indicated to minimally specify the material.

4.3 Certain required dimensional items may be specified as a group according to the standard values presented in the applicable SEMI specification, or they may be specified individually.





4.4 Visual inspection criteria may be specified as a group according to the standard values listed in the applicable SEMI specification, or they may be specified individually.

4.5 For either dimensional values or visual inspection criteria, the appropriate SEMI specification may be marked and an optional line item (or items) marked as well. In this case, the value marked on each individual line item takes precedence over the standard value.

4.6 If the suggested form included in this format is not reproduced and used as a fill-out form, the items and responses must be adequately identified so that the information and requirements are clear to all parties.

## **5. Test Methods**

5.1 Measurements shall be made or certifiable to the ASTM, JEIDA, JIS, or DIN standard test method as cited in Table 1.

5.2 When standard test methods from different geographic regions are available, the default method shall be the method in common usage for the region of the purchaser of the wafer.

5.3 If several different standard test methods for an item are commonly used within a region, a specific entry must be made to identify which method of test is applicable.

5.4 If no standard test method for an item is available, the test procedure must be specified.

## **6. Testing Level and Certification**

6.1 Material ordered using this format shall be tested and/or certified to the limits set forth in the individual criteria.

6.2 The actual testing level, whether the test is performed on all wafers, a sample of the wafers, special test pieces representing all portions of the material, or a sample of the test pieces, may be specified using this format.

6.3 In some cases, the material may be certified as "capable of meeting" certain requirements. In this context, the supplier is not required to perform the tests outlined in this format. However, if the purchaser performs the test and the material fails to meet the requirement, the material may be subject to rejection.



## SEMI SILICON WAFER SPECIFICATION FORM FOR ORDER ENTRY (Page 1)

## PART 1. GENERAL INFORMATION

ITEMS		INFORMATION	Date:
Customer Name			
Purchase Order Number			
	Line Number		
	Item Number		
General Specification Number			
	Revision Level		
Part Number/Revision			

## PART 2. POLISHED WAFER

CUSTOMER:		PART NUMBER:	REVISION	DATE:			
R E Q	ITEM	SPECIFICATION	TESTING LEVEL				
			WAFER		TEST PIECE		
			100%	SAMPLE	100%	SAMPLE	
1. GENERAL CHARACTERISTICS							
◆	1.1	Growth Method	<input type="checkbox"/> Cz <input type="checkbox"/> FZ <input type="checkbox"/> MCz				
◆	1.2	Crystal Orientation	<input type="checkbox"/> (100) <input type="checkbox"/> (111) <input type="checkbox"/> ( )				
◆	1.3	Conductivity Type	<input type="checkbox"/> p <input type="checkbox"/> n				
◆	1.4	Dopant	<input type="checkbox"/> B <input type="checkbox"/> Phos <input type="checkbox"/> Sb <input type="checkbox"/> As <input type="checkbox"/> NTD				
	1.5	Nominal Edge Exclusion Distance for Fixed Quality Area	6.10 - 6.14; 11 <input type="checkbox"/> 3 mm <input type="checkbox"/> 5 mm <input type="checkbox"/> other ____ mm 7, 8, 12, 13 <input type="checkbox"/> 3 mm <input type="checkbox"/> 5 mm <input type="checkbox"/> other ____ mm (except edge defects)				
2. ELECTRICAL CHARACTERISTICS							
◆	2.1	Resistivity	Nominal <input type="checkbox"/> ± Tolerance <input type="checkbox"/> Ω-cm				
		Measurement Position	<input type="checkbox"/> Center Point <input type="checkbox"/> Other:				
	2.2	Radial Resistivity Variation (RRG)	Not greater than <input type="checkbox"/> %				
		Measurement Position	ASTM F 81 Fig. 1- <input type="checkbox"/> A, <input type="checkbox"/> B, <input type="checkbox"/> C, <input type="checkbox"/> D; <input type="checkbox"/> JEIDA				
		Calculation Method	<input type="checkbox"/> ASTM F 81 <input type="checkbox"/> JEIDA <input type="checkbox"/> Other:				
	2.3	Resistivity Striations	Not greater than <input type="checkbox"/> %				
	2.4	Minority Carrier Lifetime	Greater than <input type="checkbox"/> μs				
		Test Method	ASTM F28 <input type="checkbox"/> A, <input type="checkbox"/> B; ASTM F391 <input type="checkbox"/> A, <input type="checkbox"/> B; <input type="checkbox"/> Other				
3. CHEMICAL CHARACTERISTICS							
	3.1	Oxygen Concentration	Nominal <input type="checkbox"/> ± Tolerance <input type="checkbox"/> x 10 <sup>18</sup> cm <sup>-3</sup> or ppma				
		Calibration Factor	<input type="checkbox"/> IOC-88 <input type="checkbox"/> old ASTM <input type="checkbox"/> Other:				
		Measurement Method	<input type="checkbox"/> IR <input type="checkbox"/> SIMS <input type="checkbox"/> GFA				
	3.2	Radial Oxygen Variation	Not greater than <input type="checkbox"/> %				
		Measurement Position	ASTM F 951 Plan <input type="checkbox"/> A <input type="checkbox"/> B <input type="checkbox"/> B-1 <input type="checkbox"/> C <input type="checkbox"/> D <input type="checkbox"/> Other:				
		Calculation Method	ASTM F 951 Plan <input type="checkbox"/> A <input type="checkbox"/> B <input type="checkbox"/> B-1 <input type="checkbox"/> C <input type="checkbox"/> D <input type="checkbox"/> Other:				
	3.3	Carbon Concentration	Not greater than <input type="checkbox"/> ppma				
	3.4	Metallic Content	Not greater than <input type="checkbox"/> ppma				
	3.5	Surface Organics	Not greater than <input type="checkbox"/> /cm <sup>2</sup>				
4. STRUCTURAL CHARACTERISTICS							
	4.1	Dislocation Etch Pit Density	<input type="checkbox"/> Not greater than <input type="checkbox"/> /cm <sup>2</sup>				
	4.2	Slip	<input type="checkbox"/> None <input type="checkbox"/> Other:				
	4.3	Lineage	<input type="checkbox"/> None <input type="checkbox"/> Other:				
	4.4	Twin	<input type="checkbox"/> None <input type="checkbox"/> Other:				
	4.5	Swirl	<input type="checkbox"/> Not greater than <input type="checkbox"/> % of wafer area				
	4.6	Shallow Pits	Not greater than <input type="checkbox"/> /cm <sup>2</sup>				
	4.7	Oxidation Induced Stacking Faults (OSF)	Not greater than <input type="checkbox"/> /cm <sup>2</sup>				
		Test Cycle	ASTM F 416 Cycle- <input type="checkbox"/> 1 <input type="checkbox"/> 2 <input type="checkbox"/> 3 <input type="checkbox"/> Other:				
	4.8	Oxide Precipitates(BMD) Interstitial Oxygen Reduction (ΔO <sub>i</sub> )	Range: <input type="checkbox"/> to <input type="checkbox"/> /cm <sup>2</sup> <input type="checkbox"/> ppma				
		Test Cycle	ASTM F1239 <input type="checkbox"/> A, <input type="checkbox"/> B; <input type="checkbox"/> Other:				



# SEMI SILICON WAFER SPECIFICATION FORM FOR ORDER ENTRY (Page 2)

## PART 2. POLISHED WAFER (continued)

CUSTOMER:		PART NUMBER:	REVISION:	DATE:			
REQ	ITEM	SPECIFICATION	TESTING LEVEL				
			WAFER		TEST PIECE		
			100%	SAMPLE	100%	SAMPLE	
<b>5. WAFER PREPARATION CHARACTERISTICS</b>							
5.1	Wafer ID Marking	<input type="checkbox"/> None <input type="checkbox"/> SEMI M12 <input type="checkbox"/> SEMI M13 <input type="checkbox"/> Other:					
5.2	Front Surface Thin Film(s) Appl	<input type="checkbox"/> None <input type="checkbox"/> Description:					
5.3	Denuded Zone	<input type="checkbox"/> None <input type="checkbox"/> Description:					
5.4	Extrinsic Gettering Treatment	<input type="checkbox"/> None <input type="checkbox"/> Description:					
5.5	Backseal	<input type="checkbox"/> None <input type="checkbox"/> Description:					
5.6	Annealing	<input type="checkbox"/> None <input type="checkbox"/> Description:					
<b>6. MECHANICAL CHARACTERISTICS</b>							
THE ITEMS LISTED IN THIS SECTION MAY BE							
6.0I	<input type="checkbox"/> Specified According to SEMI MI. _____						
OR SPECIFIED INDIVIDUALLY							
◆ 6.1	Diameter <sup>1</sup>	Nominal [ ] ± Tolerance [ ] mm					
◆ 6.2	Primary Flat Length/Diameter Notch Dimensions <sup>1</sup>	<input type="checkbox"/> SEMI MI. _____ <input type="checkbox"/> Other: _____ mm					
◆ 6.3	Primary Flat/Notch Orientation <sup>1</sup>	<input type="checkbox"/> SEMI MI. _____ <input type="checkbox"/> Other:					
◆ 6.4	Secondary Flat Length <sup>1</sup>	<input type="checkbox"/> SEMI MI. _____ <input type="checkbox"/> Other: _____ mm <input type="checkbox"/> None					
◆ 6.5	Secondary Flat Location <sup>1</sup>	<input type="checkbox"/> SEMI MI. _____ <input type="checkbox"/> Other: _____ <input type="checkbox"/> None					
◆ 6.6	Edge Profile <sup>1</sup>	<input type="checkbox"/> SEMI Standard [ ] Other:					
◆ 6.7	Thickness <sup>1</sup>	Nominal [ ] ± Tolerance [ ] μm					
6.8	Thickness Variation (TTV) <sup>1</sup>	<input type="checkbox"/> SEMI MI. _____ <input type="checkbox"/> Other: _____ μm					
	Measurement Position	<input type="checkbox"/> F 533 <input type="checkbox"/> F 657 <input type="checkbox"/> H 611 <input type="checkbox"/> Other:					
◆ 6.9	Surface Orientation	<input type="checkbox"/> 0.00 ± 0.50 <input type="checkbox"/> 2.50 ± 0.50 <input type="checkbox"/> 4.00 ± 0.50 <input type="checkbox"/> Other:					
6.10	Bow <sup>1</sup>	<input type="checkbox"/> SEMI M1 _____ <input type="checkbox"/> Other: _____ μm					
6.11	Warp <sup>1</sup>	<input type="checkbox"/> SEMI M1 _____ <input type="checkbox"/> Other: _____ μm					
6.12	Sori	<input type="checkbox"/> _____ μm					
6.13	Flatness/Global	Acronym: <sup>2</sup> [ ] [ ] [ ] [ ] Value _____ μm					
6.14	Flatness/Site	Acronym: <sup>2</sup> [ ] [ ] [ ] [ ] Value _____ μm Site Size _____ x _____ mm Total Sites _____ % Usable Area _____ <input type="checkbox"/> Include partial sites					
<b>7. FRONT SURFACE VISUAL INSPECTION CHARACTERISTICS</b>							
THE ITEMS LISTED IN THIS SECTION MAY BE							
7.0I	<input type="checkbox"/> Specified According to SEMI MI TABLE I						
OR SPECIFIED INDIVIDUALLY							
7.1	Scratches <sup>3</sup>	<input type="checkbox"/> SEMI MI Table 1 <input type="checkbox"/> Other:					
7.2	Pits <sup>3</sup>	<input type="checkbox"/> SEMI MI Table 1 <input type="checkbox"/> Other:					
7.3	Haze <sup>3</sup>	<input type="checkbox"/> SEMI MI Table I <input type="checkbox"/> Other:					
7.4	Light Point Defects (Particulate Contamination) <sup>3</sup>	<input type="checkbox"/> SEMI MI Table 1 <input type="checkbox"/> Other:					
7.5	Contamination/Area <sup>3</sup>	<input type="checkbox"/> SEMI MI Table 1 <input type="checkbox"/> Other:					
7.6	Edge Chips <sup>3</sup>	<input type="checkbox"/> SEMI MI Table 1 <input type="checkbox"/> Other:					
7.7	Edge Cracks <sup>3</sup>	<input type="checkbox"/> SEMI MI Table 1 <input type="checkbox"/> Other:					
7.8	Cracks, Crow's Feet <sup>3</sup>	<input type="checkbox"/> SEMI MI Table I <input type="checkbox"/> Other:					
7.9	Craters <sup>3</sup>	<input type="checkbox"/> SEMI MI Table I <input type="checkbox"/> Other:					
7.10	Dimples <sup>3</sup>	<input type="checkbox"/> SEMI MI Table 1 <input type="checkbox"/> Other:					
7.11	Grooves <sup>3</sup>	<input type="checkbox"/> SEMI MI Table I <input type="checkbox"/> Other:					
7.12	Mounds <sup>3</sup>	<input type="checkbox"/> SEMI MI Table I <input type="checkbox"/> Other:					
7.13	Orange Peel <sup>3</sup>	<input type="checkbox"/> SEMI MI Table I <input type="checkbox"/> Other:					
7.14	Saw Marks <sup>3</sup>	<input type="checkbox"/> SEMI MI Table I <input type="checkbox"/> Other:					
7.15	Dopant Striation Rings	<input type="checkbox"/>					
7.16	Stains	<input type="checkbox"/>					





## SEMI SILICON WAFER SPECIFICATION FORM FOR ORDER ENTRY (Page 3)

### PART 2. POLISHED WAFER (continued)

CUSTOMER:		PART NUMBER:	REVISION:	DATE:			
R E Q	ITEM	SPECIFICATION	TESTING LEVEL				
			WAFER		TEST PIECE		
			100%	SAMPLE	100%	SAMPLE	
8. BACK SURFACE VISUAL INSPECTION CHARACTERISTICS							
THE ITEMS LISTED IN THIS SECTION MAY BE							
	8.01	<input type="checkbox"/> Specified According to SEMI M1 Table 1					
OR SPECIFIED INDIVIDUALLY							
	8.1	Edge Chips <sup>3</sup> <input type="checkbox"/> SEMI M1 Table 1 <input type="checkbox"/> Other:					
	8.2	Cracks, Crow's Feet <sup>3</sup> <input type="checkbox"/> SEMI M1 Table 1 <input type="checkbox"/> Other:					
	8.3	Contamination/Area <sup>3</sup> <input type="checkbox"/> SEMI M1 Table 1 <input type="checkbox"/> Other:					
	8.4	Saw Marks <sup>3</sup> <input type="checkbox"/> SEMI M1 Table 1 <input type="checkbox"/> Other:					
	8.5	Stains <input type="checkbox"/>					
	8.6	Roughness <input type="checkbox"/>					
	8.7	Brightness <input type="checkbox"/>					
9. OTHER CHARACTERISTICS							

### PART 3. EPITAXIAL WAFER

CUSTOMER:		PART NUMBER:	REVISION:	DATE:			
R E Q	ITEM	SPECIFICATION	TESTING LEVEL				
			WAFER		TEST PIECE		
			100%	SAMPLE	100%	SAMPLE	
10. GENERAL EPITAXIAL WAFER AND LAYER CHARACTERISTICS							
◆	10.1	Conductivity Type/Structure <input type="checkbox"/> n/n+ <input type="checkbox"/> p/p+ <input type="checkbox"/> Other:					
◆	10.2	Dopant <input type="checkbox"/> B <input type="checkbox"/> Phos <input type="checkbox"/> As					
	10.3	Silicon Source Gas <input type="checkbox"/> SiH <sub>4</sub> <input type="checkbox"/> SiH <sub>2</sub> Cl <sub>2</sub> <input type="checkbox"/> SiHCl <sub>3</sub> <input type="checkbox"/> SiCl <sub>4</sub>					
	10.4	Growth Method Reactor <input type="checkbox"/> Pressure <input type="checkbox"/>					
◆	10.5	Net Carrier Density (Resistivity) Nominal <input type="checkbox"/> ± Tolerance <input type="checkbox"/> (check unit below)					
		Units <input type="checkbox"/> 10 <sup>1</sup> atoms/cm <sup>3</sup> ; <input type="checkbox"/> Ω·cm					
		Test Method <input type="checkbox"/> Hg C-V; ASTM F419 <input type="checkbox"/> Gated, <input type="checkbox"/> Ungated, <input type="checkbox"/> Schottky; <input type="checkbox"/> ASTM F374 (4-Pt); <input type="checkbox"/> ASTM F525 (SRP); <input type="checkbox"/> Other _____					
◆	10.6	Net Carrier Density Variation <input type="checkbox"/> SEMI M2 <input type="checkbox"/> Not greater than <input type="checkbox"/> %					
		Measurement Position <input type="checkbox"/> SEMI M2 <input type="checkbox"/> SEMI M11 <input type="checkbox"/> Other:					
		Calculation <input type="checkbox"/> SEMI M2 <input type="checkbox"/> SEMI M11 <input type="checkbox"/> Other:					
◆	10.7	Thickness Nominal <input type="checkbox"/> ± Tolerance <input type="checkbox"/> μm					
		Test Method <input type="checkbox"/> FT-IR <input type="checkbox"/> ASTM F 672 (SRP)					
◆	10.8	Thickness Variation <input type="checkbox"/> SEMI M2 <input type="checkbox"/> Not greater than <input type="checkbox"/> %					
		Measurement Position <input type="checkbox"/> SEMI M2 <input type="checkbox"/> SEMI M11 <input type="checkbox"/> Other:					
		Calculation <input type="checkbox"/> SEMI M2 <input type="checkbox"/> SEMI M11 <input type="checkbox"/> Other:					
	10.9	Transition Width Not greater than <input type="checkbox"/> μm					
		Measurement Position					
		Calculation					
	10.10	Flat Zone Not less than <input type="checkbox"/> μm					
		Measurement Position					
		Calculation					
	10.11	Phantom Layer <input type="checkbox"/> None <input type="checkbox"/> Not greater than <input type="checkbox"/> μm					





## SEMI SILICON WAFER SPECIFICATION FORM FOR ORDER ENTRY (Page 5)

## PART 3. EPITAXIAL WAFER WITH BURIED LAYER

CUSTOMER:		PART NUMBER:	REVISION:	DATE:			
R E Q	ITEM	SPECIFICATION	TESTING LEVEL				
			WAFER		TEST PIECE		
			100%	SAMPLE	100%	SAMPLE	
15. PHOTOLITHOGRAPHY CHARACTERISTICS							
	15.1	Mask ID	[ ] Number: [ ] [ ] None				
	15.2	Alignment Precision	X max [ ] $\mu$ m, Y max [ ] $\mu$ m, $\Theta$ max [ ] $^{\circ}$ Reference Point (Wafer Coordinate System): x [ ] mm, y [ ] mm				
	15.3	Pattern Line Width Tolerance	Tolerance $\pm$ [ ] $\mu$ m				
16. BURIED LAYER CHARACTERISTICS							
	16.1	Dopant	[ ] B, [ ] Phos, [ ] S, [ ] As				
	16.2	Diffusion Depth (xj)	Nominal [ ] $\pm$ Tolerance [ ] $\mu$ m				
	16.3	Sheet Resistance	Nominal [ ] $\pm$ Tolerance [ ] $\Omega$				
	16.4	Pattern Step Height	Nominal [ ] $\pm$ Tolerance [ ] nm				
	16.5	Defect Density (Before Epi)	Not greater than [ ] /cm <sup>2</sup>				
17. BURIED LAYER PATTERN CHARACTERISTICS AFTER EPI							
	17.1	Pattern Shift Ratio	Nominal [ ] $\pm$ Tolerance [ ]				
	17.2	Pattern Distortion Ratio	Max. [ ]				
18. OTHER CHARACTERISTICS							

<sup>1</sup> Individual value is not required if wafer is specified according to SEMI M1. \_\_\_\_.<sup>2</sup> Flatness Acronyms are determined from the Flatness Decision Tree in SEMI M1, Appendix A1.<sup>3</sup> Individual value is not required if wafer is specified according to SEMI M1, Table 1.<sup>4</sup> Individual value is not required if wafer is specified according to Table I of SEMI M2 or SEMI M11.





**Table 1**  
**Industry Standard References**

**POLISHED WAFER**

ITEM	VALUE		STANDARD REFERENCE <sup>A</sup>		STANDARD TEST METHODS			
	IS IN SEMI	IS REQ'D <sup>B</sup>	SEMI	JEIDA	ASTM	JIS	JEIDA	DIN
<b>1. GENERAL CHARACTERISTICS</b>								
1.1	Growth Method	NO	YES	M1 Note 5				
1.2	Crystal Orientation	NO	YES			F 26	18	50433
1.3	Conductivity Type	NO	YES	M1 Note 5		F 42	H 607	50432
1.4	Dopant	NO	YES	M1 Note 5				50438/3
1.5	Nominal Edge Exclusion Distance for Fixed Quality Area	NO	NO	M1 Fig 1				
<b>2. ELECTRICAL CHARACTERISTICS</b>								
2.1	Resistivity	NO	YES	M1 Sec 9		F 84, F 673	H 612 18	50431
2.2	Radial Resistivity Variation (RRG)	NO	NO	M1 Sec 9		F 81	18	50435
2.3	Resistivity Striations	NO	NO			F 154, F 525		
2.4	Minority Carrier Lifetime	NO	NO			F 28, F 391, F 1388	H 604	50440/1
<b>3. CHEMICAL CHARACTERISTICS</b>								
3.1	Oxygen Concentration	NO	NO			F 120, F 1188, F 1189, F 1366		50438/1
3.2	Radial Oxygen Variation	NO	NO			F 951		
3.3	Carbon Concentration	NO	NO			F 120, F 1391		50438/2
3.4	Metallic Content	NO	NO					
3.5	Surface Organics	NO	NO					
<b>4. STRUCTURAL CHARACTERISTICS</b>								
4.1	Dislocation Etch Pit Density	NO	NO			F 47	H 609	50434
4.2	Slip	NO	NO			F 47, F 416	H 609	50434
4.3	Lineage	NO	NO			F 47	H 609	50434
4.4	Twin	NO	NO			F 47	H 609	50434
4.5	Swirl	NO	NO			F 416	H 614 24	
4.6	Shallow Pits	NO	NO			F 416, F 1049	H 614 24	
4.7	Oxidation Induced Stacking Faults (OSF)	NO	NO			F 416		
4.8	Oxide Precipitates (BMD) Interstitial Oxygen Reduction ( $\Delta O_i$ )	NO NO	NO NO			F1239		
<b>5. WAFER PREPARATION CHARACTERISTICS</b>								
5.1	Wafer ID Marking	YES	NO	M12, M13				
5.2	Front Surface Thin Film(s) Applied	NO	NO					
5.3	Denuded Zone	NO	NO					
5.4	Extrinsic Gettering Treatment	NO	NO					
5.5	Backseal	NO	NO					
5.6	Annealing	NO	NO					
<b>6. MECHANICAL CHARACTERISTICS</b>								
6.1	Diameter	YES	YES <sup>C</sup>	M1 Sec 9	27	F 613		50441/4
6.2	Primary Flat Length/Diameter Notch Dimensions	YES	YES <sup>C</sup>	M1	27	F 671, F 1152		50441/4
6.3	Primary Flat/Notch Orientation	YES	YES <sup>C</sup>	M1 Sec 9	27	F 847		
6.4	Secondary Flat Length	YES	YES <sup>C</sup>	M1 Sec 9		F 671		50441/4
6.5	Secondary Flat Location	YES	YES <sup>C</sup>	M1 Sec 9		F 847		
6.6	Edge Profile	YES	YES <sup>C</sup>	M1 Sec 5		F 928		50441/2
6.7	Thickness	YES	YES <sup>C</sup>	M1 Sec 9	27	F 533	H 611	50441/1
6.8	Thickness Variation (TTV)	YES	NO	M1 Sec 9	27	F 533, F 657	H 611	50441/1
6.9	Surface Orientation	YES	YES	M1 Sec 9	27	F 26	18	50433
6.10	Bow	YES	NO	M1 Sec 9		F 534	H 611	
6.11	Warp	YES	NO	M1 Sec 9		F 657, F 1390		
6.12	Sori	NO	NO	M1 Sec 9				
6.13	Flatness	NO	NO	M1 Sec 9		F 775	DEF43	50441/3



**Table 1 (cont'd)**  
**Industry Standard References**

**POLISHED WAFER**

ITEM		VALUE		STANDARD REFERENCE <sup>A</sup>		STANDARD TEST METHODS			
		IS IN SEMI	IS REQ'D <sup>B</sup>	SEMI	JEIDA	ASTM	JIS	JEIDA	DIN
<b>7. FRONT SURFACE VISUAL INSPECTION CHARACTERISTICS<sup>D</sup></b>									
7.1	Scratches	YES	NO	M1 Table 1	26	F 523	H 614		
7.2	Pits	YES	NO	M1 Table 1	26	F 523	H 614	24	
7.3	Haze	YES	NO	M1 Table 1	26	F 523	H 614	24	
7.4	Light Scattering Defects (Particulate Contamination)	YES	NO	M1 Table 1	26	F 523	H 614	24	
7.5	Contamination/Area	YES	NO	M1 Table 1	26	F 523	H 614	24	
7.6	Edge Chips	YES	NO	M1 Table 1	26	F 523	H 614	24	
7.7	Edge Cracks	YES	NO	M1 Table 1	26	F 523	H 614	24	
7.8	Cracks, Crow's Feet	YES	NO	M1 Table 1	26	F 523	H 614	24	
7.9	Craters	YES	NO	M1 Table 1	26	F 523	H 614	24	
7.10	Dimples	YES	NO	M1 Table 1	26	F 523	H 614	24	
7.11	Grooves	YES	NO	M1 Table 1	26	F 523	H 614	24	
7.12	Mounds	YES	NO	M1 Table 1	26	F 523	H 614	24	
7.13	Orange Peel	YES	NO	M1 Table 1	26	F 523	H 614	24	
7.14	Saw Marks	YES	NO	M1 Table 1	26	F 523	H 614	24	
7.15	Dopant Striation Rings	NO	NO		26	F 523	H 614	24	
7.16	Stains	NO	NO		26	F 523	H 614	24	
<b>8. BACK SURFACE VISUAL INSPECTION CHARACTERISTICS</b>									
8.1	Edge Chips	YES	NO	M1 Table 1		F 523			
8.2	Cracks, Crow's Feet	YES	NO	M1 Table 1		F 523			
8.3	Contamination/Area	YES	NO	M1 Table 1		F 523			
8.4	Saw Marks	YES	NO	M1 Table 1		F 523			
8.5	Stains	NO	NO						
8.6	Roughness	NO	NO						
8.7	Brightness	NO	NO						
<b>9. OTHER CHARACTERISTICS</b>									

**EPITAXIAL WAFER**

ITEM		VALUE			STANDARD REFERENCE <sup>A</sup>			STANDARD TEST METHODS			
		IS IN M2	IS IN M11	IS REQ'D <sup>B</sup>	SEMI M2	SEMI M11	JEIDA	ASTM	JIS	JEIDA	DIN
<b>10. GENERAL EPITAXIAL LAYER CHARACTERISTICS</b>											
10.1	Conductivity Type/structure	NO	NO	YES	Sec 3	Sec 3					
10.2	Dopant	NO	NO	YES	Sec 3	Sec 3					
10.3	Silicon Source Gas	NO	NO	NO	Sec 3	Sec 3					
10.4	Growth Method	NO	NO	NO	Sec 3	Sec 3					
10.5	Net Carrier Density (Resistivity)	NO	NO	YES	Sec 3	Sec 3		F 1392, F 1393 (F 374, F 398, F 525, F 723)			50438 (50444)
10.6	Net Carrier Density Variation (Resistivity Variation)	YES	NO	YES	Sec 3, 5	Sec 3, 5					
10.7	Thickness	NO	NO	YES	Sec 3	Sec 3		F 95, F 110			50437
10.8	Thickness Variation	YES	NO	YES	Sec 3, 5	Sec 3, 5					
10.9	Transition Width	NO	NO	NO							
10.10	Flat Zone	NO	NO	NO							
10.11	Phantom Layer	NO	NO	NO							

**Table 1 (cont'd)**  
**Industry Standard References**

## EPI TAXIAL WAFER

[illegible]

<sup>A</sup> Item is defined or described and/or a test procedure applicable to the item is included in the cited reference.

<sup>B</sup> Value is/is not required to minimally specify a wafer.

<sup>C</sup> Individual value is not required if wafer is specified according to SEMI M1.

<sup>D</sup>In today's technology, it is possible to inspect for some of these items using automated laser scanning systems; however, a standard test procedure has yet to be developed. Application of automated inspection must be agreed upon between supplier and user.

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