Improving Silicon Solar Cell Efficiency Through Advanced Cell Processing, Highly Uniform Texturing, and Thinner Cells

Cooperative Research and Development Final Report

CRADA Number: CRD-15-585

NREL Technical Contacts: Bhushan Sopori and Dan Friedman

NREL is a national laboratory of the U.S. Department of Energy
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Cooperative Research and Development Final Report

Report Date: 12-21-18

In accordance with requirements set forth in the terms of the CRADA agreement, this document is the final CRADA report, including a list of subject inventions, to be forwarded to the DOE Office of Science and Technical Information as part of the commitment to the public to demonstrate results of federally funded research.

Parties to the Agreement: The University of Central Florida Board of Trustees

CRADA Number: CRD-15-585

CRADA Title: Improving Silicon Solar Cell Efficiency Through Advanced Cell Processing, Highly Uniform Texturing, and Thinner Cells

Joint Work Statement Funding Table showing DOE commitment:

Estimated Costs	NREL Shared Resources a/k/a Government In-Kind
Year 1	$ .00
TOTALS	$ 00.00

Abstract of CRADA Work:

This CRADA is aimed at developing silicon solar cell technologies that can yield higher efficiency solar cells. Specifically, this CRADA cover three technologies: (i) developing a high temperature process for dissolution of oxygen precipitates, (ii) uniform texturization of diamond wire sawn wafers, and (iii) evaluation of techniques to bond techniques thin wafers and thin films.

Summary of Research Results:

This project successfully demonstrated that flash annealing can be highly effective in mitigating the presence of oxygen precipitates in silicon wafers, thus facilitating cost reductions by the use of less expensive wafers. The project also successfully determined the optimal amount of saw damage removal in diamond wire sawn wafers, again facilitating lower-cost high-efficiency silicon solar cells. The techniques of flash-annealing and diamond wire wafering are thus both shown to be highly effective.

2.0 Proof of Concept Solar Cell Fabrication Using Temp Bonding

No data to report—project terminated early due to DOE stop-work order.

4.0 Dissolution of Oxygen Precipitate-nuclei for Making High-efficiency Solar Cells on Thin, Low-cost, N-type, CZ-Si Substrates

Flash annealing to dissolve oxygen precipitate nuclei

INTRODUCTION

It is now well recognized that monocrystalline, CZ-grown (traditional or continuous growth) wafers are highly suitable substrates for low cost, high efficiency (> 20%) solar cells. This potential as been amply demonstrated at a commercial level on N-type substrates, yielding cell efficiencies close to 25%. Clearly, such high efficiency devices require high-quality wafers. Silicon ingot growers have made this possible by using very high quality poly feedstock and maintaining cleanliness of the crystal growth equipment, which enables growth of low-Fe and low C-Si ingots. As a result, currently N-type (P-doped), CZ-Si wafers are available with long (few milliseconds) minority carrier lifetime (MCLT) in the as-grown state. These improvements in the crystal growth technology have also helped P-type wafer technology, yielding high quality P-type wafers. Despite these improvements, there are many issues with both N-based and P-based solar cells fabricated on CZ-Si. One of these issues is that material quality varies over the ingot length. Consequently, wafers near the seed end of the ingot are more suitable compared to those near the tang end. Interestingly, these issues are primarily related to O defects produced by either during solar cell processing or during the operation of the cell operation itself.

The behavior of O in Si has been studied for decades and there is a wealth of literature available. However, nearly all previous work is related to microelectronic devices aimed at understanding internal gettering, oxygen precipitation by conventional thermal anneals, and study of oxygen defects. While the fundamental characteristics of O in Si remain the same, the issues that affect solar cell fabrication and device performance are somewhat different and are only beginning to emerge. For example, some recently discovered problems, which may be related to O, are: degradation of MCLT in n-type wafers upon B diffusion, light induced degradation in B-doped wafers and solar cells, and oxygen precipitation in N-type wafers. This project primarily addresses oxygen-related issues with N-type, CZ silicon and is aimed at development of a process (flash annealing), to mitigate the O-related effects so that very high efficiency (> 20%) devices can be fabricated on CZ wafers.

Oxygen related issues for solar cells

Dissolved interstitial O in Si is known to be optically active and electronically inactive. Hence, typically, dissolved O has little or no effect on wafer MCLT or on the solar cell characteristics. For example, it is possible to make high efficiency devices on wafers with moderate O concentration (mid 10^{17} cm^{-3}). However, above these levels, O can interact and form a variety of defects either during the crystal growth itself or during solar cell fabrication. But, some of these interactions are known to be pertinent to solar cell performance. These interactions can be viewed as: oxygen can interact with itself (e.g., to form oxygen dimers, donor states), can associate with other impurities (B-O pairs), and interactions with other point defects to form oxygen precipitates.

Oxygen precipitation

It is well known that oxygen precipitation can have a strong influence on the minority carrier recombination. Yet, until recently, very little attention was paid to O precipitation in solar cells (although known for a long time). Main reason was that majority of Si solar cells were fabricated on P-type, B-doped wafers, requiring P diffusions to make N/P solar cells. Typical junction formation with P diffusion uses relatively lower temperatures, below 850 °C, and for short periods (15 -30 min). Another high temperature process step may be contact alloying (and BSF formation). This is generally a short process (few seconds) and around 850 °C. Hence, both these processes are unlikely to produce any O precipitation in most of the wafers that typically have lower O (and C) concentrations. However, it has been found that some of the wafers, especially from tang end, can have pre-existence of swirl pattern caused by presence of large nuclei of oxygen. This is true for both P- and N-type ingots/wafer. As an example, Figure 1 shows a MCLT map of a 156 mm x 156 mm, P-type wafer using Semilab tool and the measurement was done with iodine-ethanol passivation. Also shown in the figure is the MCLT measured in one of the regions by Sinton tool. This local measurement was made immediately after I-E passivation and represents the correct value of the actual effective MCLT. Because mapping takes about 30 minutes and that I-E passivation degrades rapidly, it is necessary to allow passivation to stabilize (while there is a reduction in the surface passivation) for a short time (typically about 15 min) during which the passivation is stabilized but its quality is reduced (surface recombination increases). This procedure will be followed for the entire report. Because the behavior of O during crystal growth is similar in both P- and N-type ingots, similar pattern can also be expected in some N-type wafers (shown later in Fig. 4).

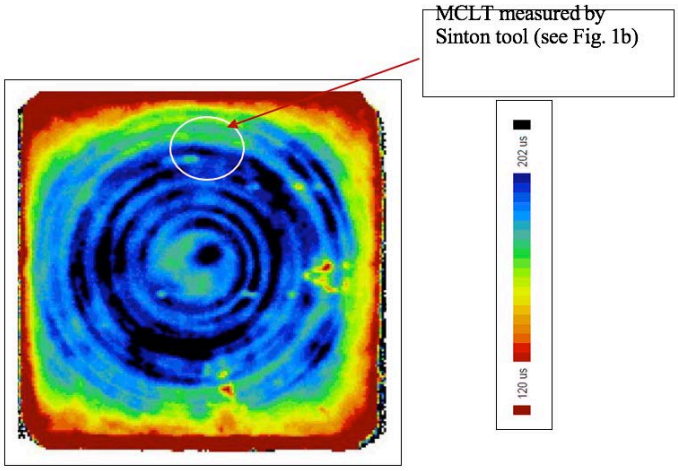

Fig. 1a. Minority carrier lifetime map of a P-type wafer grown by CZ showing oxygen- related swirl pattern caused by oxygen precipitate nuclei.

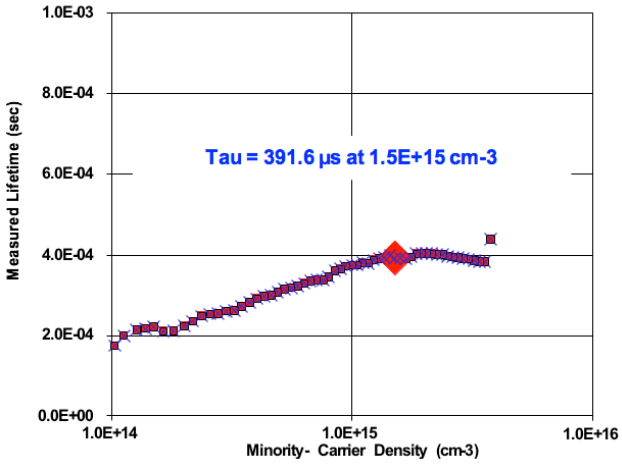

Fig. 1b. Injection level dependence of MCLT in the region labelled in Fig. 1a.

Oxygen precipitation in N-type Si wafers can be more problematic, particularly during solar cell fabrication. N-type Si offers a very big advantage for solar cell applications because MCLT in N-type Si is not as sensitive to degradation by Fe as P-type. Furthermore, as mentioned previously, ingot growers can control the TM impurities during crystal growth concomitantly yielding as-grown wafers that can MCLT in the range of few milliseconds. But there remain two major problems that still need to be solved before N-type wafers can be commercially used (without a preselection of wafers) by majority of solar companies. These problems are: (i) A Czochralski (CZ) grown ingot shows a large variation in the material quality of wafers taken along the axial direction (also discussed further in this paper). Consequently, only a limited fraction of wafers can be used for very high efficiency cell fabrication, reducing the yield (number of useable wafers per ingot length) of the ingot.

Task 4.1: Wafer acquisition and their characterization

Wafers for this project were acquired from GTAT (GT Advanced Technologies). Wafers were chosen from two ingots - ingot A and B, with some specific properties. Wafers were diamond wire sawn with nominal thickness of 190 □m. The surface damage was removed by etching in HNO_3:HF:CH_3COOH::1:1:5 solution, as described in previous papers [see bibliography]. This etch is basically an isotropic etch but has some sensitivity to damage. Typically, 6 to 8 □m were removed from each surface, resulting in wafers of about 172 □m thick. Consequently, the resultant wafer surfaces remain rather rough. Groups of wafers (G1 to G4) were taken from 4 different locations as illustrated in Fig. 2. Oxygen and carbon concentrations, and MCLT of the ingots were measured. Figure 3 shows measured C, O (dissolved), and MCLT variation along specific location over the axial length of the ingot using an ingot measurement tool. It is seen that there are significant variations in these parameters within the ingot as well as between the two ingots.

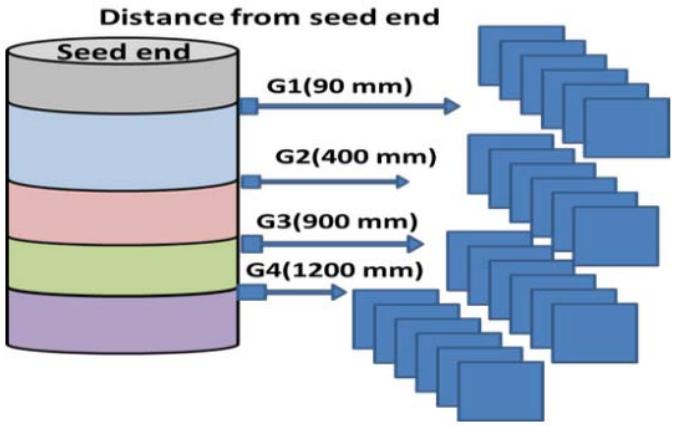

Fig. 2. Sketch illustrating the wafers used from different locations of ingots.

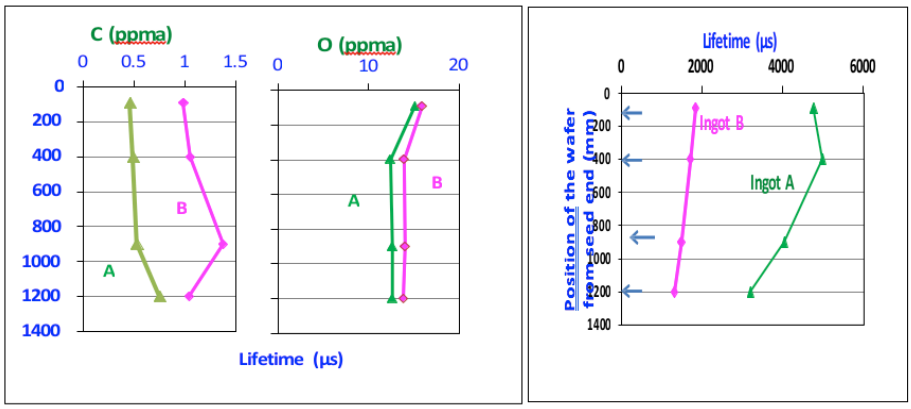

Fig. 3. Axial distribution of C, O, and MCLT along the two ingots used in the study.

As seen, ingot A has lower C and O concentrations and higher MCLT over the entire ingot. This feature allows us to compare the effect of FA on slightly different material quality.

Representative wafers from each group were also characterized by MCLT mapping, injection-dependent lifetime measurement, and O/C measurements (in some cases before and after flash annealing). It is important to point out two significant aspects of n-type, CZ Si wafers:

a. Existence of swirl pattern in high O and high C wafers (such as tang end of ingot B). These patterns, observed on wafers by MCLT and photoluminescence mapping are shown in Figures 4a and 4b, respectively. It is seen that the effective MCLT is quite low. NREL has determined that these swirl patterns are due to presence of oxygen precipitate nuclei and are precursors to formation of large oxygen precipitates during solar cell processing, resulting in further degradation in the material quality.

b. It is a common experience that many N-type wafers, particularly those with moderate-to-high O and C content, develop swirl defects during cell fabrication, with a concomitant degradation in MCLT. Typically, the MCLT can reduce from several milliseconds to few hundred micro-seconds, thus severely limiting the cell efficiency. Interestingly, both problems happen to have the same origin—they both are related to presence of oxygen precipitate-nuclei (OPN) in the wafers.

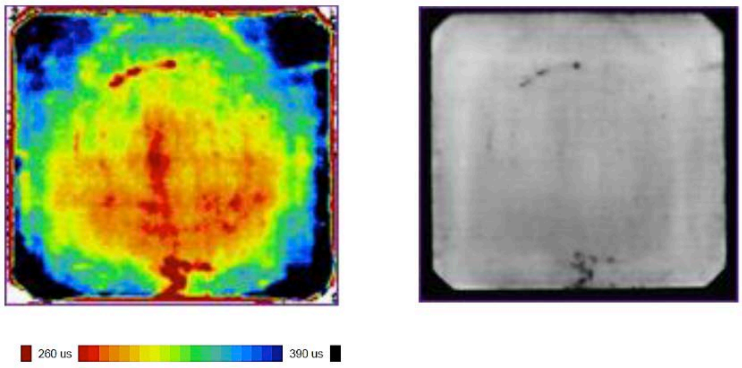

Fig. 4. MCLT map (a) and PL map (b) of a tang end wafer from ingot A showing presence of swirl defects due to OPNs.

It has been reported that the MCLT of many n-type wafers can degrade during solar cell processing. It has been recently shown that this degradation occurs because of formation of oxygen related defects. For example, a typical B diffusion, consisting of a pre-deposition and drive-in, for making p/n junction results in formation of stacking faults. Figure 5 shows etch pits corresponding to SFs delineated by Sopori etch on the surface and cross section of a (100) wafer by a B diffusion and oxidation (drive-in) done at 1050 °C for 60 minutes. NREL observed that extended processing can result in formation of typical swirl defects, as shown in Figure 5.

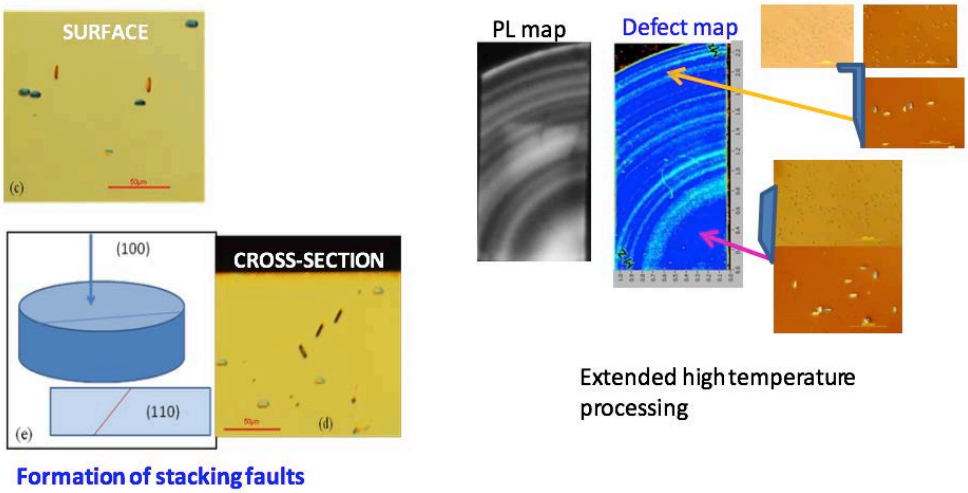

Fig. 5. Defect generation due to B diffusion - (left) stacking faults on the wafer surface and cross section, and (right) swirl defects formed upon extended diffusion + oxidation.

It is important to point out n-type wafer processing predisposes to oxygen precipitation during B diffusion. This is because B diffusion is typically done in a temperature range of 1000 -1100 °C (for example in BBr3), during which B forms an alloy with Si. This boron rich layer (BRL) consumes Si as it grows at the surface. This process is similar to oxidation, where some of Si atoms are injected back into the wafer as interstitials. Thus, like oxidation-induced SFs, B diffusion can enhance formation of SFs and formation of swirl defects. This layer also creates surface stress and is responsible for formation of dislocations at the wafer surface with additional degradation of MCLT. These mechanisms are illustrated in figure 6.

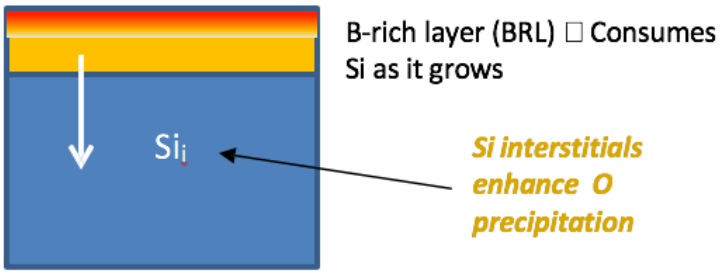

Fig. 6. Illustration of the proposed mechanism of Si interstitial injection during B diffusion.

Oxygen precipitation is a serious problem that degrades wafer quality and limits the achievable cell efficiency. One solution might be to select wafers from near-seed end of the ingot. This, however, will greatly lower the ingot yield (number of useable wafers from an ingot). Fortunately, there is a solution based on a simple concept that is very well known—pre-processing wafers to dissolve the precipitate nuclei before solar cell fabrication. Oxygen precipitate nuclei are agglomerates/embryos, typically 50- 100 Å in radius, that are formed by interaction of point defects and impurities like O and C during crystal growth, when the ingot is in the temperature range of 800 °C – 1000 °C. These embryos can be dissolved at temperatures of 1100 -1300 °C within very short periods of time. Although this solution is conceptually simple, there are numerous hurdles to apply a very high temperature process step to high quality wafers and that a commercially compatible process for OPN dissolution is not yet available.

Task 4.2, Optimization of FA process for N-type wafers

A flash annealing process has been created, which uses NREL-developed optical cavity furnace (OCF) to isothermally heat a wafer by controlling the optical flux. These furnaces are inherently "clean" and take advantage of two mechanisms: (i) thermophoresis - a process where impurities are driven from a "hot" wafer to "cold" environment. For example, when a wafer is at 1200 °C the walls of the quartz liner are at < 200 °C; and (ii) photopheresis—whereby photons that impinge on the wafer remove submicron particle through a momentum transfer process. Because of these, the OCF are highly clean and do not require HCl treatments prior to wafer processing. Researchers are able to process 30 ms wafers and maintain that MCLT though the process.

Process conditions

Nucleation and growth theory suggest that OPN can be dissolved at high temperatures where the nuclei size is below the critical size. Hence, if a wafer is heated to a high temperature, the OPNs will shrink and dissolve. If it is assumed that the size of the largest OPNs is □ 100 Å, the required process temperature can be estimated to be in the range of 1150 °C to 1250 °C. Another important parameter is time needed to dissolve OPNs. Because dissolution time depends on the precipitate size, temperature, and the difference between oxygen concentration in the wafer and the equilibrium solubility at temperature T, an optimum time can be difficult to predict. However, it is known that larger size precipitates can be dissolved in thermally pretreated samples using so called "low-high" treatment, by heating to 1200 °C for short periods of time. NREL has completed some detailed experiments and selected two process conditions, which will be illustrated in the next section. For the present, it will be assumed that OPNs can be dissolved with process times that can be quite short (□ 2 to 3 minutes).

The process times can be further reduced by simulating conditions for injecting Si interstitials, which favor the reverse reaction based on increased volume upon oxidation, resulting in kick-out of Si interstitials (Isi): Si + 2Oi □ SiO2 + Isi. This reaction suggests dissolution process will be favored in oxygen ambient, which injects interstitials from the surface. Because annealing must be done at a very high temperature, there are stringent requirements for cleanliness and temperature uniformity. The furnace cleanliness must be compatible with processing wafers of several millisecond MCLT. Likewise, a high degree of temperature uniformity is needed to prevent any defect generation (and, in an extreme case prevent wafer shattering).

Each group of wafers was Flash Annealed under two slightly different process conditions (Process A & Process B). A typical optical flux profile of a FA process is shown in Fig. 7. This process involves two segments - Segment 1 that raises the optical flux linearly to a level □□ and holds it during time t_1 to t_2. And segment 2 that raises the optical flux abruptly to a level □□ and holds it during time t_1 to t_2. The corresponding temperature profiles are also illustrated in Fig. 7. The entire process takes less than 2 minutes. Process B has a 2nd segment, (t_2 - t_3), 5s longer while all other parameters are same. The entire process is done with oxygen gas ambient. Although our optical furnaces have TLC capability, there was no HCl type of cleaning used in this furnace. This is simply to show that our process is commercially compatible and low cost.

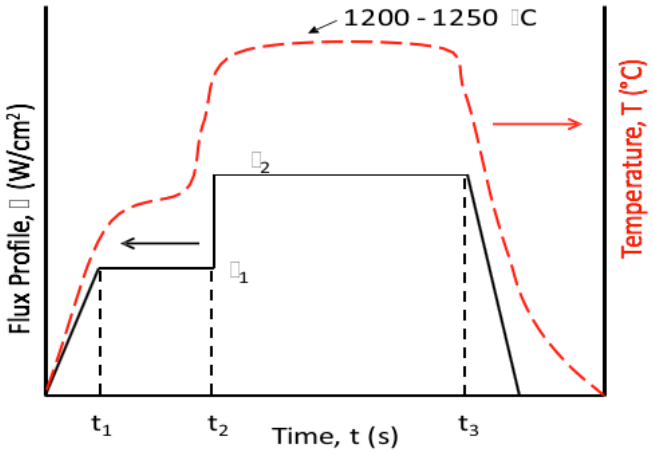

Fig. 7. Illustration of typical flux and temperature profiles used in our OPF during a FA process. Note: Segment (t_2 - t_3) for process B is 5s longer than process A.

Effect of ambient during FA

As pointed out in the previous section, O2 ambient can provide Si interstitial injection that favors precipitate dissolution. Oxidizing ambient is also favored for protecting wafers from degradation. Figure 8 shows injection level dependence of MCLT of three adjacent wafers annealed in O, Ar, and N gas flow. The starting MCLT of the wafers was □1ms. It is seen that O2 flow maintains the wafer quality.

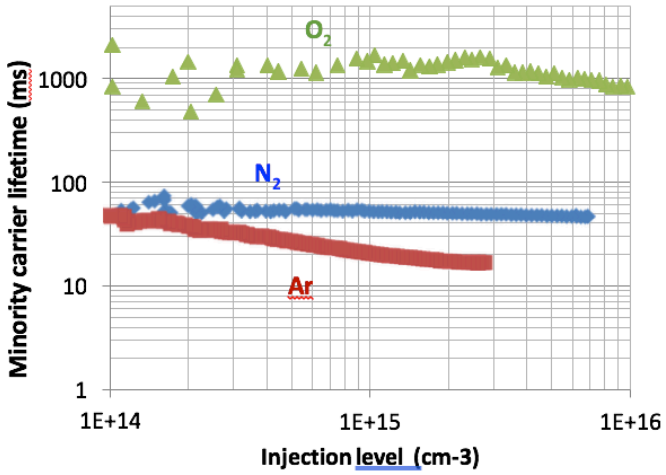

Fig 8. Injection level dependence of MCLT of three adjacent wafers processed in different ambient gases. (starting MCLT of the wafers □1 ms)

Figure 9 compares MCLT maps of three sequential wafers (156 mm x 156 mm). The wafer on the left, B-G3-1, is unprocessed and displays a swirl pattern of OPN. The color legend shows the highest MCLT to be 320 □s. Also shown on the top (region marked by white circle) is the maximum value of MCLT measured by Sinton's wafer-lifetime tool (WCT-100), which is also 320 □s. Figure 9 also shows MCLT maps of two FA'd wafers. The middle wafer was annealed with process A, while wafer on the right was annealed with process B. This clearly shows that process B is an optimum process.

An important feature can be clearly seen in both processed wafers—the swirl pattern has been eliminated by FA. Furthermore, for the middle wafer (process A), the maximum value in the MCLT map has increased to 1 ms, while the maximum MCLT at the top of the wafer with Sinton tool is now 1.1 ms. For the wafer on the right-hand side (process B), the MCLT map shows further increase to a maximum value of 1.6 ms, while Sinton tool shows increase to 3.2 ms. These results clearly show precipitate dissolution and its dependence on the process time.

It should be noted that the MCLT of FA wafers from ingot B have increased above the ingot values (as seen in Fig. 3) and are approaching that of ingot A. The thickness of all the wafers shown in Fig. 9 is about the same (□155 □m). However, their surfaces are quite rough, giving rather large $S_{eff,}$ which is estimated to be in 5-7 cm/s range.

Let us look at the effect of FA on the MCLT plot (injection level dependence). Figure 10 shows these plots for 3 wafers from group A-G2. Wafer # A-G2-68 is unannealed; A-G2-70 is annealed with profile A, while A-G2-69 is annealed with process B. Two important observations from Fig. 10 are: (i) The maximum lifetime increases from about 700 □s for unprocessed wafer to 3 ms for process A and 3.2 ms for process B (before Auger recombination takes over); (ii) The MCLT of A-G2-68 increases with injection level (up to 2 x 10^{15} cm^{-3}). On the other hand, the plots for annealed wafers are near ideal and do not show low-level injection dependence. Because it is not expected for the Fe concentration to change during FA, this implies that the injection level dependence of unprocessed wafer is related to the recombination associated with OPN

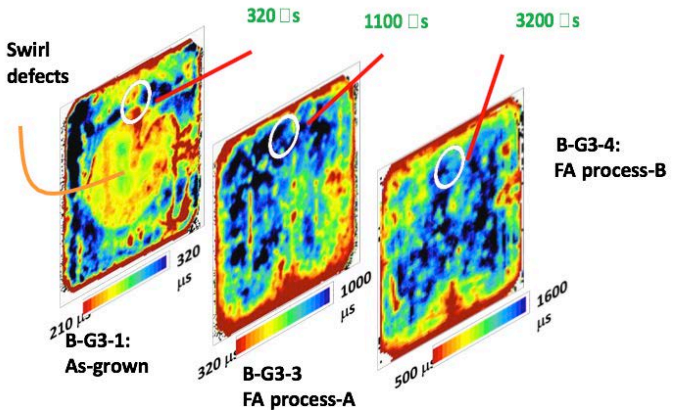

Figure 9. MCLT maps of (left) unprocessed, (middle) shorter flash annealed, and (right) longer flash annealed sequential wafers.

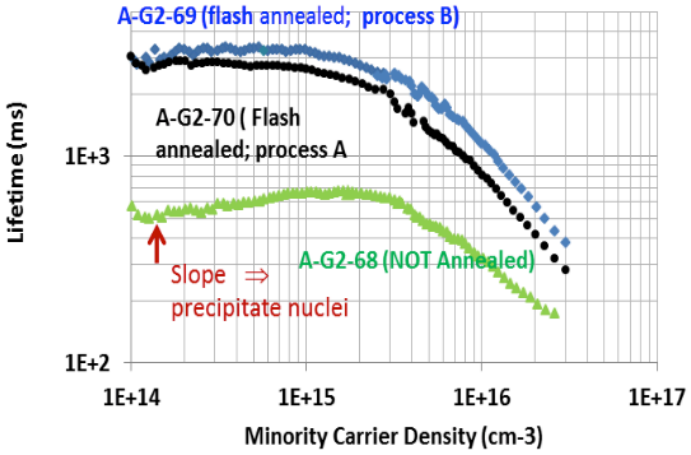

Figure 10. Comparison of results of two FA processes, A and B, on wafers from ingot A. For reference, the lifetime plot of unannealed wafer is also shown.

Now it is considered that MCLT plots of higher quality ingot A, before and after FA. Figure 11 compares MCLT vs injection level of wafers A-G1-1(unannealed) and A-G1-37 (FA). These wafers were not of the same thickness. AG1-1 was only 100 □m in thickness while AG-1-37 was 160 □m thick. Keeping this in mind, it is clear that FA does not affect MCLT to any significant level. It is worthwhile noting that A-G1-1 does display some injection level dependence indicating presence of some OPNs.

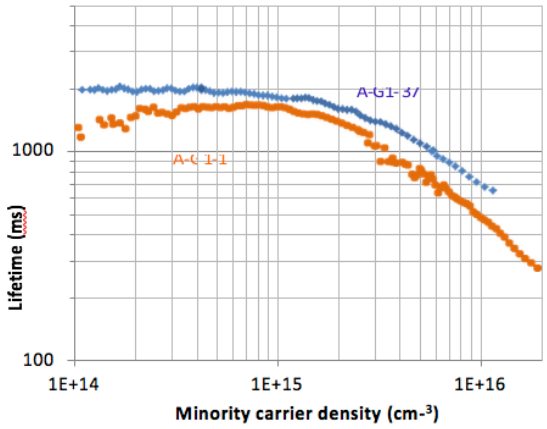

Fig. 11. Comparison of FA and unannealed wafers from ingot A. The MCLT remains almost unchanged by FA.

To further support the argument that the injection level dependence of unannealed wafer comes from OPNs, it has been modeled unprocessed wafer lifetime using two-trap model (Fei and OPN), using the following well-known relationship:

$$1/\tau_{eff} = 1/\tau_{SRHO} + 1/\tau_{Fe} + 1/\tau_{SR} + 1/\tau_{Aug}$$

where □Fe,□SRHO,□SR and, □Aug correspond to lifetimes associated with Fe, OPN, surface recombination, Auger, respectively. Standard formulas were used and data from literature for energy levels and capture cross sections of Fe, and Auger coefficients, and a surface recombination value for I-E passivated Si wafer surface as 7 cm/s, which was determined from known bulk lifetime of the wafers (as measured on the ingot). This fit yields the following values: OPN trap level, $E_t = E_c - 0.2$ eV with electron capture coefficient of 10^{-19} cm^2; Fei concentration of $1.6x10^{11}$ cm^{-3}, and the OPN density of 2×10^{13} cm^{-3}.

OPN density can now be checked to confirm it is reasonable. To do that, it needs to be determined if the increase in the dissolved O concentration due to FA. Figure 12 shows FTIR transmission spectrum corresponding to O peaks (1107 cm^{-1}) before and after FA. From these data and using the new ASTM (ASTMF121-83) published calibration coefficient of $2.45 X10^{17}$ cm^{-2}, the calculated increase in O concentration was determined to be 2.9×10^{17} cm^{-3}. The measured increase in dissolved O concentration can now be used to verify if the OPN density (N_{OPN}) is appropriate. To complete, this expression is used:

$$[4/3 \cdot \pi r_0^3] \cdot C_p \cdot N_{OPN} = [O_i]_i - [O_i]_f$$

where, r_0 = average radius of OPN, C_p = atomic density of oxygen in OPN = 4.5×10^{22} cm^{-3}, N_{OPN}

= average OPN density. Here it is assumed OPNs to be spherical SiO_2 particles of 100Å in diameter. This expression yields $N_{OPN} = 2x10^{13}$ cm^{-3}. It should be noted that no attempts have been made to consider effects of SiO_2 being under compression in the Si lattice.

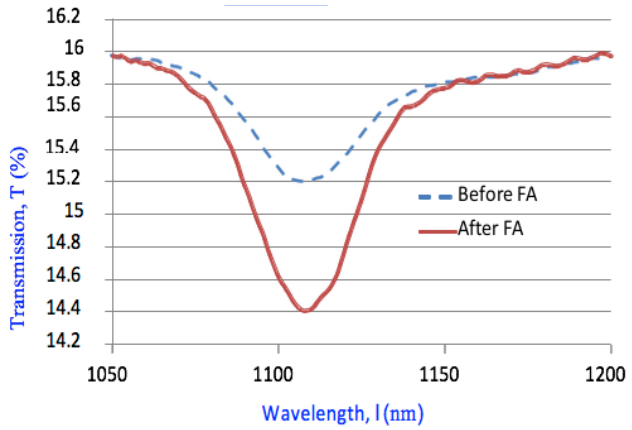

Fig 12. O (before FA) = 6.6 x 10^{17} cm^{-3}, O (after FA) = 9.52 x 10^{17} cm^{-3} Increase in dissolved O = 2.9 x 10^{17} cm^{-3}

NOPN can now be used to estimate density of traps associated with the trap level E_t. The traps are assumed to be like those at the Si-SiO2 interface (without H annealing). To determine the trap density, calculate the total Si- SiO2 area of each OPN of 50 Å in radius to be □ 3x10^{-12} cm^2. Using typical trap density in the range of 5 x 10^{11} cm^{-2} to 10^{12} cm^{-2}, trap density associated with NOPN is in the range of 2x 10^{13} – 6 x10^{13} cm^{-2}. It is believed that these qualitative agreements (within order of magnitude) are quite sufficient to show validity of the recombination mechanism due to OPNs

Task 4.4: Preparing wafers for solar cell fabrication/cell characterization

To date, NREL has prepared two sets of N-type wafers for solar cell fabrication. The first set consisted of n-type wafers, textured at GaTech. These wafers were split into two groups—one group was flash annealed and the other remained unannealed. Both sets were then sent to GaTech for cell fabrication. It was planned to take out test wafers after completion of B and P diffusion because these are critical steps that will readily show a comparison between unannealed and annealed wafer quality (without finishing the cell processing). Unfortunately, the test wafers showed no difference in the wafer quality between annealed and unannealed wafers. In most cases, the unannealed wafers improved but annealed wafers degraded. At this point, the cell fabrication on rest of the wafers was halted. Further analyses of diffused wafers showed that wafers were contaminated during the texturing step. Identifying and solving the contamination during texturing was reported in task #7. It was established that wafers need to be precleaned in HCl at room temperature before texture etching.

A new set of wafers was recently prepared where damage removal was done at NREL using acid etching. This set of wafers was split into two groups—one group was flash annealed and the other remained unannealed. The entire set will now go through GIT cell fabrication (including texturing). Figure 13 compares MCLT maps of two adjacent wafers —one unannealed and the other FA'd. As expected, the FA wafer shows MCLT □ 3 times that of unannealed.

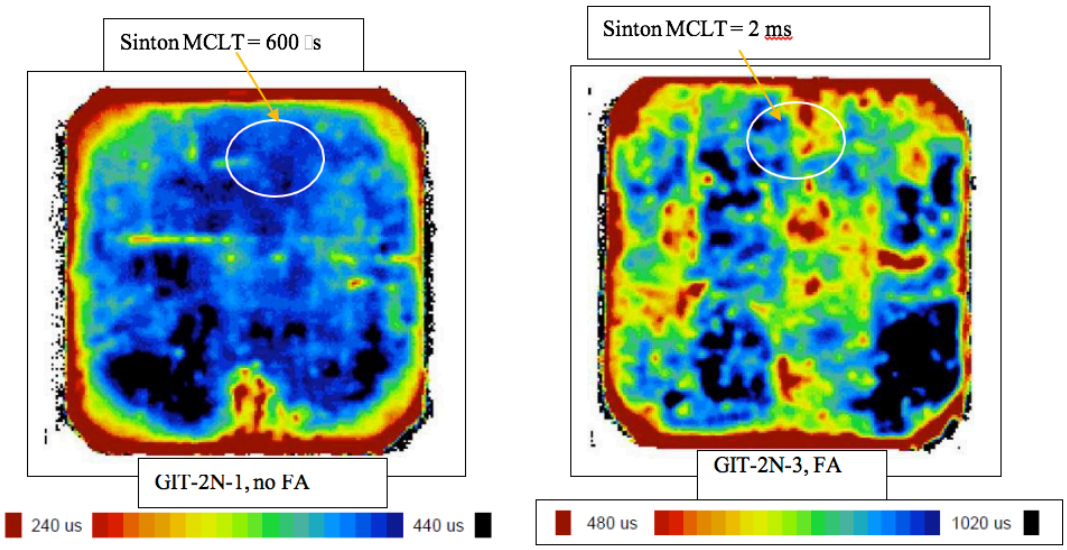

Fig. 13. Typical MCLT maps of unannealed (left) and flash annealed sequential wafers

Discussion/Conclusions

It has been demonstrated that flash annealing can be performed in optical furnaces, without any indiffusion of impurities, and the MCLT can be greatly improved by this step alone. Flash annealing was performed on a large number of wafers from two different ingots (low Fe content). In all cases, the MCLT increased from 300 – 700 □s range to 2 - 3.2 ms range. It was observed that FA resulted in MCLT of wafers from both ingots to become about the same after flash annealing. Researchers discovered the increase in MCLT is caused by OPN dissolution. The MCLT reported here is the effective lifetime on the wafers that have thickness of about 150 □m (and even thinner in some cases). However, the measurements before and after annealing are very accurate and comparable because the wafer thickness and preparation procedure are exactly the same.

NREL researchers identified some of the non-uniformities (as seen in Fig. 9). Many of these are from wafer handling and have been corrected to obtain more uniform lifetime and PL maps after annealing. B and P diffusion on FA wafers have been performed and verified that the improvement in the MCLT is maintained. Cell data are not available at this time.

7.0 Texturing of diamond wire sawed wafers

Texturing issues of diamond wire sawn wafers

Regarding the contamination issue, previous results seemed to point to an important inference that contamination was restricted. However, a deeper diffusion of the surface contamination would occur during higher temperature process of SDR and/or texturing. For example, Fe would diffuse approximately 3 □m into the wafer at 80 °C for 30 min. However, if the contamination from the surface could be removed by subjecting wafers to a cleaning step that would remove metal contamination at low (room) temperature, without allowing them to diffuse in (as would happen during SDR or texturing) because they are typically done at 80-90 °C.

Accordingly, the attempt was made to verify if precleaning wafers (prior to KOH SDR or texturing) in room temperature HCl-based solution would eliminate the contamination problem.

(*It should be noted that because all solar cell processing is developed on slurry cut wafers, other solar cell fabrication may need to be fine-tuned when using DWS wafers.)

The objectives of this work are: (i) Task # 7.3; to determine if the texture uniformity can be improved by performing sufficient SDR etching, which smoothens the surface (by forming large/shallow surface profiles). And (ii) Task # 7.4; To fabricate solar cells on optimally textured wafers and determine the influence of optimal texturing. These tasks require that wafers be pre-cleaned to remove possible contamination from DWS.

EXPERIMENTAL PLAN

To verify the hypotheses, researchers performed the following experiment. Sequential DWS wafers were separated into two groups. One group was cleaned at NREL and the other at Akrion, using methods that were established to remove the wafer contamination. Each group was further split into five sets and each of the five sets was SDR etched to remove different thicknesses. The thicknesses removed in SDR were 2 □m, 4 □m, 6 □m, 8□m, and 10 □m from various groups. All wafers were then texture etched (at Akrion) to have small texture pyramids (about 2 □m in height). NREL examined the wafers for surface striations and contamination. A slurry cut wafers as reference for texturing. A set of textured, N-type wafers were processed into solar cells. This will show some salient results for one set of samples cleaned at NREL.

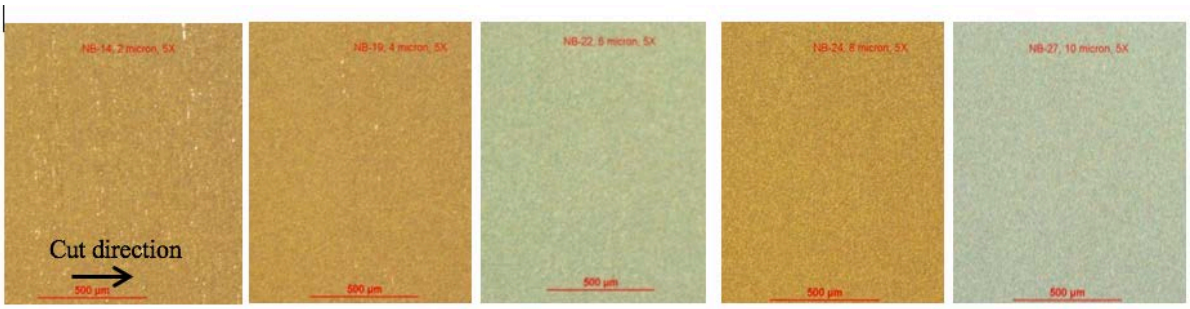

Figure 1. Optical microscope images of surfaces of wafers textured after removing different thicknesses (shown on the phots) during SDR.

Figure 1 shows low magnification images, taken under optical microscope, of textured wafer surfaces of 5 groups of wafers having different SDR removal depth with the same final texture of 2 □m. This shows a systematic decrease in the surface striations (which appears as white speckle) with increasing SDR etch depth from 2 □m to 10 □m and then striations disappear beyond that depth. From this, it can be inferred that SDR "smoothens" the scratches, saw marks, and deep gouges on wafer surface. After etching away 6 □m/side, the surfaces are smooth enough that texture shape is essentially the same all over the wafer. The wafers were also examined under oblique illumination and found that the contrast of reflectance striations followed the same behavior. Figure 2a shows a photograph (with oblique illumination) of wafer that has only 2□m/side removed by SDR and textured. Figure 2b is a microscope image of the striation region. However, the reflectance striations disappear when SDR depth is > 6 □m. It is interesting that damage depth and the SDR etch depth are same when striations disappear.

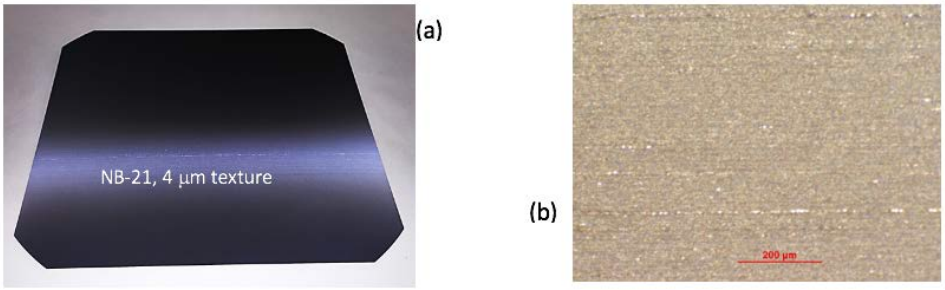

Figure 2. (a) A photograph of a wafer taken with oblique illumination showing deep, abrupt streaks of high reflectance due to localized region of residual damage. (b) Microscope image of the streak showing that it consists of many long abrasion lines during cutting.

NREL also performed MCLT maps of the textured wafers with different SDR etch depth. Figure 3 shows maps of wafers with increasing SDR depth (and final 2 □m texture), corresponding to those shown in Fig. 1. It can be seen that damage lines occur up to SDR depth of 6 □m and beyond that wafers exhibit nonuniformities due to internal structure (such as swirl defects). It was concluded, because the wafers were cleaned to ensure that no contamination was carried into SDR/texturing, there are no contamination bands. It should also be noted that the MCLT increases with SDR depth.

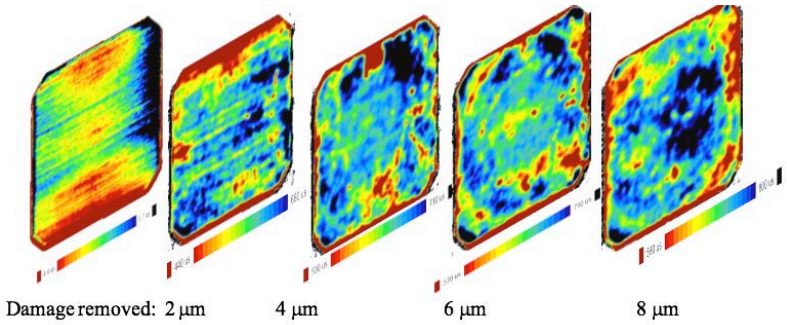

Figure 3. MCLT maps of wafers textured after removing different thicknesses (as shown) by SDR.

Now, details of streaked regions (having higher reflectance) and SEM results showing texture shape can be examined. Earlier it was argued that deep streaks and gouges represent geometries that do not have exact (100) orientation. Because texture shape is orientation dependent, the texture shapes on the walls of these streaks will change, as illustrated in Fig. 4. The argument is based on the following hypothesis.

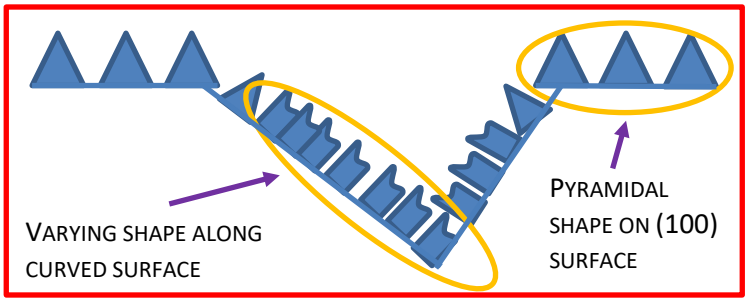

Figure 4. Illustration of formation of a higher reflecting line along wafer cut direction in a textured wafer.

An low-mag SEM image of Fig. 5a shows a nearly periodic pattern of streaks in the textured wafer (SDR depth = 2 □m and texture height of 2 □m. A magnified view of one of the regions is shown in Fig. 5b, which has a V-groove channel with slat-like texture shape.

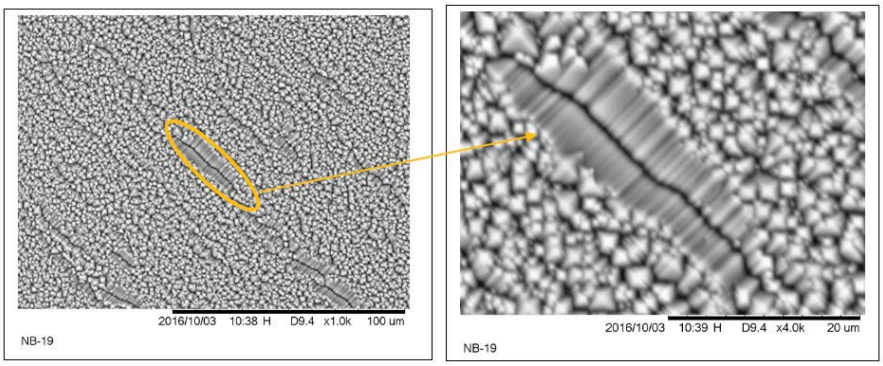

Figure 5. (a) An SEM image of a wafer with 2□m texture/2□m SDR showing texturing over cutting streaks that produce elongated texture resembling texture 0n (110) orientation. (b) a higher magnification view of the labelled region showing a detailed shape of the texture along streak walls.

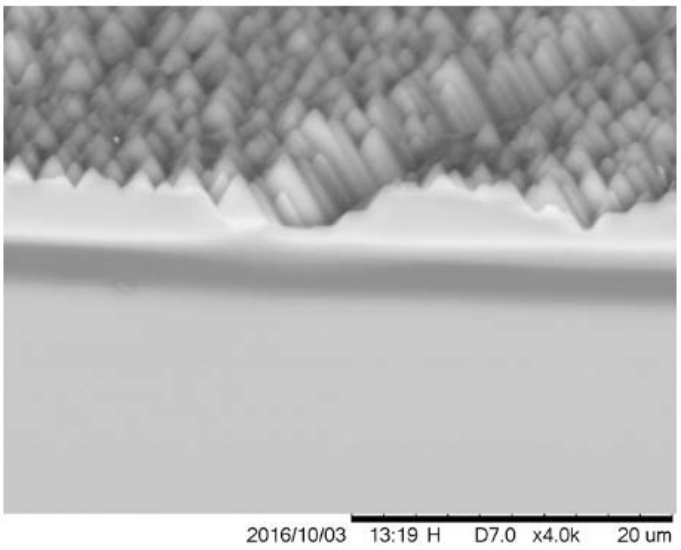

Fig. 6. An SEM image of a cross-section of wafer with 2□m texture/8□m SDR showing significantly less elongated texture on the streak walls after rounding by SDR.

A similar shape can be also be seen in the cross-section. Please note that with increasing SDR thickness removed, the walls of the V-groove become shallower and the severity of the deviation in the texture shape also diminishes. Figure 6 shows an SEM C/S of a wafer that had 8□m SDR removal, which shows texture shape is well retained in the region of streak.

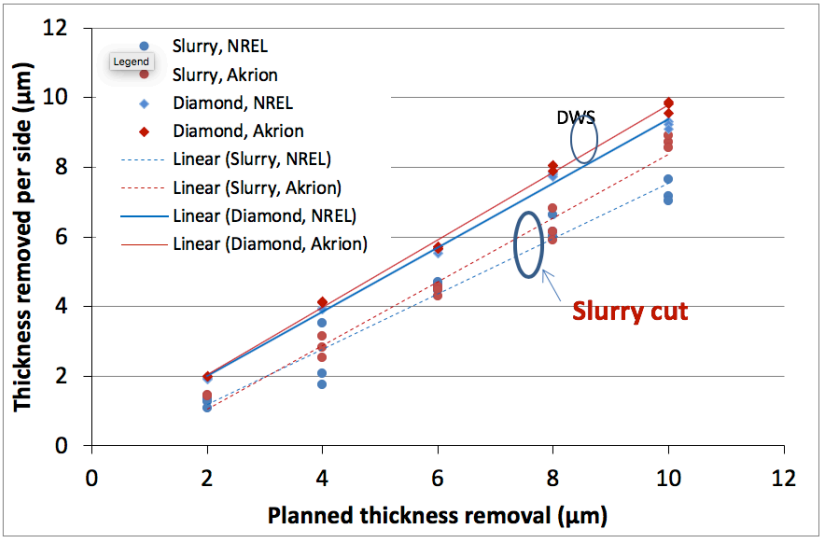

Fig. 7. A plot of thickness removed/side at various SDR etches for slurry and DWS wafers. The etch rate is higher for DWS wafers indicating slightly higher average damage. Etch rate is also slightly higher for Akrion cleaned wafers compared to those cleaned at NREL.

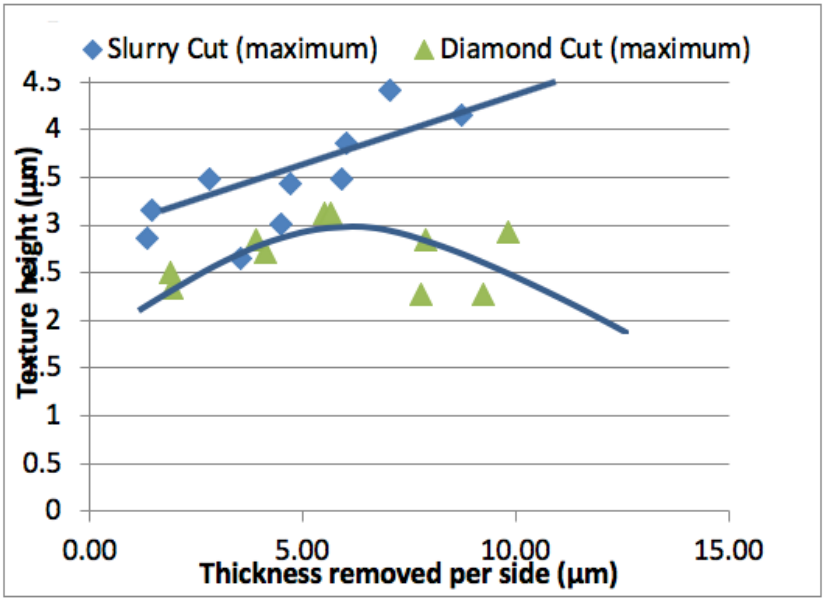

Fig 8. Maximum texture height as a function of SDR thickness removed for slurry and DWS wafers. Lines are drawn to guide the eye.

This research also yielded some very interesting and valuable results.

A. The etch rate during SDR depends on cleaning process as well as wafering technique. Figure 7 shows a plot of thickness removed/side for slurry cut and DWS wafers for each of the SDR etch. It is seen that slurry cut wafers have lower etch rate compared to the DWS wafers. Furthermore, NREL cleaned wafers showed lower etch rate than Akrion cleaned.
B. The maximum texture height is higher for slurry cut wafers compared to DWS wafers and increases with SDR thickness removed. For DWS wafers, the texture height seems to have a peak around 6 □m of SDR thickness removed.
C. The reflectance of the textured wafers varies with SDR thickness removed. Figure 9a shows reflectance spectra of textured wafers from all SDR groups. The figure 9b is a magnified view to show the details. Minimum reflectance occurs for 6 □m SDR thickness removed. Reflectance is highest for 2 µm SDR thickness removed (with a difference of about 1.5%). This behavior is consistent with observations that high-reflectance streaks are most pronounced for 2□m texture/ 2 □m SDR thickness removed.

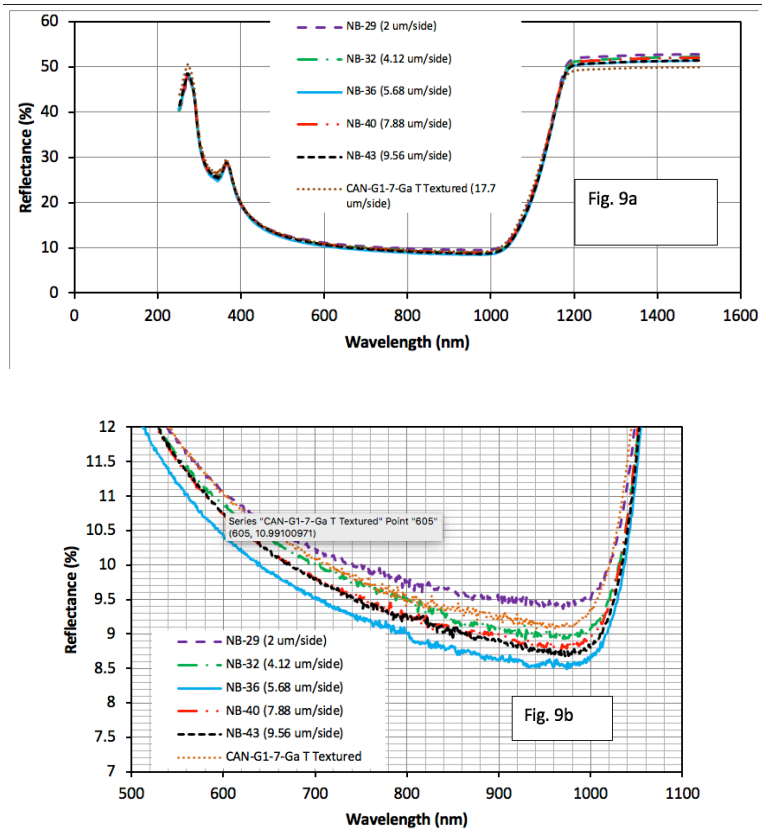

Fig. 9. (a) Reflectance spectra of textured wafers with different SDR thickness removed. (b) magnified view showing details of the reflectance spectra.

Task 7.4. Solar cell fabrication

Solar cells were fabricated on the textured N-type, DWS, wafers that had 2 □m texture with different SDR thicknesses removed. Because the lots were small, slurry cut wafers were included for comparison. The wafers were precleaned at NREL and Akrion. Interestingly, although cleaning steps are different, both procedures yielded almost identical results in texturing as well as cell performance. Cells were fabricated at Georgia Institute of Technology using their standard processes of B-implant for the front junction and a P diffusion to include a gettering step. It should be noted that the GIT process has been developed for DWS wafers: thickness ~180 □m, texture height ~ 4-5 □m, it does not include a pre-cleaning process step. A set of slurry cut wafers (from a different vendor) was textured along with DWS wafers and included for solar cell fabrication.

Figure 10 shows averaged cell parameters (Voc, Jsc, FF, and eff) for cells fabricated on DWS wafers, with different SDR thickness removed. It is seen that there is a general trend for all cell parameters to maximize at 6 to 8 □m of SDR removal. This is in spite of the fact that the wafer thickness decreases with increase in SDR removal. It is important to examine Jsc values which shows 0.5 mA/cm^2 variation (with max value of 39.6 mA/cm^2) between different SDR removed thicknesses. The best cell performance is very close to the best cell efficiency of 20.6% on GIT wafers. The important result is that our texturing, with small texture peaks and high texture uniformity represents processing quality (contamination-free cleaning and uniform texturing) as good as the best cells (with higher texture height and significantly more total thickness removal before cell fabrication).

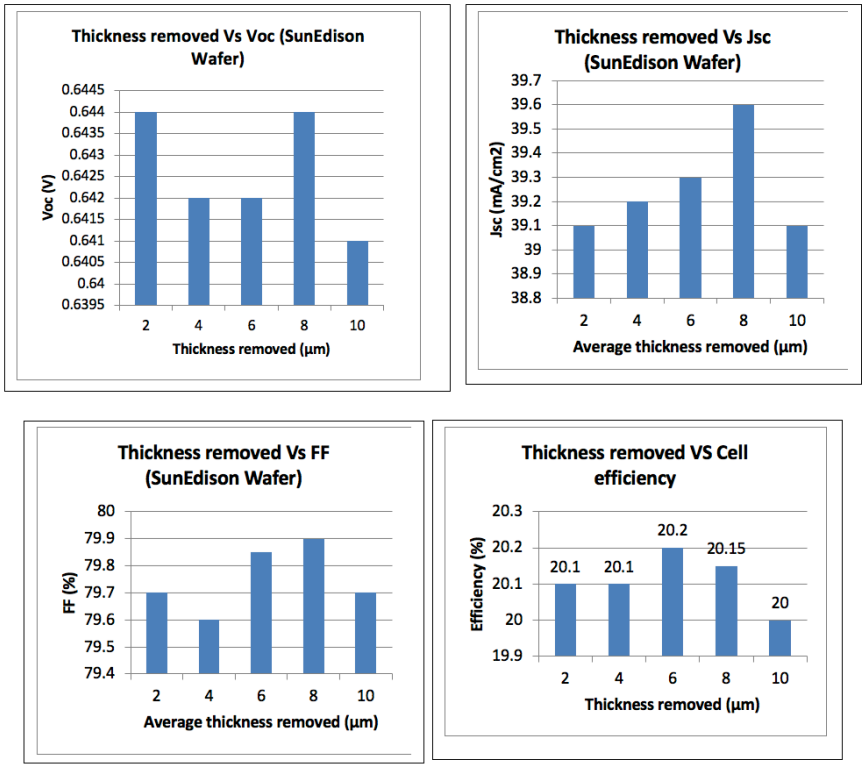

Fig. 10. Average cell parameters for DWS (SunEdison) textured wafers. Wafers have different SDR thicknesses removed, followed by the same, 2-□m texture. Wafers were cleaned at NREL.

The cells fabricated on slurry cut wafers did not perform as well as those fabricated on DWS wafers. Figure 11 shows the averaged cell parameters of these cells. Interestingly, Voc and Jsc are consistently lower while FF is generally higher. It is believed, that the quality of the slurry cut ingot was significantly poor as compared to the DWS ingot.

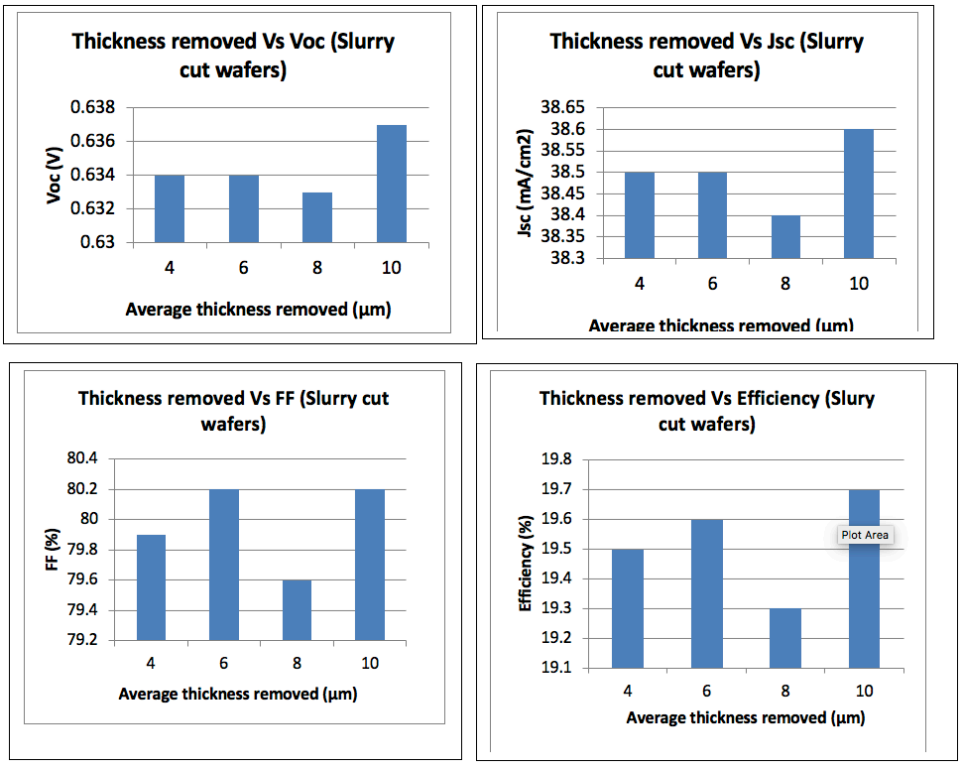

Fig. 11. Average cell parameters for slurry cut (GTAT) textured wafers. Wafers have different SDR thicknesses removed, followed by the same, 2-□m texture. Wafers were cleaned at NREL.

Summary/Conclusions

NREL has determined that textured, DWS, monocrystalline wafers show two types of nonuniformities, which are related to distribution of surface damage introduced during sawing. The direct influence of damage is associated with deep and sharp pseudo-periodic scratches, microcleavage tracks, and gouges that are not fully smoothened by SDR. These produce variations in the texture shape and concomitant higher local reflectance regions. They can be mitigated by longer etching during SDR. Typically, if the SDR etching is done to remove surface layer of average damage depth, texturing will be devoid of the striations. The indirect influence of damage is occurrence of contamination bands. These bands can be eliminated by suitable wafer cleaning before they go into high-temperature etch bath(s).

It is believed that the contamination comes from the diamond wire during cutting when diamond wire or parts of wire rubs into the ingot. Typically, in DWS if the “wire-use” parameter is high, the diamond chips either become blunt or fall off. This can lead to an intimate contact between steel core and the wafer surface. Thus, some of the Fe (and perhaps other impurities) from the stainless steel core is embedded into the wafer surfaces. The

propensity of such contamination will follow the damage depth profile, which exhibits striations as described in reference. It is a general experience that cleaning DWS wafers is particularly difficult because of surface roughness and its morphology. A typical cleaning procedure generally used in manufacturing (which seems to work well for slurry wafers) is not adequate for DWS wafers.

NREL believes that the main mechanism for contamination is that traces of impurities on the wafer diffuse in during higher temperature cleaning itself. For example, SDR and texturing are typically carried out at 80 °C for 20 to 30 minutes. Any contamination (e.g. Fe with diffusivity of ~10^{-12} cm^2/s at 80 °C) will diffuse few □m deep.

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None

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None

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