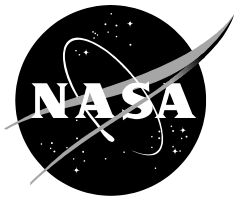


NASA/TM-20210014982



**SEE Test Report for Analog Devices
ADP3330 High Accuracy, Ultralow IQ, 200
mA, SOT-23, anyCAP Low Dropout
Regulator**

Raymond Ladbury

June 2021

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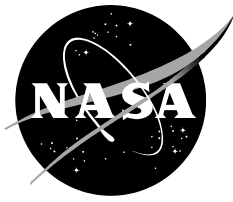
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SEE Test Report for Analog Devices ADP3330 High Accuracy, Ultralow IQ, 200 mA, SOT-23, anyCAP Low Dropout Regulator

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Test Date: 24-27 October 2014
Report Date: 04 November 2014*

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1. Reference Documents

- ADP3330 Datasheet, http://www.analog.com/static/imported-files/data_sheets/ADP3330.pdf ,9/15/2014
- Johnston, A.H., "The influence of VLSI technology evolution on radiation-induced latchup in space systems," *IEEE Trans. Nucl. Sci.*, vol.43, no.2, pp. 505-521, Apr 1996.
- "IEEE Recommended Practice for Latchup Test Methods for CMOS and BiCMOS Integrated-Circuit Process Characterization," *IEEE Std 1181-1991*. (Deprecated)
- JEDEC JESD57

2. Purpose

The primary purpose of this testing is to characterize the Analog Devices ADP3330 LDO regulator for single-event latchup (SEL) susceptibility. These data will be used to assess the SEL risk for the OSIRIS-REx Laser Altimeter (OLA). A secondary goal is to assess the susceptibility of the regulator to single-event transients (SET) and other nondestructive Single-Event Effects (SEE).

3. Test Samples

Six (6) parts were being provided to Code 561 for de-encapsulation and SEL testing. During this processing, it was discovered that the parts were mounted die facing downward in the package. Because the parts had to be mounted on the daughter card prior to the plastic being etched, this meant that the parts were soldered with the die facing the board. It was not feasible to unsolder the parts, re-form the leads and resolder the parts, so we decided to drill through the mother board, daughter board. Miraculously, one of the parts was fully functional after this treatment. This part was exposed to heavy ion irradiation. However, the fact that the beam had to pass through small holes in the mother and daughter cards before reaching the regulator die, it was only possible to irradiate this part at normal incidence. More information about the devices can be found in Table I.

The part was prepared for testing by removing the plastic encapsulation from the target die on the underside of the part. These parts were fabricated in bulk BiCMOS technology. Since we do not know the number of overlayers used in these processes, linear energy transfer calculations were recorded based on the top-surface incident ion species and kinetic energy, and we ensured that the particles had a range in Si of more than 100 microns from the top of the die.

Table I: Part Identification Information

Qty	Part Number	LDC	Source	Package
1 functional after processing	ADP3330	N/A	Analog Devices	6-lead SOT-23

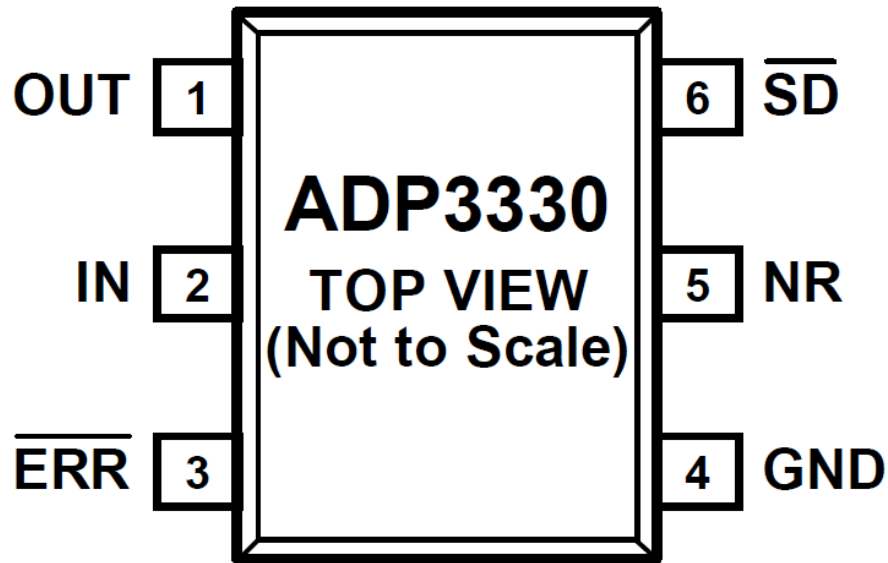


Figure 1: Pin diagram for ADP3330 LDO voltage regulator

4. Test Facility

Facility: Texas A&M University Radiation Effects Facility. Tune: 15 MeV/amu

Flux: 5×10^3 to 5×10^5 ions $\text{cm}^{-2} \text{s}^{-1}$

Fluence: All tests will be run to a fluence of $5 \times 10^6 \text{ cm}^{-2}$ or until a latchup event is observed

Table II: Possible Ions Used for Device Irradiation

Ion	Energy (MeV)	Range in Silicon	Silicon LET ($\text{MeV cm}^2/\text{mg}$)
^{197}Au	2954	155	80.2
^{129}Xe	1934	156	47.3
^{109}Ag	1634	156	38.5
^{84}Kr	1259	170	25.4
^{40}Ar	599	229	7.7
^{20}Ne	300	316	2.5

Note that energy, range, and Linear Energy Transfer (LET) are those characteristic of ions before traversing the aramica window and 50 mm of air prior to the silicon target.

5. Test Conditions and Error Modes

Table III - Test Conditions

Test Temperature	Ambient and $>80^{\circ}\text{C}$
Test Inputs	Static VCC
Power Supply Voltage	4-10 Vdc
Parameters of Interest	LET _{th} , temperature, supply voltage
SEE Conditions	Prolonged and self-sustained high-current state, SETs

Current limit was set $> 110\%$ of absolute maximum rating. In the event of observing SEL, a destructive test limiting current to 1 A could be run.

6. Test Methods

The test circuits for these devices were built to approximate the intended application. The accompanying figure captures the essentials of the application.

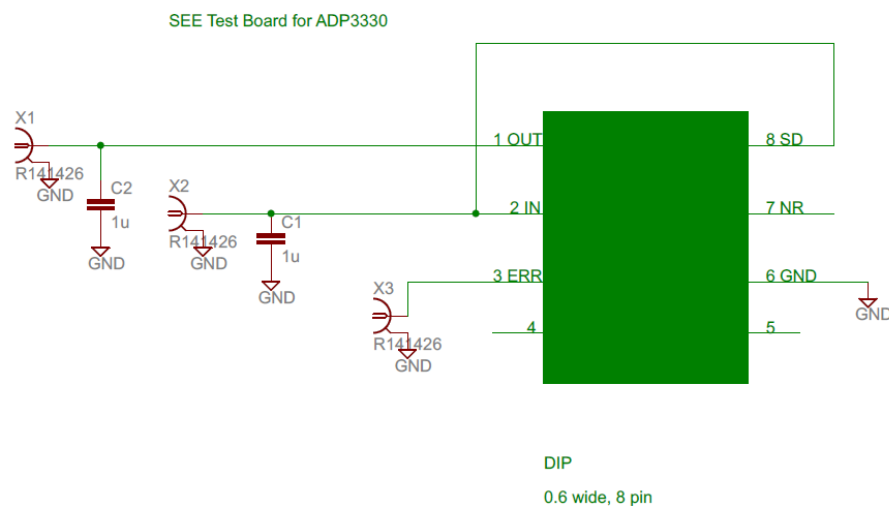


Figure 2: ADP3330 test circuit

The test setup required only power supplies and data logging equipment. The power supplies will be located in the irradiation cave, while the data logging equipment will be in the control room. Each test board has a single device under test, with new samples switched by hand.

7. Test Performance

Test personnel included the principal investigator, the test engineer and an observer for CSA. Eight hours were allotted for the test. A run was stopped if an SEL is seen or if the effective fluence reached 5×10^6 ions/cm². The following table is a rough outline of the tests planned during the test slot.

Table IV: Test Condition Plan

Condition	Temp (°C)	Tilt (°)	Roll (°)	Ion	Notes
1	80	0	0	Ne, Ar, Kr, Xe, Au	SEL Test
2	25	0	0	Ne, Ar, Kr, Xe	Characterize SET behavior

8. Results and Test Report

No SEL was seen up to the highest LET tested (53.1 MeVcm²/mg with Xe at normal incidence, since the mounting of the die precluded testing at other angles to the normal) and at the highest temperature tested (80 °C). We also tested with Au ions, but the results seem unphysical (substantially lower cross section than for the nominally lower LET Xe ions), so these are deemed untrustworthy. SET were seen with Xe and Au ions. No SET were seen with Kr ions, suggesting that the onset LET is >28.8 MeVcm²/mg. Because we only have SET data for one ion (that we trust) a full SET rate estimation is not possible. However, making worst-case assumptions, we conclude that the chances of seeing a transient from this device during the mission are less than 1%.

9. Implications of Results

The low cross section and high LET threshold for transients and the immunity to SEL suggest that this part will fulfill its requirements for OLA's mission without significant impairment due to radiation effect.

