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Single-Event Effect Test Report Texas Instruments DS25BR100 LVDS Buffer

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1. Introduction

This study was to determine the destructive single-event effect (SEE) susceptibility of the DS25BR100 series Low-Voltage Differential Signaling (LVDS) Buffers with Pre-emphasis and Equalization (DS25BR100, 110, and 120). The device was monitored primarily for destructive events while exposing it to a heavy ion beam at the Texas A&M University's (TAMU) K500 Cyclotron.

2. Test Result Summary

The DS25BR100 experienced permanent, destructive single-event latchup (SEL) at a linear energy transfer (LET) of 30.8 MeV·cm^2/mg at room temperature and at 85°C. No SEL was noted at an LET of 21.3 MeV·cm^2/mg at room temperature. After the destructive effect was observed on the DS25BR100, no testing of the DS25BR110 or DS25BR120 parts was performed. Limited single-event upset data was captured.

3. Devices Under Test

The DS25BR100, DS25BR110, DS25BR120 are LVDS buffers manufactured by Texas Instruments on a BiCMOS process and sold as COTS (commercial off the shelf) products. The DS25BR100 has control pins for output pre-emphasis (PE) and input equalization (EQ); the DS25BR110 is equipped with EQ only, and the DS25BR120 is equipped with PE only.

The device's LVDS pins are terminated with 100 Ω internally. Three DS25BR100EVK evaluation kits were obtained, each with three testable devices (one each of the 100, 110, and 120) for a total of nine (9) devices. These devices were prepared for testing by chemical/laser decapsulation of the plastic package to expose the silicon die. The device was packaged in a wire-bonded WSON-8 package soldered to a DS25BR100EVK evaluation board.

Note that the device primarily under evaluation for use was the DS25BR100, which is the top device on each evaluation board. The other two devices present were prepared for testing to evaluate process and family susceptibilities, but were not tested following destructive SEL in the DS25BR100.

The Radiation Effects and Analysis Group (REAG) internal ID# for this device is 20-016. The lot date code of the devices tested is unknown, but they were commercially procured in 2019. A total of three DS25BR100 devices were irradiated, and none of the DS25BR110 or -120 devices were irradiated.

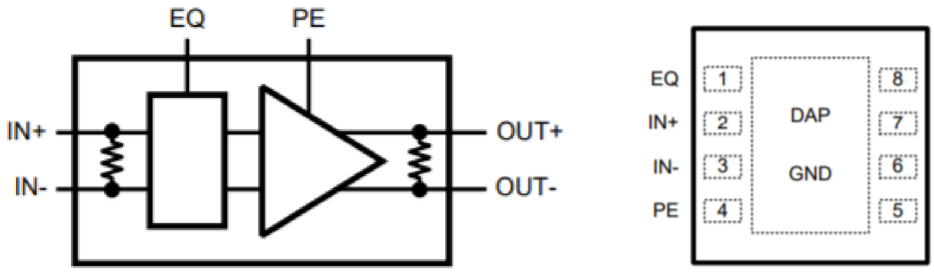

Fig. 1. Device functional diagram [DS25BR100 datasheet] and package pinout

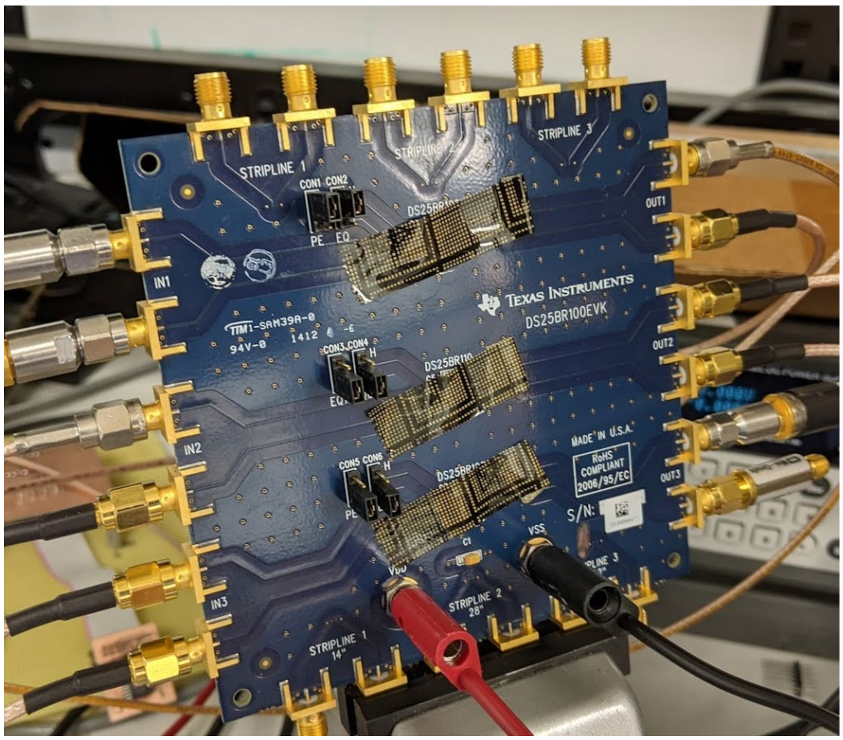

Fig. 2. DS25BR100EVK board with three decapsulated devices ready for testing.

4. Test Facility

Facility: Texas A&M University Cyclotron Institute, K500 cyclotron, 25 MeV/amu tune

Flux: Approximately $2x10^4 cm^{-2} s^{-1}$.

Fluence: Testing was conducted to $1x10^7 cm^{-2}$ at the worst-case planned test condition.

Ions / LET: During this test, limited ions were available due to facility maintenance. The highest nominal LET was 25 MeV/amu Xe, at 42.7 $MeVcm^2/mg$.

5. Test Conditions

Test Temperature: Worst case for SEL runs: 85°C.

Operating Frequency: 3.125 Gbps

Power Supply Voltage: Worst-case SEU: 2.97 V; Nominal: 3.3 V; Worst-case SEL: 3.63 V

Parameters of Interest: Power supply current (I_{DD}), Errors, Sync Losses

On-board control signals: Select equalization level by setting the EQ pin and select pre-emphasis level by setting the PE pin as in ***Table 1***.

Table I. Truth table selection of EQ and PE on DUT Test Boards
(primary config of interest is highlighted)

DS25BR100 (TRX)			
EQ (CON2)	**PE (CON1)**	**Equalization**	**Pre-emphasis**
L: 2-3	L: 2-3	Low (4dB)	Off
L: 2-3	H: 1-2	Low (4dB)	Medium (6dB)
H: 1-2	L: 2-3	Medium (8 dB)	Off
H: 1-2	H: 1-2	Medium (8 dB)	Medium (6dB)
DS25BR110 (RX)			
EQ1 (CON3)	**EQ0 (CON4)**	**Equalization**	**Pre-emphasis**
L: 2-3	L: 2-3	Off	*N/A*
L: 2-3	H: 1-2	Low (4dB)	*N/A*
H: 1-2	L: 2-3	Medium (8 dB)	*N/A*
H: 1-2	H: 1-2	High (16 dB)	*N/A*
DS25BR120 (TX)			
PE1 (CON6)	**PE0 (CON5)**	**Equalization**	**Pre-emphasis**
L: 2-3	L: 2-3	*N/A*	Off
L: 2-3	H: 1-2	*N/A*	Low (3dB)
H: 1-2	L: 2-3	*N/A*	Medium (6 dB)
H: 1-2	H: 1-2	*N/A*	High (9 dB)

6. Test Methods

The primary test was operation of the device under worst-case conditions for single-event latchup (V_{DD} = 3.6 V, Temperature > 85°C) while monitoring power supply current for high-current states. A 2.025 Gbps pseudo-random bit sequence (PRBS) was provided to the input pins, and a bit error rate tester (BERT) was used to monitor for functionality and count errors on the output side. For most testing, all three devices on the evaluation board were attached in series, with only a single buffer actively irradiated. Testing was also performed with individual devices isolated to ensure the effects observed were not influenced by the attached buffers. A schematic of the test is shown in Fig. 3.

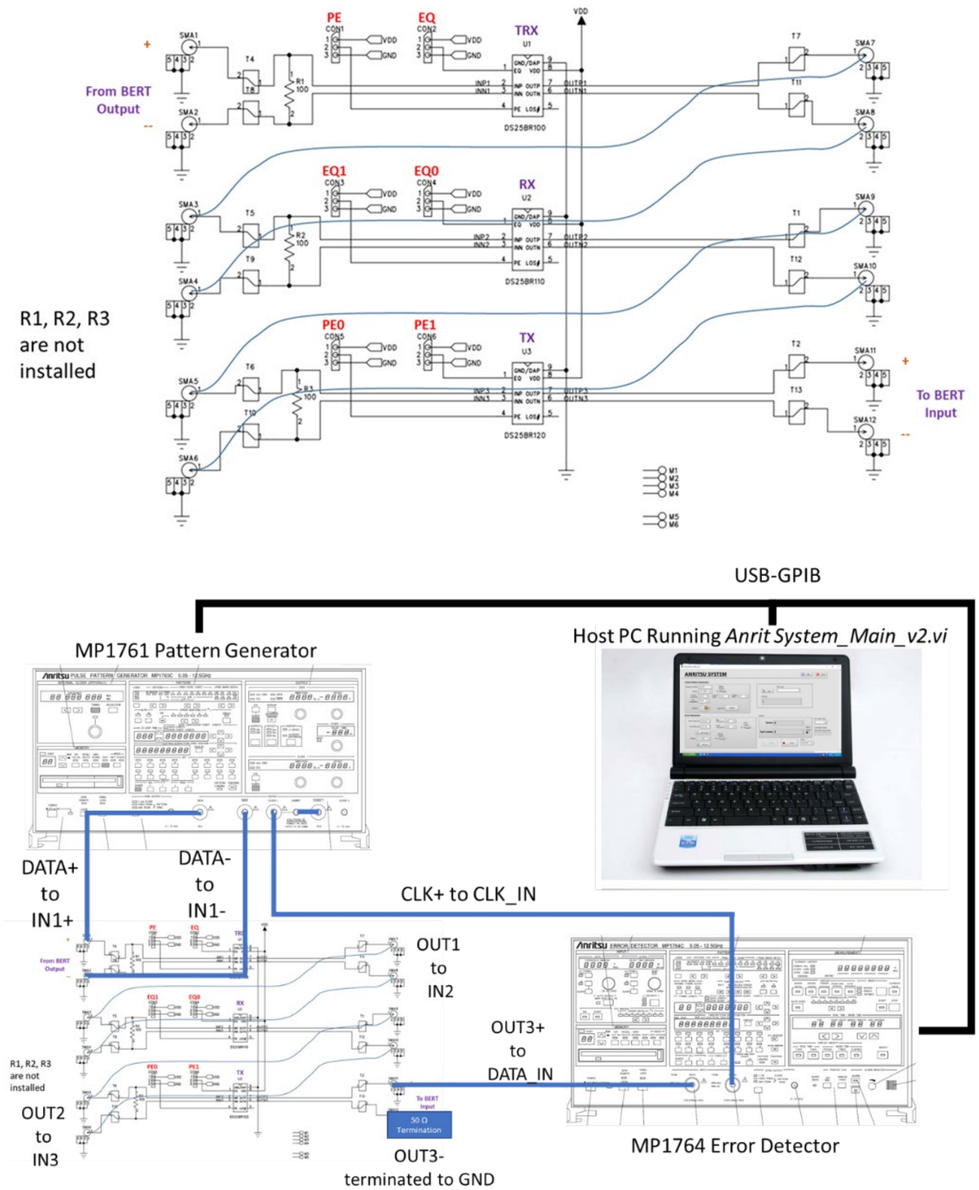

Fig. 3. Schematic of evaluation board (top) and test equipment setup (bottom).

7. Test Performance

Personnel: Michael Campola (NASA)

The notional testing plan is provided below for reference as it existed in the test plan. Test time and beams available were limited.

1. Prefer to start with a high-LET beam, such as 15 MeV/amu Au. Due to time constraints likely on this test, if a lower LET beam is already tuned and can generate an LET_{eff}>75 MeV·cm^2/mg, use that instead to eliminate a beam change.
2. Test at V_{DD} = +3.63 V, V_{SS} = GND, Temp ~ 85 °C, Fluence to 1E7. Monitor power for indication of SEL failure. This is a worst-case test, on a COTS part. Starting with the worst-case will save time during this constrained test window.
3. If pass, repeat with sample #2 on the DUT board. If it passes, the primary test of the device is complete. Return to room temperature and gather SEU data at V_{DD} = 2.97 V on the part with a repeated run at the same LET.
4. If either part fails, switch a different DUT board into the daisy chain, reduce voltage to +3.3V and repeat once. The application voltage is 3.3V. I would prefer a high-LET, high-temperature passing run at reduced voltage over a lower-LET test at full voltage due to low application needs.
5. If fails at lower voltage, reduce LET to ~37 and repeat, starting at 3.3 V. If still fails, end test (consider revisiting as time allows). If pass, repeat at LET = 50-60 at both voltages and gather SEE data as time allows at ambient temperature and reduced voltage to fill out the SEU Weibull curve.
6. Upon obtaining the SEL threshold, reduce LET until the SEU threshold is found for a good estimate of error rate.

8. Test Results

8.1. Single-Event Latchup (SEL)

The DS25BR100 was first irradiated with 42.7 MeVcm^2/mg Xe, with a range of 220 um in silicon. At ambient temperature and nominal voltage (3.3 V), single-event latchup was observed. The power supply current jumped to the hardware limit of 500 mA. This was repeated on several runs and several devices, and for the four runs on which fluence-to-failure was noted, the average cross-section was 2.18×10^{-6}cm^2.

A sample was heated to 85C and exposed to greater than 1×10^7/cm^2 at an effective LET of 60.4 MeVcm^2/mg by use of beam degraders to reduce energy. Single-event latchup was again observed, limited by the 500mA power supply compliance. No parts were catastrophically damaged during this phase of testing.

At an LET of 30.8 MeVcm^2/mg and ambient temperature, SEL was observed. After one test to 2.30×10^6/cm^2, the device was catastrophically destroyed and could not be restored to functionality.

Finally, at an LET of 21.3 MeVcm^2/mg, three tests to a total of 5x10^6/cm^2 at ambient temperature did not result in any single-event latchup, but time did not allow for additional testing at elevated temperature.

8.2. Single-Event Upsets (SEU)

Single-event upset data was a secondary objective of this test. Many runs were obscured by SEL that caused a near-infinite number of errors to be recorded. However, the data in the following table is selected from runs that completed without SEL. No clear cross-section vs LET curve is possible from the limited dataset, but it may be useful in understanding the magnitude of possible errors from this device.

Table II. Selected Single-Event Upset Test Runs

Effective LET (MeVcm^2/mg)	Power Supply Voltage (+/- V)	Temperature (°C)	Data Rate	Fluence (/cm^2)	Errors
60.4	3.6	85	2.025 Gbps	9.9E5	772
60.4	3.6	85	2.025 Gbps	2.6E6	686
21.3	3.3	25	2.025 Gbps	1E6	421
21.3	3.3	25	2.025 Gbps	3E6	688
30.8	3.6	25	3.125 Gbps	1E6	403
30.8	3.6	70	3.125 Gbps	5.58E6	1376

9. Summary

The DS25BR100 is susceptible to single-event latchup at an LET of 30.8 MeVcm^2/mg at room temperature. The threshold LET at room temperature is greater than 21.3 MeVcm^2/mg; no threshold was determined at elevated temperatures. One device was catastrophically damaged during testing.

10. Appendix 1: Equipment List as Tested.

MFG and P/N	Function	S/N or ECN	Calibration Status
Dell Laptop		5065858	
Anritsu MP1761B	Pulse Pattern Generator	M162840	
Anritsu MP1764A	Error Detector	M162842	
Keithley 2230-30-1	DC Power Supply	M164756	