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Productization and Manufacturing Scaling of High-Efficiency Solar Cell and Module Products Based on a Disruptive Low-Cost, Mono-Crystalline Technology

Final Technical Progress Report
April 1, 2009 — December 30, 2010

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Solexel, Inc.

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Subcontract Report
NREL/SR-5200-55733
July 2012

Contract No. DE-AC36-08GO28308

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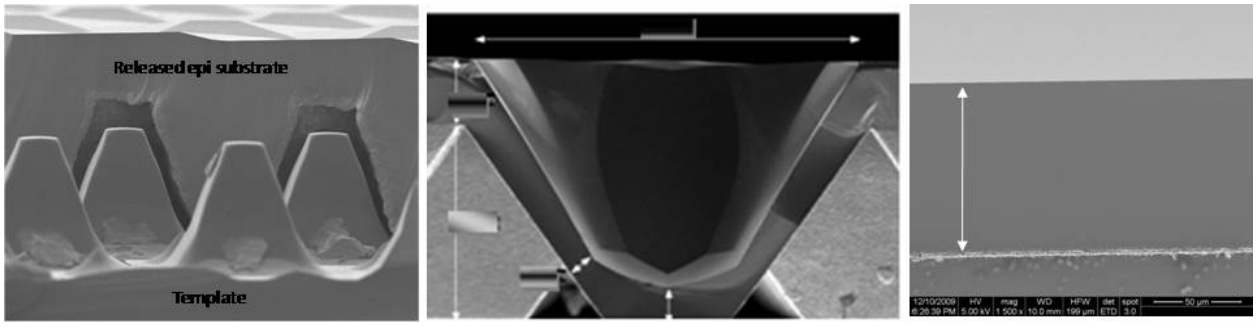
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Project Objective: The purpose of this project was to develop Solexel's Unique IP, productize it, and transfer it to manufacturing. Silicon constitutes a significant fraction of the total solar cell cost, resulting in an industry-wide drive to lower silicon usage. Solexel's disruptive Solar cell structure got around these challenges and promised superior light trapping, efficiency and mechanical strength, despite being significantly thinner than commercially available cells. Solexel's successful participation in this incubator project became evident as the company is now moving into commercial production and position itself to be competitive for the next Technology Pathway Partnerships (TPP) funding opportunity.

Deliverable Summary: Per the original SOW, the plan for template reuse was using a honeycomb Prism 3D structure using deep reactive ion etching (DRIE). However, Solexel decided to move to a crystallographic potassium hydroxide (KOH) etch-based process (Pyramid cell, i.e. PyCell). The choice of PyCell over Prism cell was driven primarily by three factors. Firstly, the Pycell lended itself more favorable to increasing the number of reuses from the mother template. This was facilitated by less variation in the dimension of the mother template after every reuse. Secondly, the wet etch process for creating the mother template in the case of PyCell was more cost effective than the DRIE in High Volume Manufacturing (HVM). Thirdly, because the PyCell did not require a complete epi fill like the prism cell, it afforded an atmospheric pressure epi process. This opened doors to very high deposition rates, thus increasing throughput and also helped carve out the path for substantially lower cost.

Additionally, when the solar market experienced a significant drop in cost of solar power in 2009, as well as then the developments in the Solexel's manufacturing processes, Solexel decided to move to textured flat cell structures. This was strongly motivated by further reducing the cost by going to very thin substrates, as well as the ease of reuse with flat cell over PyCell. Flat cell template had better mechanical strength with reuse compared to PyCell template. Formation of deep pyramids of the PyCell on the template resulted in significant amount of silicon to be removed from the template, so PyCell template was an effectively thinner substrate compared to the flat template of the flat cell structure. Also, template structure shape retention was easy with flat cell as the template is flat.

Whether the cell was Prism, PyCell or flat (Fig. 1), the general process paradigm remained the same and included using a master template, converting its surface to the sacrificial layer for release of the substrate, perfecting the release of the substrate from the mother template, and using the subsequently released substrate for cell processing.



(a) (b) (c)

Figure 1. The cross-sectional scanning electron microscopy (SEM) pictures of the three embodiments of Solexel's solar cell, a) Prism cell, b) Pyramid cell (PyCell), and c) Flat cell.

All images in this report are property of Solexel.

Solexel developed a sacrificial layer that enables successful release of epitaxial solar cell substrate from a master template, while enabling high quality epitaxial films. The optimization process which led to a good release as well as good quality epi-substrates involved tailoring thickness and the transfer of the sacrificial layer to an alpha tool.

Solexel also developed a high quality Epi deposition process by utilizing a pre-epi deposition bake process in order to increase the quality of epitaxial film while decreasing the epi process time. Defect density of 1.4E4 defects/cm^2, average bulk lifetime (τ_{bulk}) of 341μs and effective lifetime (τ_{eff}) of 146μs, all indication of good epi quality, were achieved.

Per the original SOW, Solexel needed to demonstrate 50 reuse cycles on a single template by releasing 156mmx156mm Thin Film Silicon Substrate (TFSS) with a yield of greater than 50%. Solexel completed this task by demonstrating the leading template to go through 50 reuse and release cycle and yielding 44 full 156mmx156mm 35μm stand-alone TFSS, which corresponds to a TFSS yield of 88%.

As for the cell efficiency, Solexel first developed the processes on 125X125mm CZ wafers and then transferred the process to 125X125mm TFSS. Then the substrate size was scaled to final 156X156mm TFSS with 192 circle trim on the corners producing cell efficiency of 15.23% as the highest efficiency level as verified by NREL and produced at the time of the final report. Solexel only delivered 2 out of required 5 cells as set by SOW at the target efficiency of 15%.

As for Module assembly and reliability performance, Solexel produced a 5x6 module with 90um 156mm pseudo-square TFSS cells assembled using conventional solder-coated copper tab interconnects and encapsulation. This module was submitted for temperature cycle testing at TUV-Rheinland in Arizona. The 2.6ft x 3.1ft module (8ft.sq approx.) was subjected to 200 cycles of thermal cycling from -40C to 90C per the requirements of IEC61215 at 10 cycles per day. The performance of the module pre- and post- lamination as measured at Solexel and TUV-Rheinland. The module efficiency pre-lamination was 11.8% and 11.1% post lamination as measured at Solexel and 10.4% as measured at TUV-Rheinland (including connectors). After 200 temperature cycles, the module power had dropped by only 3.1% satisfying the performance requirements for IEC61215 per the deliverable. After 138 cycles, the module was damaged due to a handling issue in the chamber but nevertheless still passed the IEC requirement confirming the robustness of the design.

Solexel started a pilot fab in Milpitas, CA. The sacrificial layer formation and epi capacity set the fab capacity as released substrates were supplied to cell processing. In addition to the alpha sacrificial layer tool, Solexel established a batch epitaxial silicon tool. The batch epi tool at Solexel Pilot Fab ran 7x24 to maximize the output. Epi module was staffed to run in 4x12 hour shifts in a compressed work week format. Epi weekly capacity maped to ~20 runs/week or nearly 200 epi substrates/week. Solexel Pilot Fab was set up for 5x24 coverage for front-end and back-end solar cell processes. These process modules were staffed to run in 3x8 hour shifts in a normal work week format. Total fab shift coverage was >120 hours/week, for epi being 168 hours/week. Capacity at Pilot Fab of >20KW/year at targeted efficiency for 156x156 targeted size solar cells was established. Solexel also ordered a second batch Epi tool which arrived during the first week of October 2009. This second batch Epi tool increased available capacity of the Pilot Fab to >50kW/year.

Solexel did not satisfy the requirement of 19% cell efficiency nor the pilot line capacity of > 3MWp due Dec 2010 as set by SOW. Similarly for the NREL goal of >3MWp pilot capacity, there was no reason to invest in the pilot line hardware when the final process of Record (POR) for cell processing and tool sets were not ready.

Task Accomplishments:

Task 1: Template Reuse

Subtask 1.1: Template Formation

This subtask required the demonstration of a process of record for creating a master template that enables scaling up to 156mmx156mm solar cells. Per the original SOW, the plan was to do this on a honeycomb Prism 3D structure using deep reactive ion etching (DRIE). However, Solexel decided to move to a crystallographic potassium hydroxide (KOH) etch-based process (Pyramid cell, i.e. PyCell). The choice of PyCell over Prism cell was driven primarily by three factors. Firstly, the Pycell lends itself more favorable to increasing the number of reuses from the mother template. This was facilitated by less variation in the dimension of the mother template after every reuse. Secondly, the wet etch process for creating the mother template in the case of PyCell was more cost effective than the DRIE in High Volume Manufacturing (HVM). Thirdly, because the PyCell did not require a complete epi fill like the prism cell, it afforded an atmospheric pressure epi process. This opened doors to very high deposition rates, thus increasing throughput and also helped carve out the path for substantially lower cost. Additionally, as a response to the solar market that experienced a significant drop in cost of solar power as well as due to recent developments in the Solexel's manufacturing process, Solexel decided to move to textured flat cell structures. The key cost advantage stems from the following factors:1. Capital cost to make the template, and 2. Easier to do template reuse, hence greater reuse numbers and amortization of the template.

Subtask 1.2: The Sacrificial Layer

The objective of this subtask was to develop a sacrificial layer that enabled successful release of epitaxial solar cell substrate from a master template, while enabling high quality epitaxial films. The optimization process which led to a good release as well as good quality epi-substrates involved tailoring thickness variation. Furthermore the sacrificial layer was tailored towards high volume manufacturing by acquiring an alpha porous silicon tool and transferring the sacrificial layer to this tool. The Alpha tool can process up to 24 master templates/hour with four chambers, and each chamber is well-characterized to give similar sacrificial layer properties. Pre-epi bake process was done in the epi chamber directly following the sacrificial layer formation and just before the epitaxial deposition.

The sacrificial layer on flat cell is expected to have better thickness uniformity than PyCell on both the active area and on the edge region of the cell. For PyCell structure, area difference between the active area and the unpatterned edge of the cell can cause non-ideal sacrificial layer on the edge. This can result in locking and thus epi leftover, which can potentially decrease the number of reuse cycles on such templates. The 3D textured Flat cell structure has proven to be less prone to this issue due to better porous silicon uniformity.

Subtask 1.3: Sacrificial Layer Etch Stop

By transitioning from DRIE-patterned honeycomb structures to KOH-etched pyramid structures (PyCell), the issue of dimensional change in master template and 3D released substrates with each re-use was nominally solved. This is because in a PyCell all dimensions get etched by the subtractive sacrificial layer by the same amount. As a result, dimensions of the template as well as the epitaxial films released from this template are preserved. Because of this, sacrificial layer etch stop process was not needed anymore. It simplifies the fabrication process while resulting in additional cost saving. Epitaxial films from this template also showed similar dimensions. This milestone was addressed by transitioning to the PyCell concept. By the same token, textured Flat cell structure did not need any silicon etch stop.

Subtask 1.4: Epitaxial Process

Epi process was optimized to produce TFSS on sacrificial layer with better than 2um growth rate. In parallel, pre-epi deposition was decreased down to the same temperature as the epi growth temperature in order to further increase the quality of epitaxial film while decreasing the epi process time. The defect density was improved from 1.5E4 defects/cm^2 to 1.4E4 defects/cm^2. Figure 2 shows released epitaxial substrates after the Wright etch. Wright etch was used as a staining technique to highlight the defects in the grown silicon. The facets seen in the epitaxial film are due to the unique epitaxial growth on the template.

In addition, Solexel continued to track the lifetime progress throughout the program. Table 1 shows the lifetime progress. Bulk lifetime (τ_{bulk}), dark current density of the emitter (J_o), and effective lifetime (τ_{eff}), which depends on τ_{bulk} and J_o, are summarized. These results reflect lifetimes when Solexel considered in-situ emitter as part of Epi deposition. As shown, bulk and effective lifetimes for the in-situ emitter process were comparable to the results reported before and J_o was improved. Solexel continued to have >20μs bulk lifetime with world class epi defect densities. By the end of the program, Solexel developed a high quality Epi deposition process by utilizing a pre-epi deposition same as the epi growth temperature in order to increase the quality of epitaxial film while decreasing the epi process time. Defect density of 1.4E4 defects/cm^2, average bulk lifetime (τ_{bulk}) of 341μs and effective lifetime (τ_{eff}) of 146μs, all indication of good epi quality, were achieved.

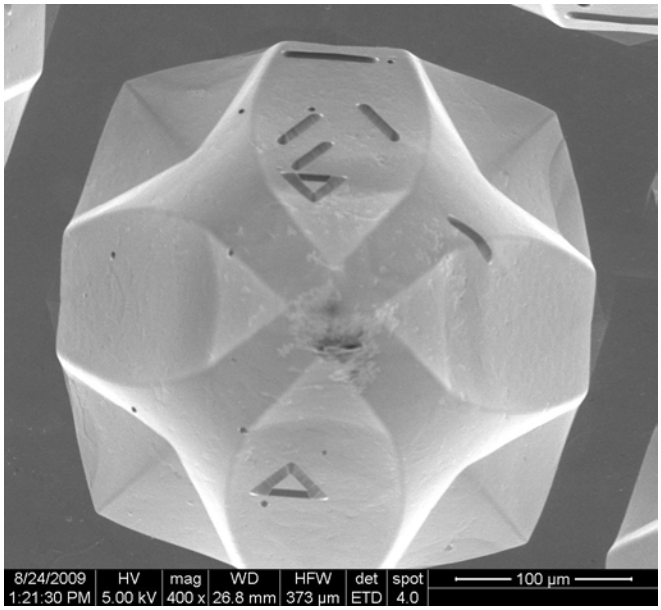


Figure 2. Epi defects highlighted using the staining technique developed in-house.

Table 1. Lifetime Progress at Solexel

	2/15/2009-3/15/2009	3/16/2009-4/15/2009	4/16/2009- 5/15/2009	5/16/2009- 9/15/2009 (In-situ Emitter)
τ_{bulk} (µs)	<3us	<5us	26.6	24.4
J_o (fA/cm^2)	>1000	>1000	264.7	<150
τ_{eff} (µs)	0.1-1us	1-2us	6.7	6.5

Subtask 1.5: Substrate Release

A highly simplified released process was developed which became a streamlined process in fabrication. Figure 3 shows the first released 156mmx156mm epitaxial substrate and its master template. Solexel also developed a laser scribe technique to replace manual scribe. Laser scribe was important for both reuse of the master template and the epitaxial substrate release yield. When the epitaxial substrate was manually scribed, there was a risk of damaging the master template. In addition, the scribed edges of the substrate could chip, or a crack might form and propagate during the release process. With laser process, chipping and cracking at the edges was kept to a minimum, thus increasing the release yield.

This scribe ensured the released substrate had the correct shape with minimum edge defects as described above. Figure 4 shows that the laser cutting process was well-controlled at various places on the wafer. This was true for both the outer circular scribe and inner solar cell scribe. Laser scribe was done in a series of cutting loops on both of these scribe areas. Increased number of laser cutting process, i.e. loops, deepened the laser cut down to a desired depth while keeping the depth uniform throughout the trench. SEM pictures on right-hand side of Figure 4 show such uniform depths of a circular scribe on a flat test wafer. The thickness of the epitaxial solar cell substrate will not be thinner than 20µm in order to keep the mechanical integrity of the released substrates. As a result, the cutting depth for number of loops smaller than three was not measured except for one data point for 2 cutting loops.

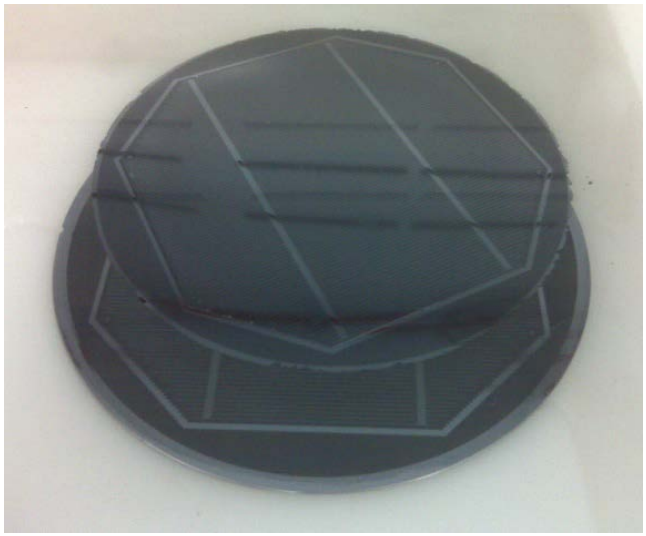


Figure 3. First 156mmx156mm epitaxial substrate and its master template released using SMR technique.

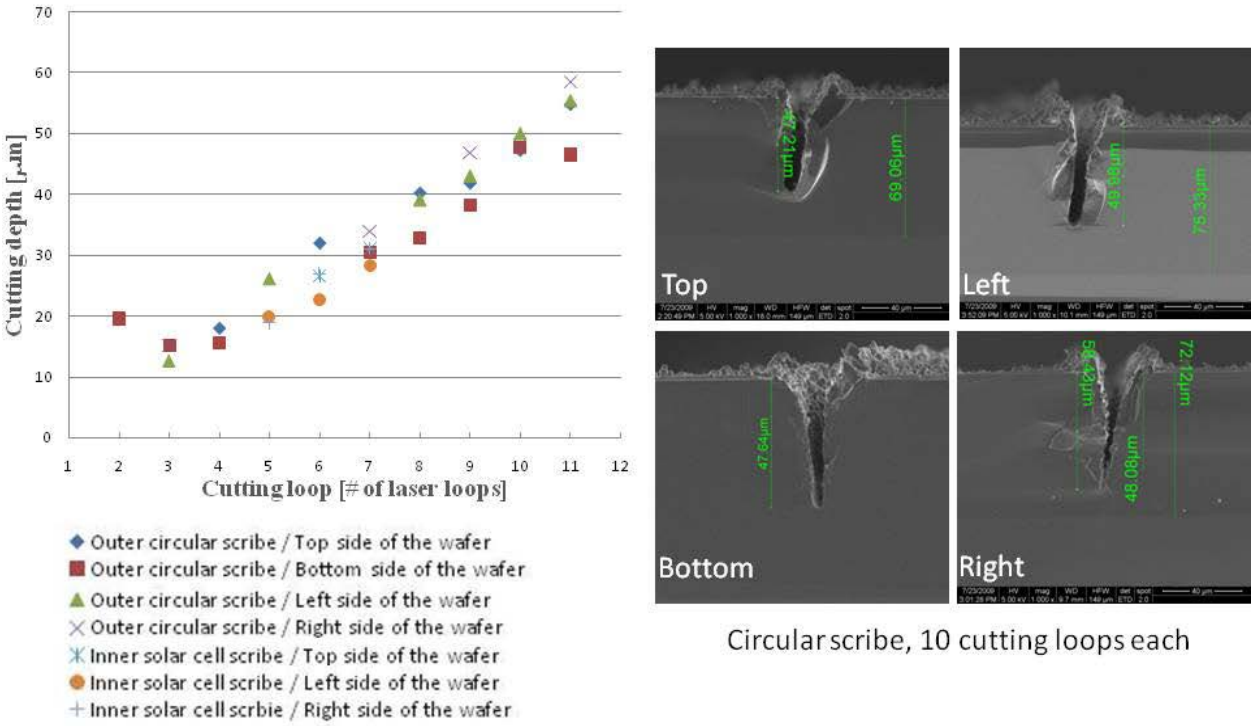


Figure 4. Laser cutting process is well-controlled at various places on a flat test wafer for both the outer circular scribe and inner solar cell scribe.

Subtask 1.6: Template Re-use

In the early part of the program, Solexel did show 5 reuses of the flat template by releasing 156mmx156mm flat TFSS while only 3 reuses of the PyCell template by releasing 156mmx156mm PyCell TFSS were demonstrated. This was later improved to 10 reuse cycles on a single template by releasing 156mmx156mm flat TFSS.

The three causes affecting the reuse and yield are

1- Chipping and breakage of the template

2- Unreleased, i.e. locked, areas of the TFSS

3- Template consumption

The highest frequency of template breakage was observed during mechanical release for higher reuse numbers, and close to the notch area. Further inspection of the wafers showed that there were accumulated epi at the backside of the template, which was suspected to cause point stress during vacuum chucking, especially close to the notch where the accumulated backside epi was the thickest. Figure 5 shows backside epi deposition across wafer orientation, and Fig. 5 shows the amount of backside deposition per reuse cycle. For 50μm TFSS, the maximum backside deposition was approximately 17μm, and there was no apparent correlation to the reuse cycle per each backside deposition (Fig. 6-b).

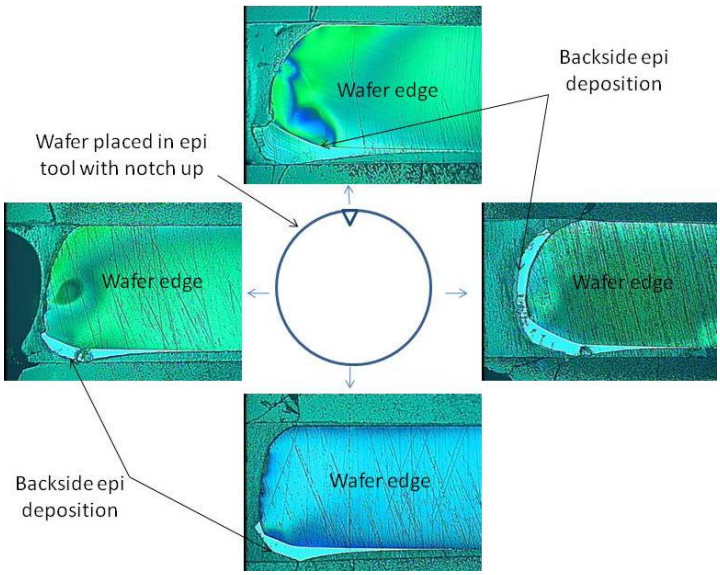


Figure 5. Backside epi deposition across wafer orientation.

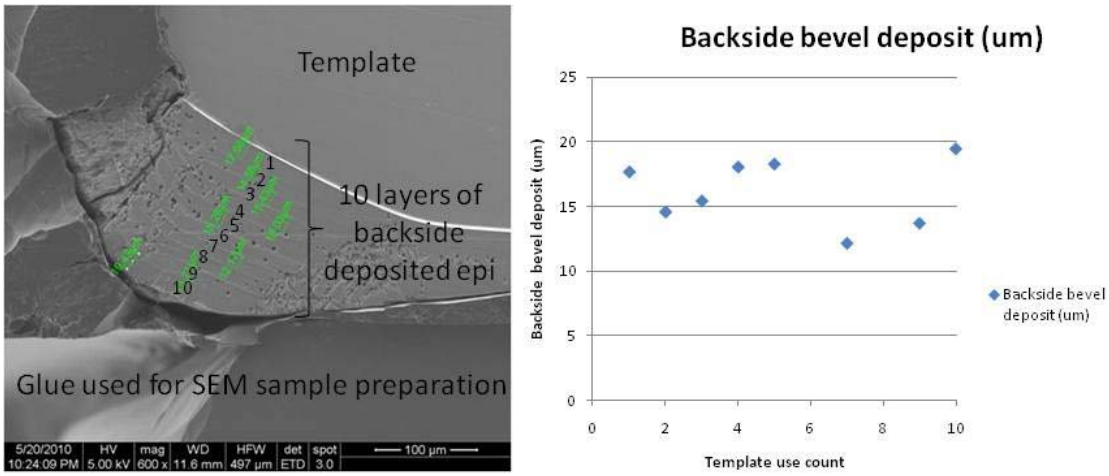
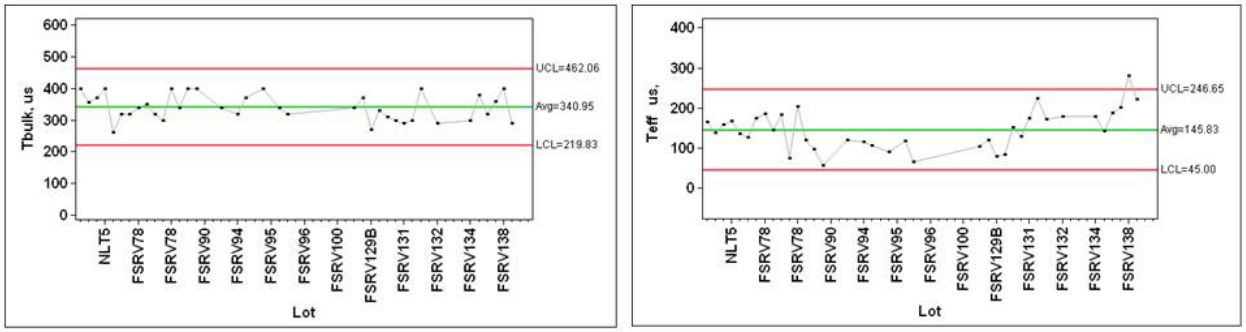


Figure 6. (a) Backside epi deposition close to notch, and (b) Deposition thickness for each template use count.

After the implementation of the fixes, the leading template completed going through the 50th reuse and release cycle and yielded 44 full 156mmx156mm 35 µm stand-alone flat TFSS. This corresponds to a TFSS yield of 88%.

Figure 7 shows bulk and effective lifetime baseline trend during the period when 50 reuse cycles were run at Solexel. All parameters are shown to be stable and in control. The average τ_{bulk} and τ_{eff} Solexel has achieved are 341µs and 146µs, respectively, measured on >35 samples. It should be noted that even though reuse was demonstrated on 35µm epi, in order to achieve lifetime measurements, epi thickness for the test wafers needs to be thick enough to enable full handling through the line for passivation and lifetime test. The current limit is >=90µm epi thickness.



(a) (b)

Figure 7. Bulk and effective lifetime baseline trend during 50 reuse cycles.

Task 2: Cell Process Development

Solexel originally started with the cell process flow using $POCl_3$ based doping for emitter and screen-print based metallization and fire-through for contact opening and metallization. Later on Solexel altered this cell flow for dopant application, contact opening and metallization by using in-situ epitaxial emitter doping, screen printed etch paste based contact opening and plating based metallization. By going to epitaxial emitter process, it was possible to save both the capital cost of $POCl_3$ and deglaze step as well as dramatically increase throughput. In addition, more control over the phosphorous profile potentially enabled higher performance as well.. Plated material was a lower resistivity material compared to the screen printed metal. This potentially enables a higher fill factor and efficiency.

Subtask 2.1: Dopant Application

In-situ emitter approach resulted in a very controlled emitter doping profile. It also obviated the necessity to purchase capital equipment for emitter doping and deglaze and reduced the thermal budget on the template. Emitter profile was optimized in order to provide a good contact to the metal, increase blue response and reduce Front Surface Recombination Velocity (FSRV). Figure 8 shows a SIMS profile of a typical in-situ epitaxially doped emitter. It shows epitaxially grown emitter which was also selective. The Boron base doping is 5e16/cm^3.

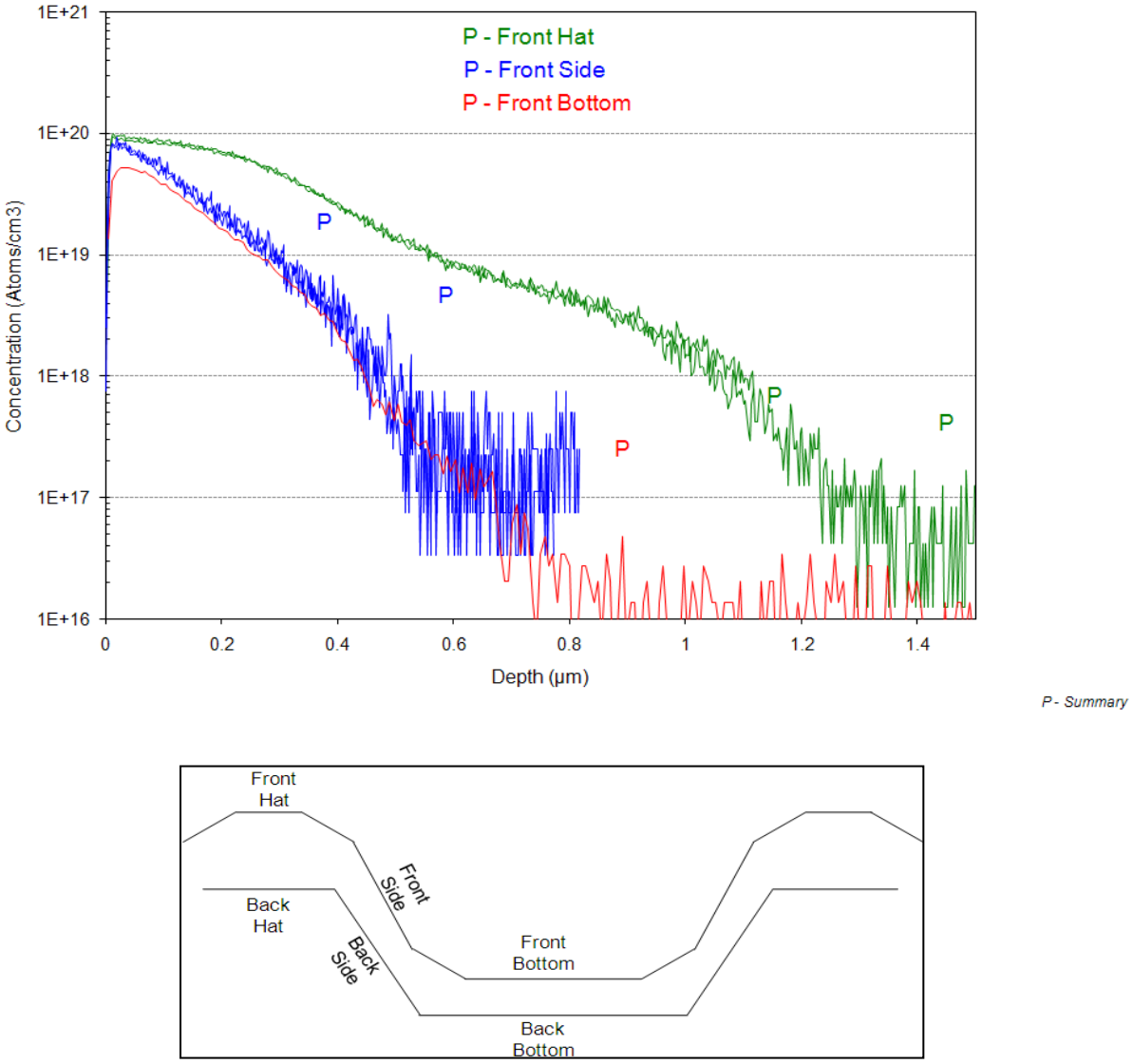


Figure 8. SIMS profile of in-situ epitaxially grown emitter at different locations on the cell.

Subtask 2.2: Diffusion/Passivation

Dopant diffusion was not needed as in-situ doped emitters were used for cell fabrication.

For the front-surface, Silicon Nitride (SiN) was used for passivation. Silicon Nitride deposited with our PECVD system has fixed positive charges on the order of $10^{12}/cm^2$ which reduced the FSRV by repelling the minority carriers (holes). The thickness of SiN was optimized for front-surface reflectivity.

For the back surface, we used in-situ epitaxially grown back surface field (BSF) for passivation. The thickness and doping concentration was optimized to improve efficiency. Figure 9 shows the effect of reduced metal coverage and thicker BSF on V_{OC} for a particular cell lot. BKM are cells with more metal coverage. BKM-ASP is BKM cells with aligned screen print which reduces

the metal coverage. BKM-BSF1 and BSF2 are cells with aligned screen print and thicker BSF than BKM-ASP. In this plot, the red boxes are the box-plots for the data (i.e. middle value in the box is the 50th%, upper is the 75th% and the lower is 25th%), each black dot is a data point for a cell, and the green diamonds are mean values with the upper and lower tips of the diamonds representing the 95% confidence interval value.

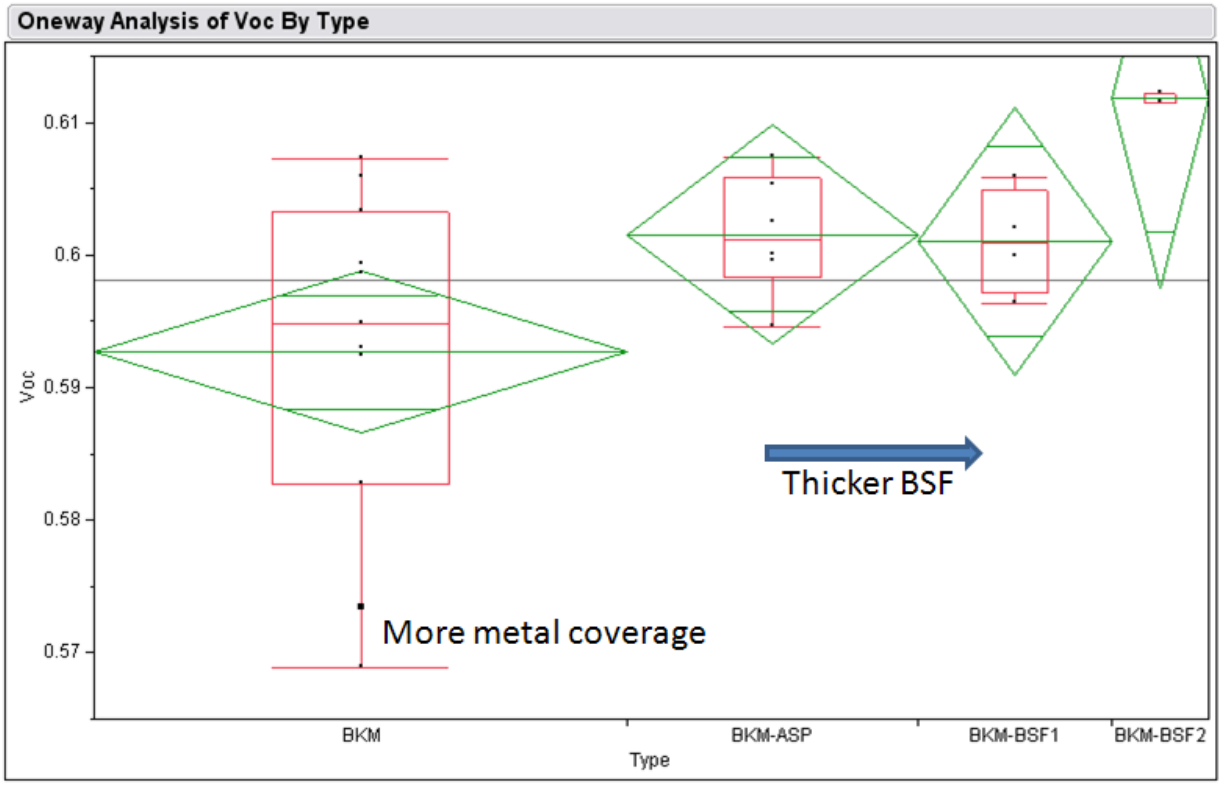


Figure 9. Effect of metal coverage and BSF thickness on Voc.

Subtask 2.3: Metallization

Plating resulted in lower, consistent R_{series} (Series Resistance) due to lower contact and line resistance compared to metal fired process as shown in Figure 10. Hence etch paste and plating based metallization scheme was chosen for our cells. Plating also results in more consistent Voc, Jsc and FF values. Typical Voc, Jsc and FF values for a lot are given in Figures 11, 12 and 13.

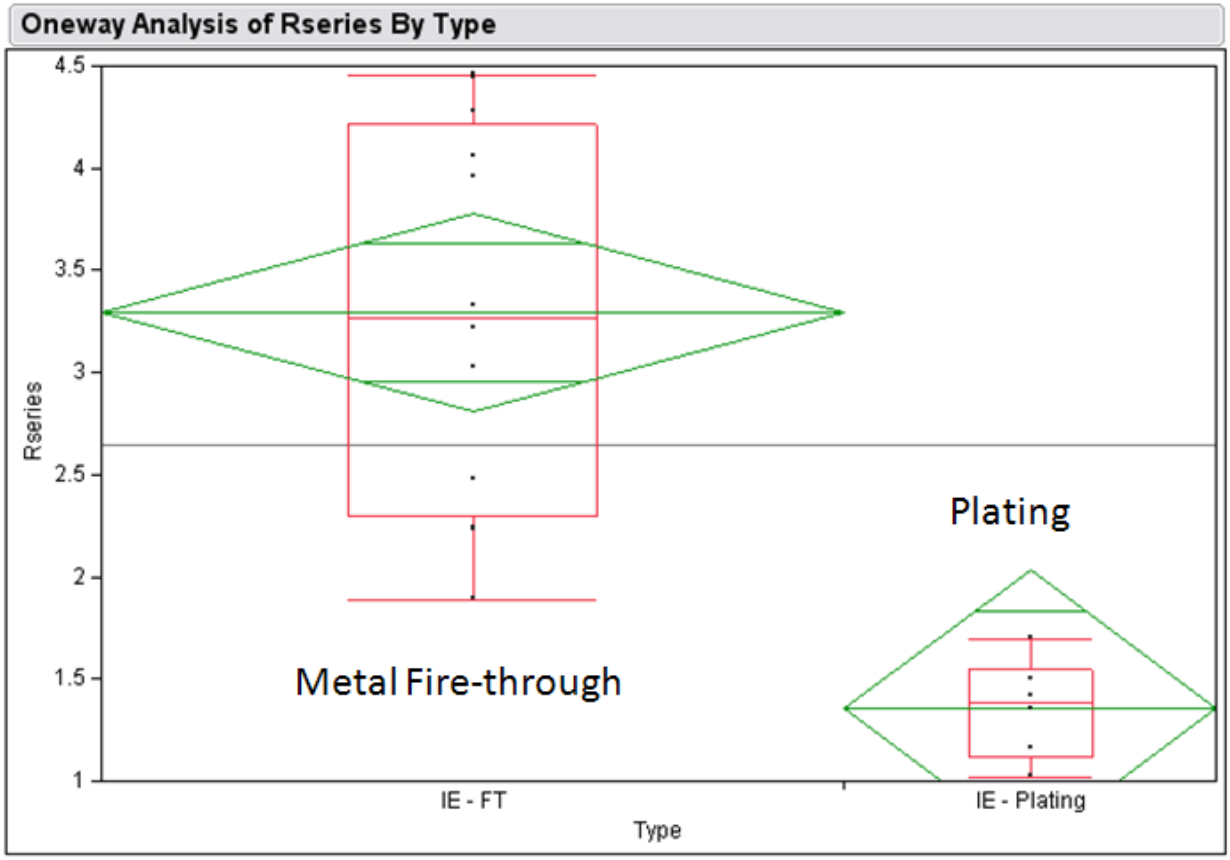


Figure 10. R_{series} with metal fire-through and metal plating.

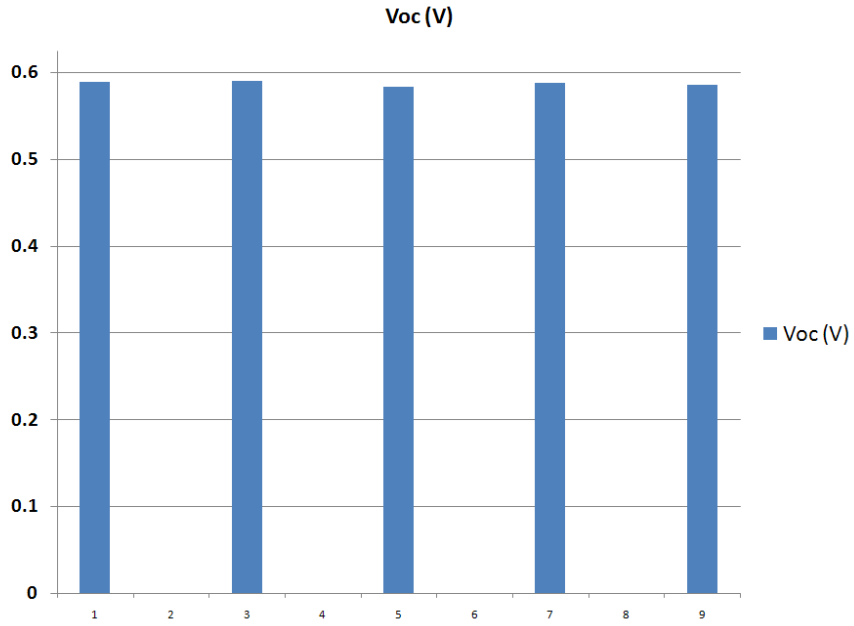


Figure 11. Voc (on y-axis) of a plated PV cell lot (on x axis).

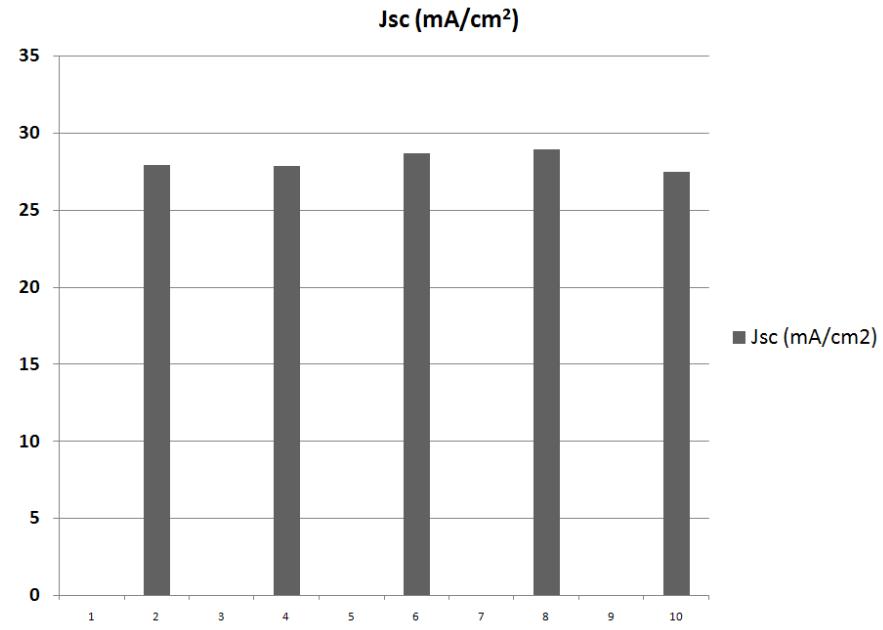


Figure 12. Jsc (on y-axis) of a plated PV cell lot (on x axis).

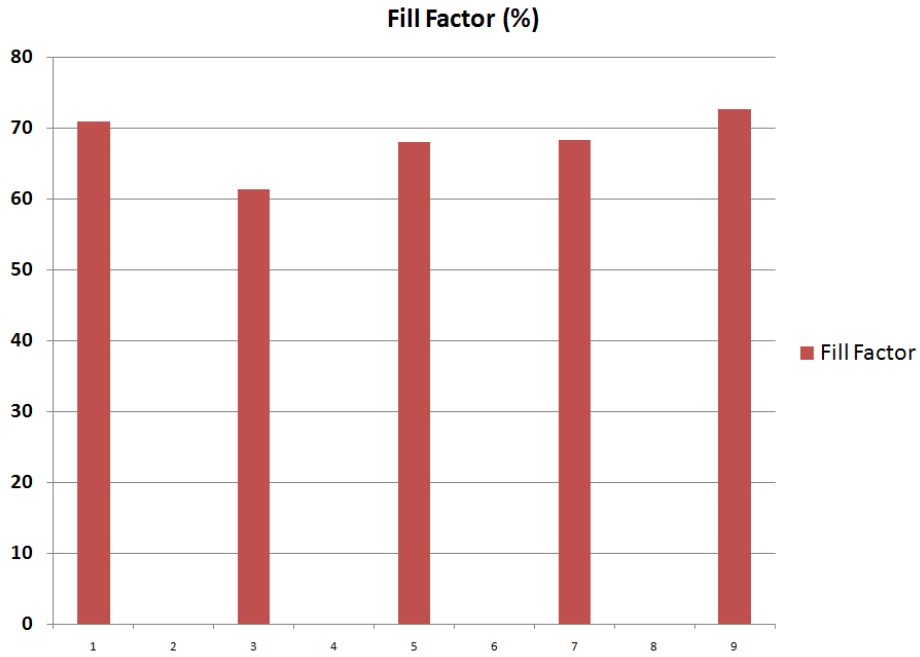


Figure 13. FF (on y-axis) of a plated PV cell lot (on x axis).

Task 3: Cell Efficiency Increase

In order to increase cell efficiency, the approach was to develop the processes on 125X125mm CZ wafers and then transfer the processes to 125X125mm TFSS. Then the substrate size was

scaled to final 156X156mm TFSS. Figures 14 and 15 show a 125X125 TFSS cell from the front-side and the backside.

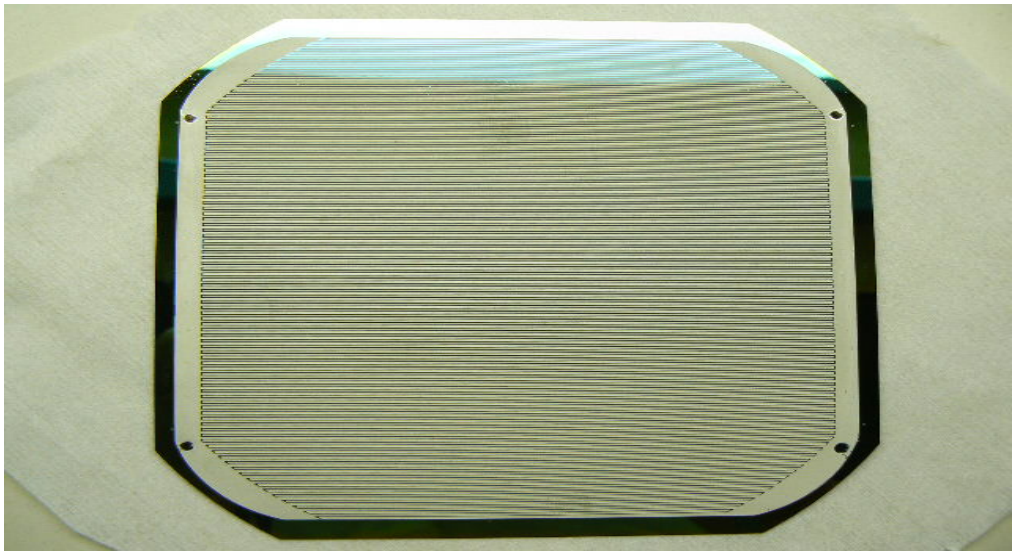


Figure 14. Backside of a TFSS cell. The emitter and base busbars are located at the edges with interdigitated fingers collecting the current.

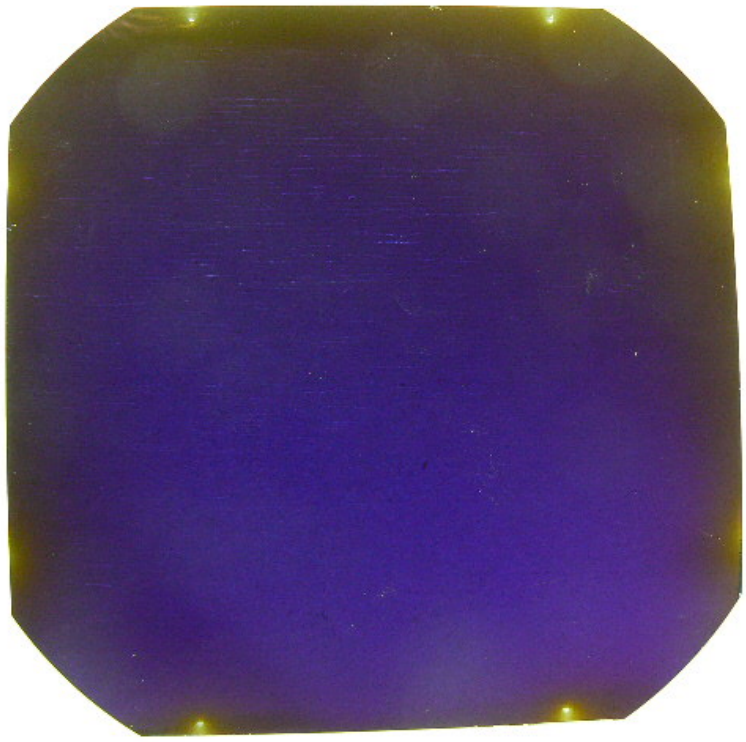


Figure 15. Frontside or sunnyside of a TFSS cell.

The IV curve for a 17.69% efficient CZ cell is presented in Figure 16 and 15.8% efficient TFSS cell is presented in Figure 17. Process and cell design improvements are being implemented to improve the FF and Voc of the cells produced using the process modules and flow described above. IQE for a CZ cell and a TFSS cell is presented in Figure 17. Lifetime for the CZ cell is higher than for the TFSS cell as can be seen from the slope of the IQE.

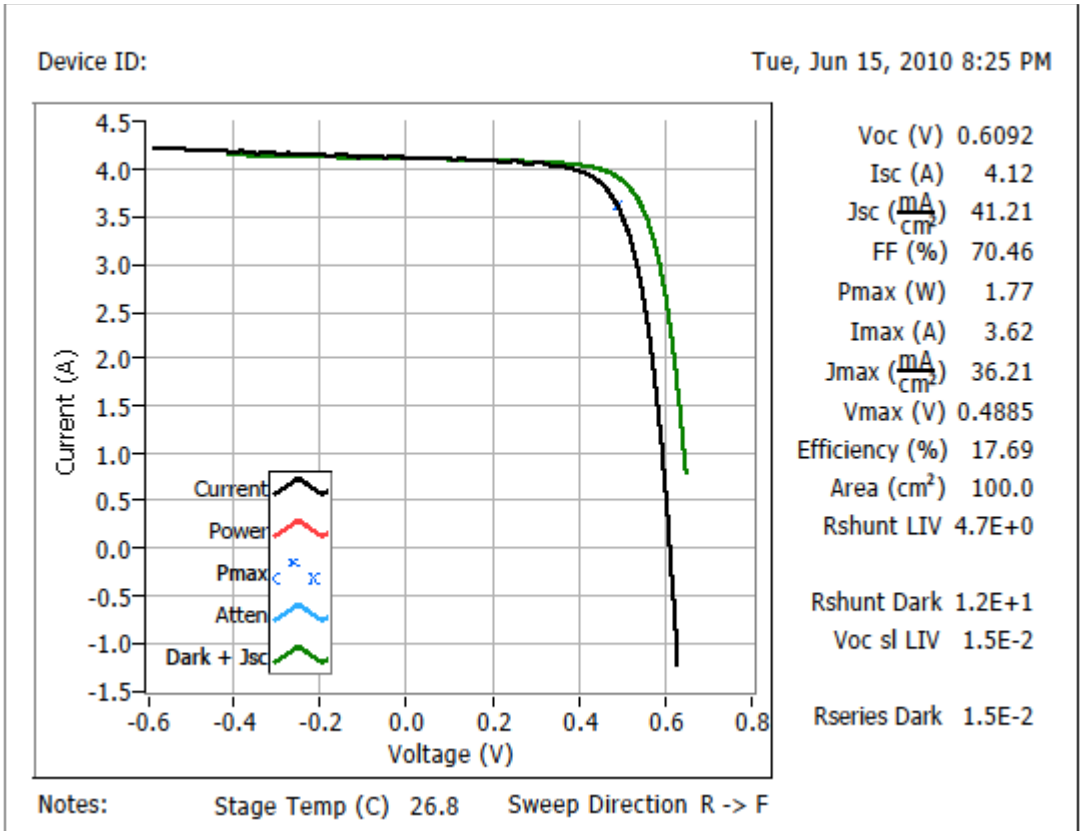


Figure 16. IV curve of a 17.69% efficient CZ cell. Rseries is higher than target for this cell, leading to depressed FF. Attenuated IV curve and power curves were disabled during testing.

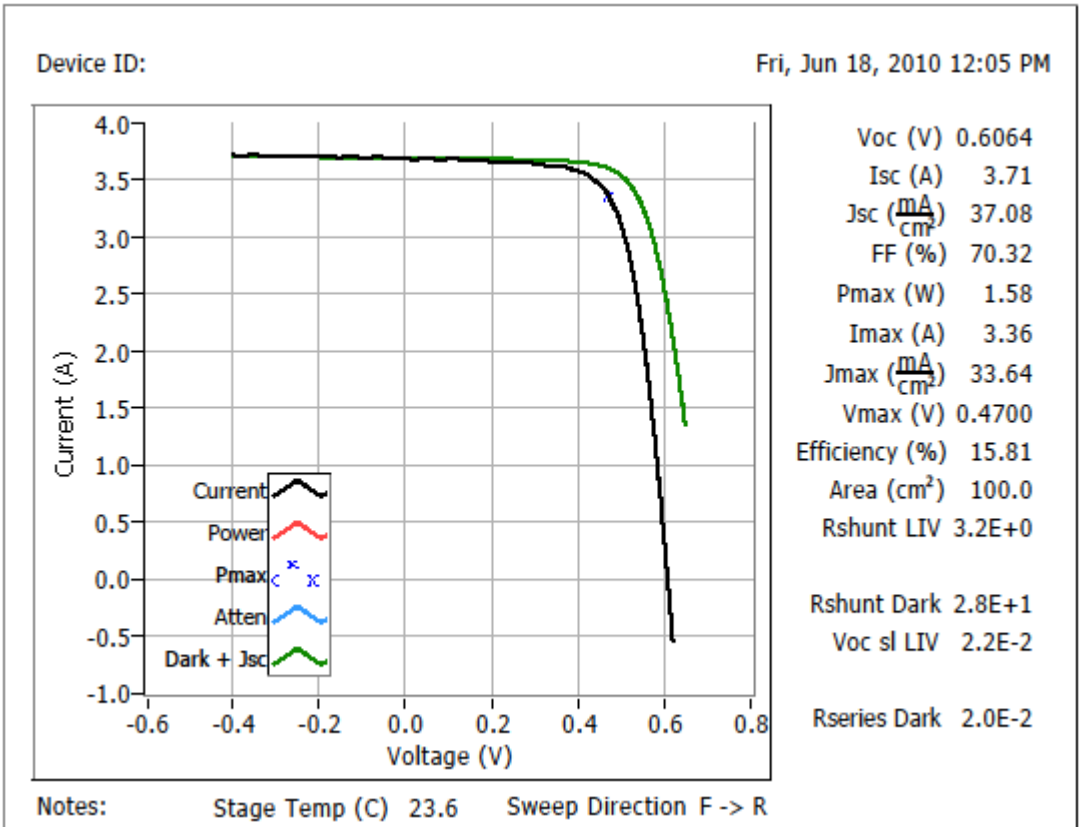


Figure 17. IV curve of a 15.81% efficient TFSS cell. Rseries is higher than target for this cell leading to depressed FF. Jsc is also lower due to lower lifetimes in TFSS compared to CZ. Attenuated IV curve and power curves were disabled during testing.

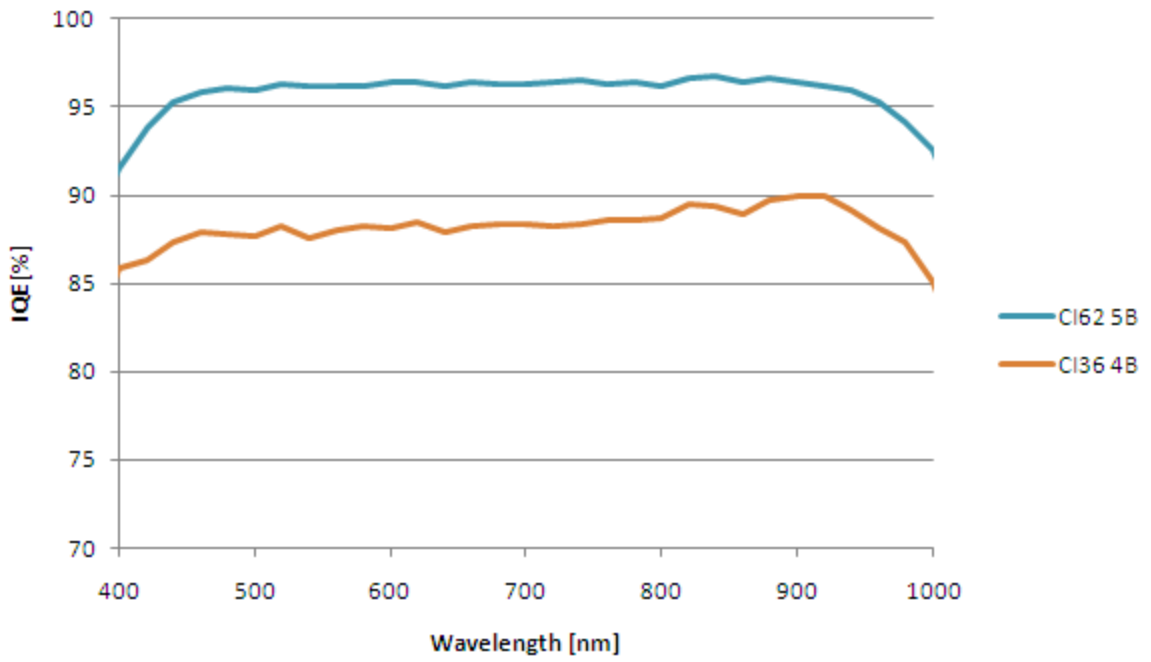


Figure 18. IQE of CZ cell (in blue) compared to the TFSS cell (in orange). Difference in the slope due to differences in the lifetime was noted.

The substrate size was then scaled to final 156X156mm TFSS with 192 circle trim on the corners as shown in Figures 19 and 20. The IV curve of a 156X156 cell is shown in Figure 21 indicating a cell efficiency of 15.23%. The same cell was measured at NREL but at ~ 0.8% absolute lower cell efficiency with Voc = 0.6133 V, Isc = 8.0562 A, Jsc = 34.282 mA/cm2, Fill Factor = 68.51 % Imax = 6.9459 A, Vmax = 0.4873 V, Pmax = 3.3849 W yielding a cell efficiency of 14.40 %. However, when adjusted for correction factor due to shading and factoring in the 3% uncertainty window, two out of five cells (Cell #1 and Cell #11) passed the required mark of 15% efficiency as shown in Table 2 below.

Table 2. Solexel Cell Data Measured at NREL and Adjusted for the Difference in Shading Between the NREL Method Used on August 13th 2010 and One Used on September 8th 2010

	Cell #1	Cell #11	Cell #12
Aug. 13 Isc (A)	8.1715	8.2596	8.0613
Sep. 8 Isc (A)	7.9930	8.0562	7.9002
Ratio	**1.0223**	**1.0252**	**1.0204**
Sep. 8 Pmax (W)	3.3676	3.3849	3.3320
Adjusted Pmax (W)	3.4428	3.4704	3.3999
Adjusted Eff.	**14.65%**	**14.77%**	**14.47%**

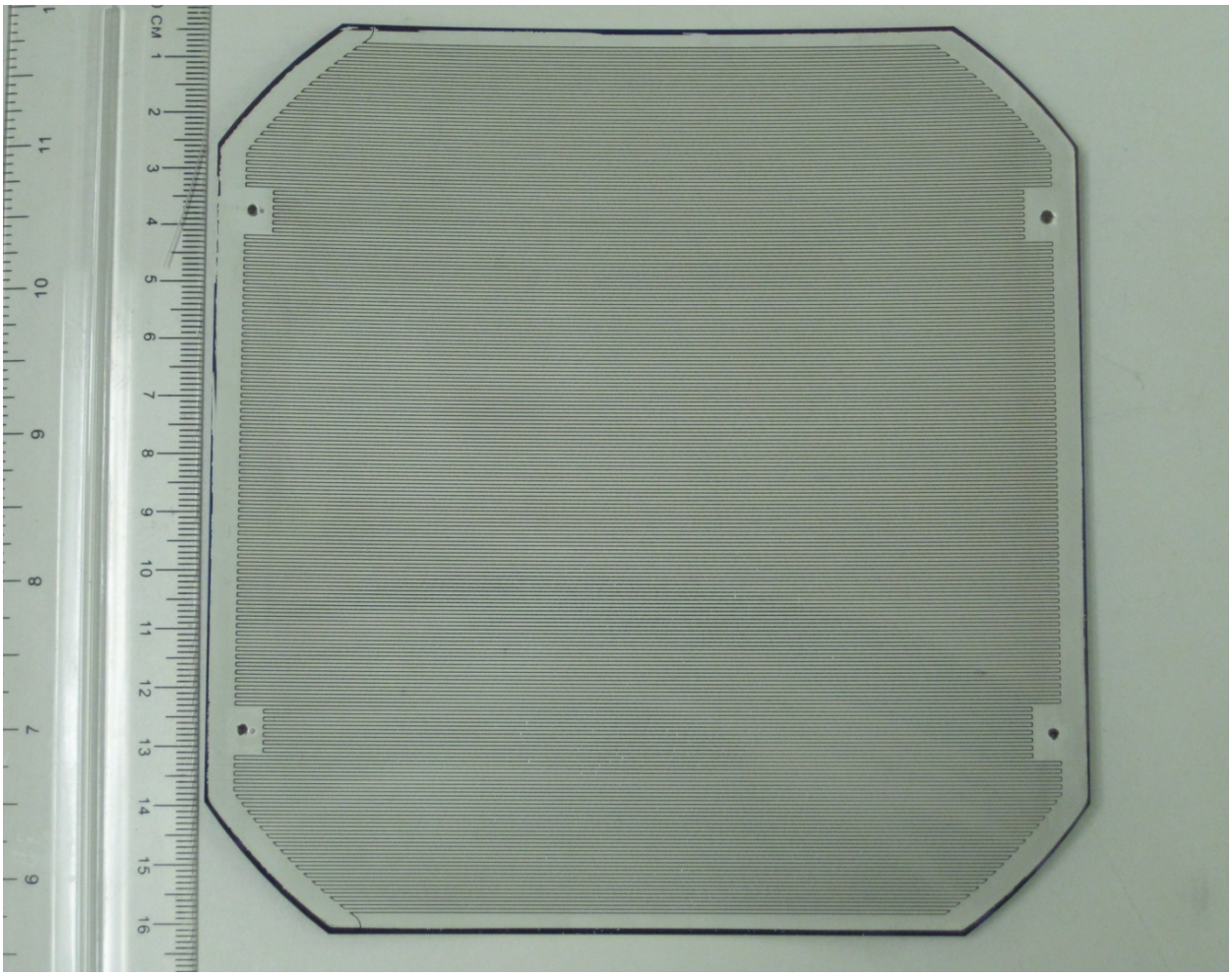


Figure 19. Backside of a 156mmX156mm TFSS cell. The emitter and base busbars are located at the edges with inter-digitated fingers collecting the current.

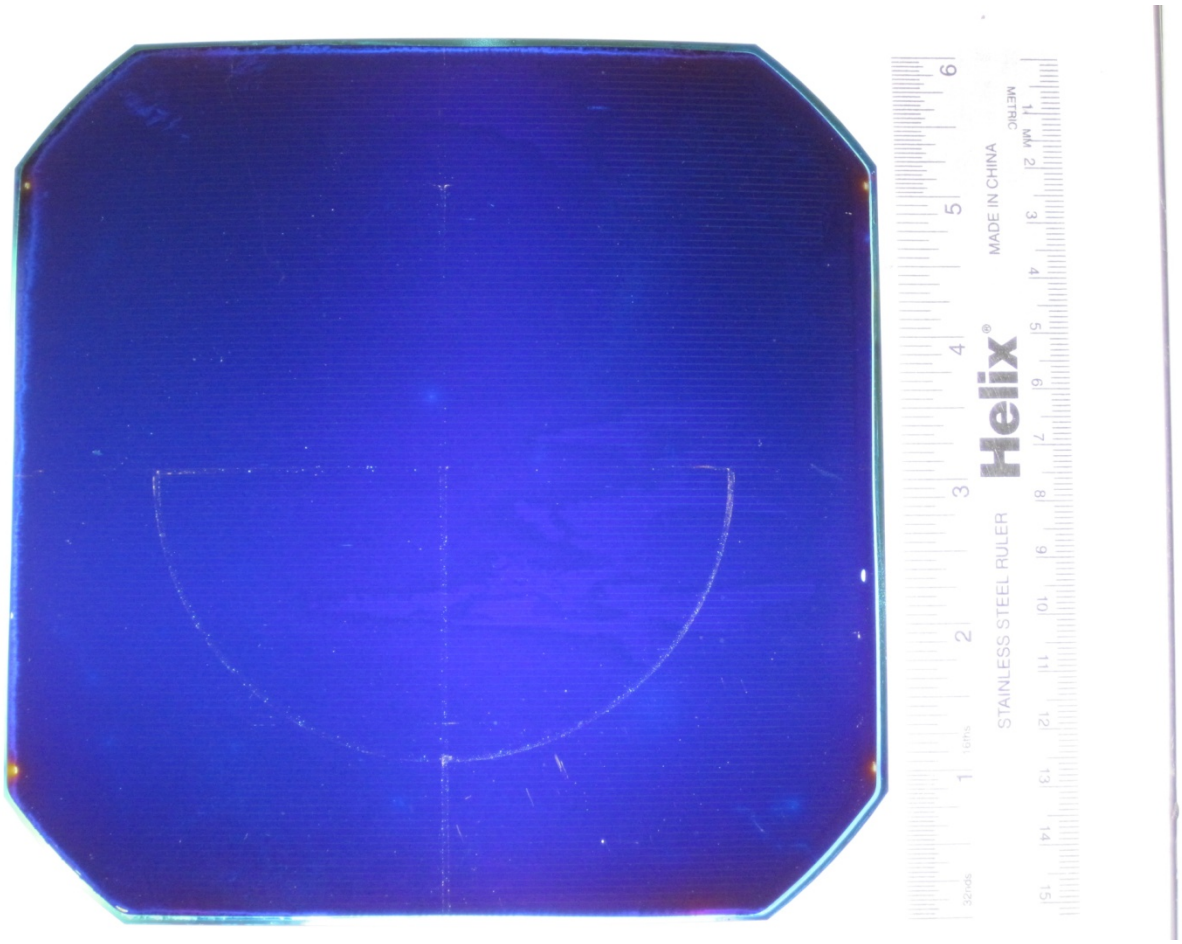


Figure 20. Frontside or sunnyside of a 156X156mm TFSS cell. Laser marks can be seen on the front-side and a newer process flow that does not result in the laser marks on the front-side is being implemented to increase Jsc.

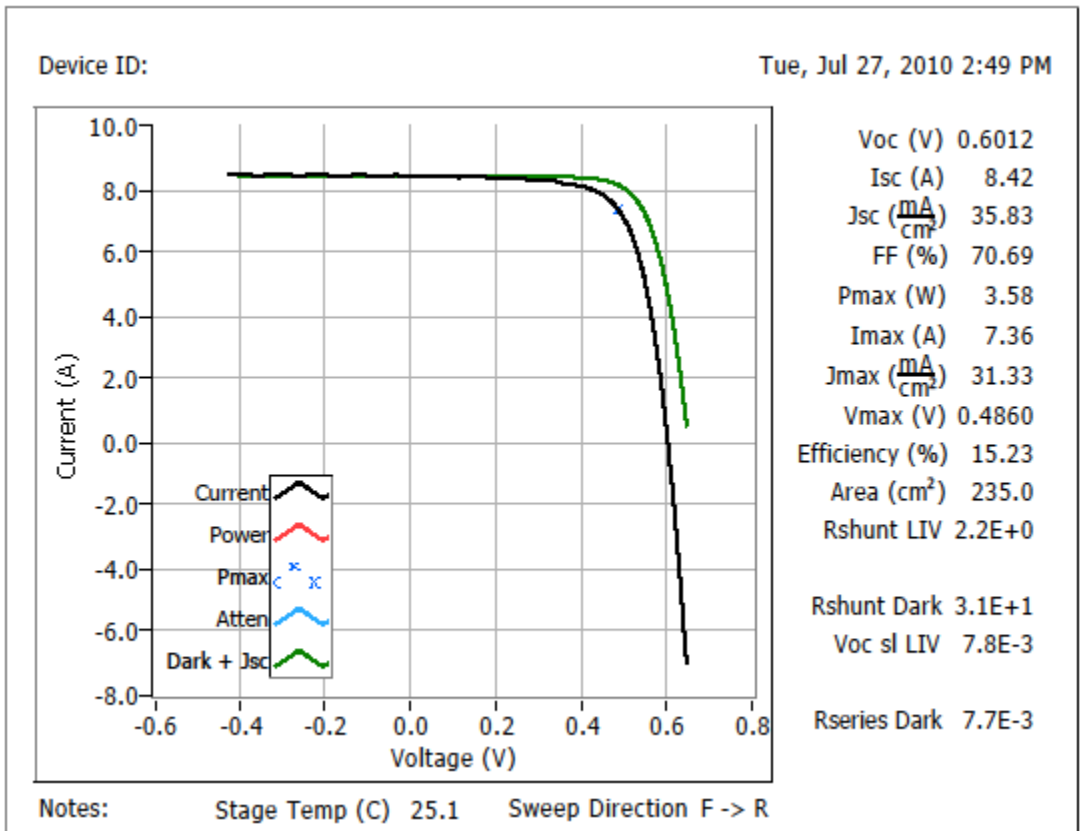


Figure 21. IV curve of a 15.23% efficient TFSS cell. Jsc is lower due to lower lifetimes in TFSS compared to CZ. Attenuated IV curve and power curves were disabled during testing.

Task 4: Module Assembly Development

Subtask 4.1: Evaluate Methods of Tabbing, Encapsulating

This subtask can be grouped in two main categories:

1- Cell robustness and handling

2- Soldering compatibility

Cell Robustness and Handling:

The break force strength of the TFSS has been evaluated using a 3-point bend technique (Figure 22) which has been shown to stress both the bulk and edge of the sample. The samples are broken into approx 40mm square pieces from within a 125mm wafer, thereby revealing both edge engineering factors in addition to the geometry of the sample.

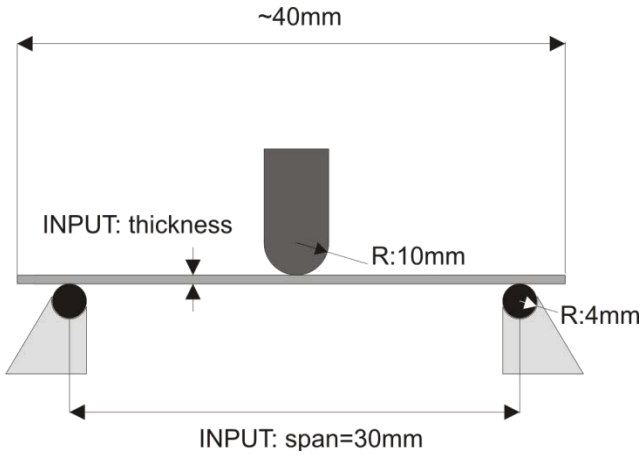


Figure 22. 3-point bend setup for cell fracture strength characterization.

For a given material, fracture strength [σ] and the absolute force per unit width [F/w] that can be withstood by the sample is given by Equation 1. The break force is proportional to the square of the material thickness (d) which explains the increasing challenges of wafer breakage as the thickness of the material decreases. Table 3 shows the 3-point and 4-point fracture strength variables and their units.

$$\frac{F}{w} = \frac{\sigma_{3pt} 2d^2}{3L} \qquad \text{(Equation 1)}$$

Table 3. 3-Point and 4-Point Fracture Strength Variables

Parameter	Variable name	Units
Load	F	N
Supporting span length	L	M
Sample thickness	d	M
Sample width	w	M
Displacement	D	M

There is no standard requirement for the fracture strength of a solar cell that can be used to determine if a substrate will have sufficient strength to withstand processing, assembly into a module and outdoor exposure for up to 25 years. Furthermore, given the unique topography of the TFSS, the application of such a standard to a three dimensional substrate would require validation. Nevertheless, some target values can be set by assuming that a conventional solar cell of a given fracture strength meets these robustness requirements and that a new cell technology should be able to withstand the force and deflection experienced by such a cell during bend test measurements. For a conventional 200um starting wafer with fracture strength of 200MPa, the break force per unit length F/w is 1.8N/cm which is currently the target specification for substrate strength.

For the flexure break strength measurements, an Instron Model 5543 universal tester with a 1KN load cell accurate to ±0.5% at 4N load was used. The 3-point bend fixture available (model number 2810-400) was fitted with 4mm radius bottom supports and a 10mm bend radius top load as shown in Figure 22 with a default span of 60mm. The span width is much larger than that required to ensure that the thickness of the material can be neglected but allowed comparison to historical data for mono-crystalline strips measured with the same equipment and span. As shown in Figure 23, the median fracture force of the TFSS PyCell is 0.39N/cm which is significantly below the break force specification of 1.8N/cm [note the measured median break force of a conventional c-Si solar cell of 1.75N/cm].

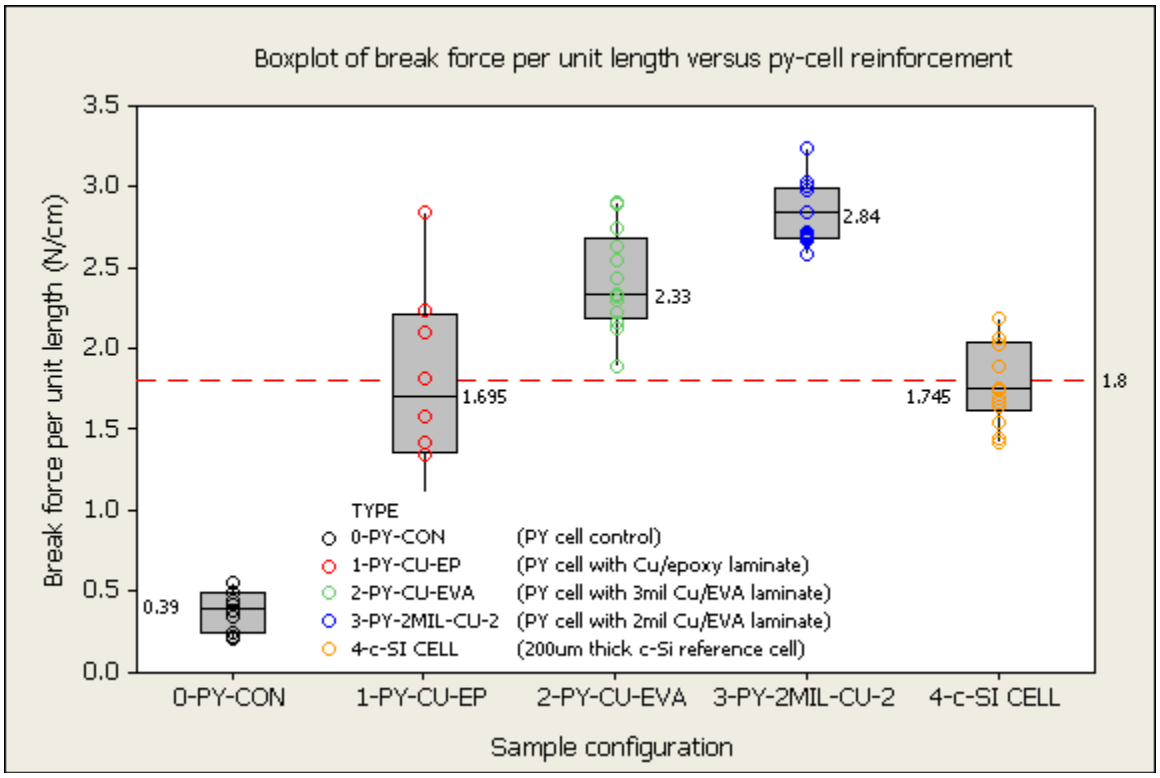


Figure 23. Boxplots of break force versus PYCell reinforcement scheme.

Soldering compatibility:

The interconnect quality for both contact soldering and conductive epoxy has been evaluated through solder pull strength measurements with conventional solder coated copper ribbon as shown in Figure 24. The force versus displacement curves are shown in Figure 25 for contact soldering pre- and post- 100 cycles from -40°C to 85°C and for silver conductive epoxy as cured. TC100 represents the 100 temperature cycle data. For all other cases, the data is initial (i.e. no temperature cycling). FS and RS refer to front-side and rear-side per Table 4.

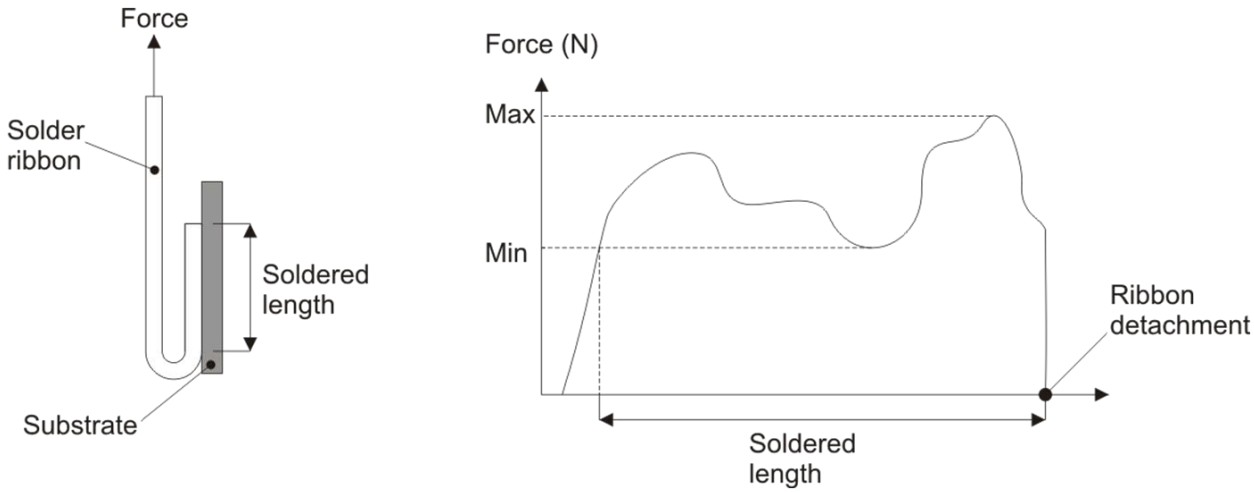


Figure 23. Ribbon pull strength measurement configuration.

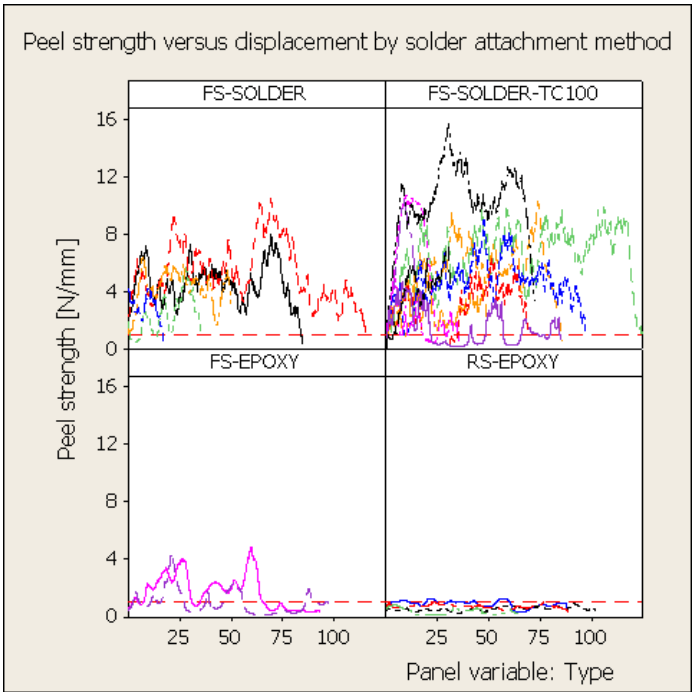


Figure 24. Ribbon pull strength by displacement and ribbon attachment method.

The probability plots for each configuration are shown in Figure 25 compared to the Solexel internal specification of 1N/mm. A probability plot is a way to determine the percentage of data above (or below) a certain value. The upper 90th percentile refers to the value at which 90% of the data is above a value x. In the case of pull strength, it would mean that 90% of the length of the solder pad had a pull strength above x N/mm. In the probability plot in Figure 25, the row order matches that of the legend key (it's specific to the stats package so there isn't an option to label both). CL is the confidence level for the fit to a normal distribution. N is the number of samples, AD is the Anderson-Darling coefficient and P is the p-value to check for normality (if

the value is below 0.05 it means that the data is not a good fit to a normal distribution). Table 4 summarizes the ribbon pull strength statistics which showed that contact soldering is able to achieve pull strengths of 2.2N/mm [upper 90th percentile] beginning-of-life [BOL] and 1.0N/mm [upper 90th percentile] after 100 cycles from -40°C to 85°C.

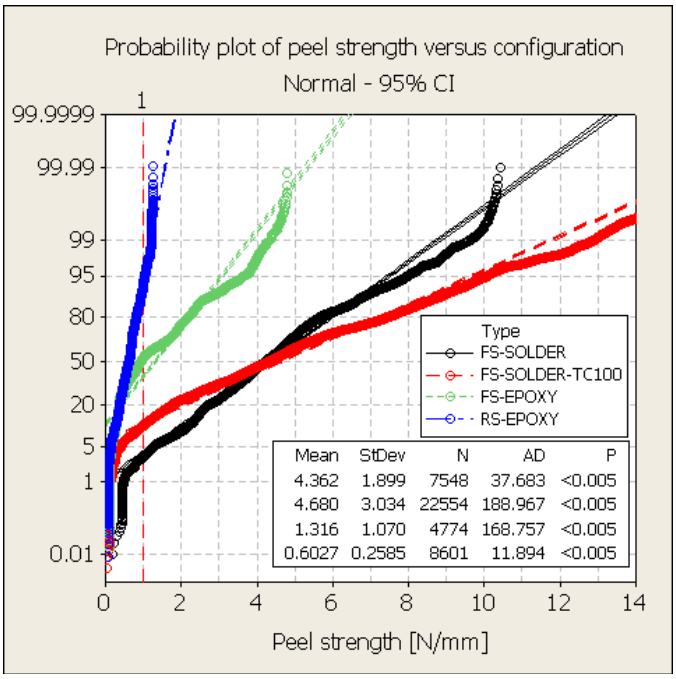


Figure 25. Probability plots of peel strength versus configuration.

Table 4. Ribbon Pull Strength Data Summary

Configuration	Sample size	Mean [N/mm]	90th percentile [N/mm]
Front side, soldered	5 busbars	4.4	2.2
Front side, soldered TC100	6 busbars	4.7	1.0
Front side, epoxy	2 busbars	1.3	0.3
Rear side, epoxy	4 busbars	0.6	0.3

Subtask 4.2: Characterize Mini-Module Reliability

Module Performance

In early phase of the project Solexel fabricated a 2x2 module from the first four front contact plated PyCells. Interconnect was standard solder coated copper ribbon with conventional low iron front glass, EVA encapsulation and TPE backsheet as shown in Figure 26. The associated I-V curve from the module is shown in Figure 27 with a measured module efficiency of 6.1%. The angular dependence of J_{sc} for the module was compared with that of a crystalline silicon

module to determine any differences in light capturing capability and showed a performance match within 5% which was within the measurement error (Figure 28).

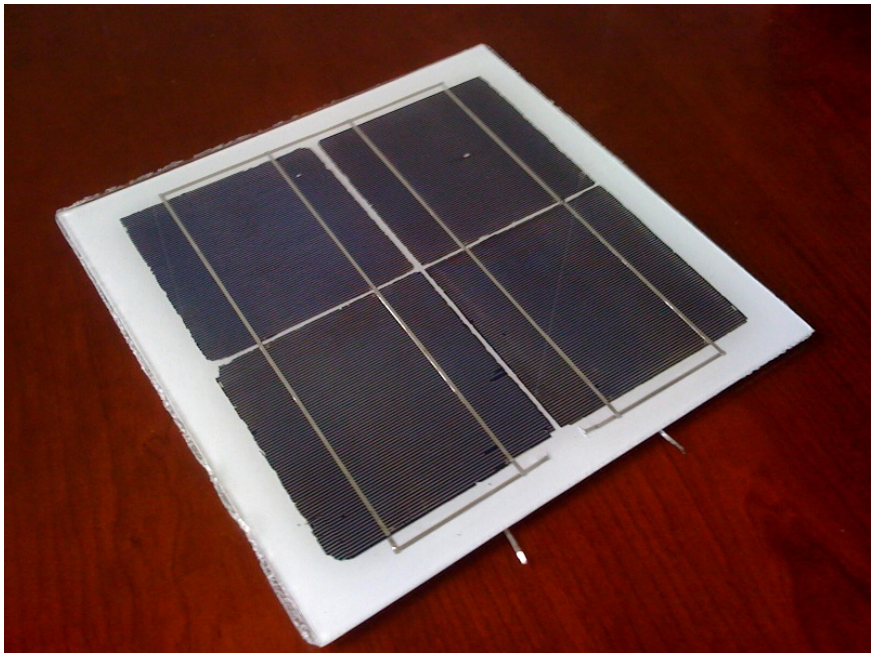


Figure 26. 2x2 plated PyCell module.

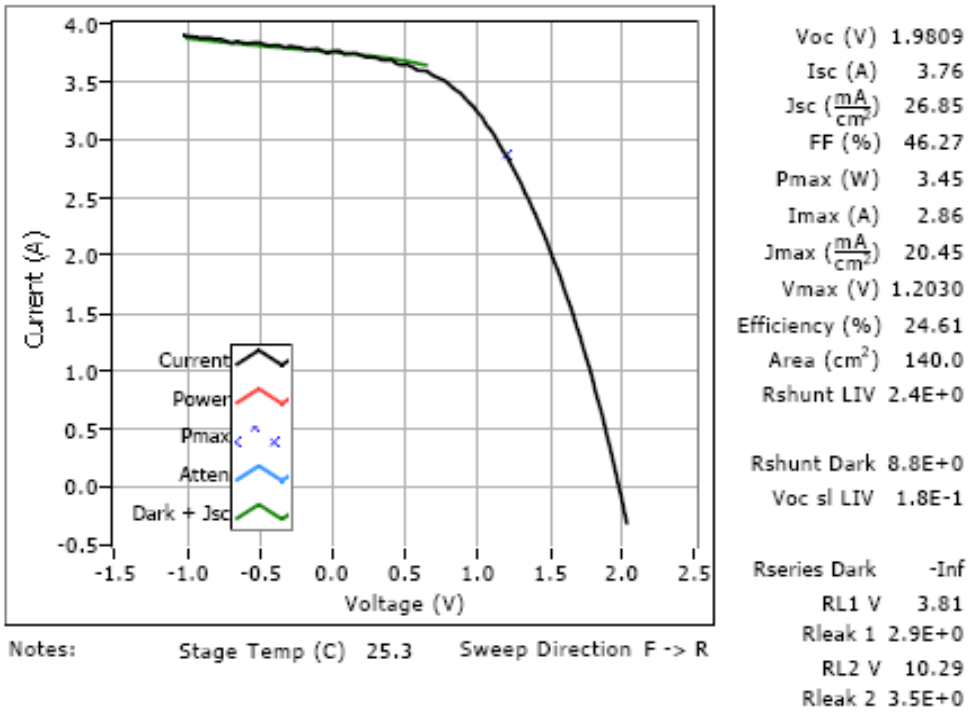


Figure 27. I-V curve for 2x2 plated module (Efficiency is 24.61/4=6.1%].

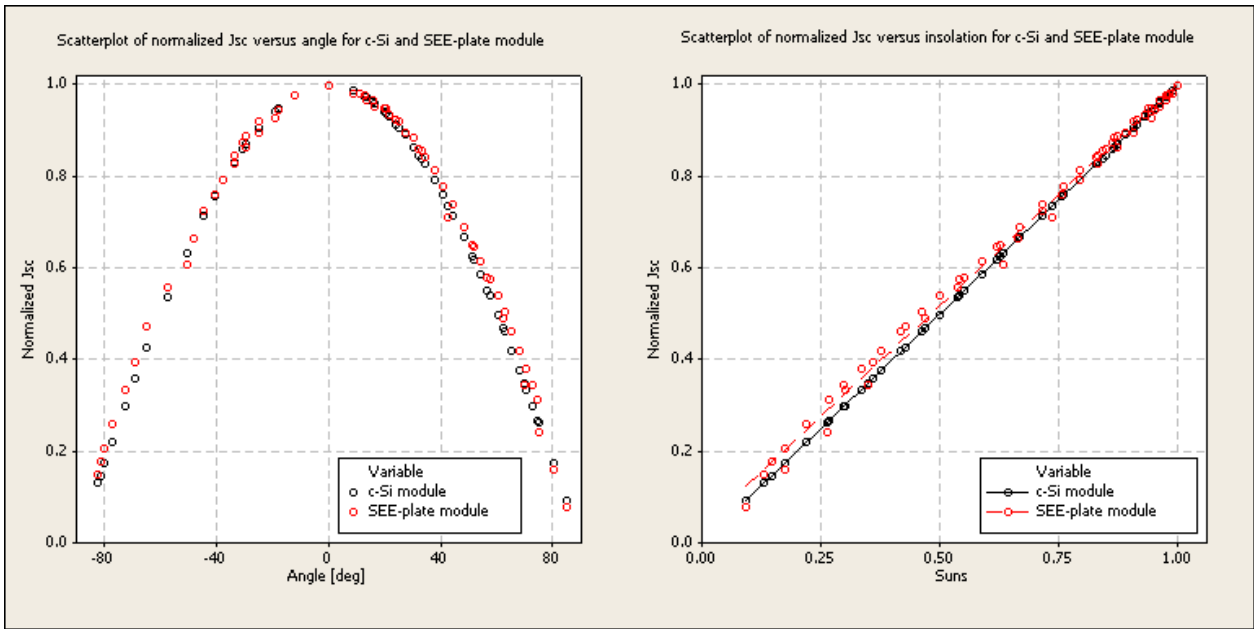


Figure 28. Comparison of normalized J_{sc} performance between Solexel plated cell module and standard c-Si module (SEE plate stands for "Selective Epitaxial Emitter").

Subtask 4.3: **Module Assembly / Reliability**

Testing to failure was performed on cells processed with the TFSS cell flow on CZ wafers to evaluate any device related failure modes. Four accelerated tests were populated with four 2x1 modules built using 125mm pseudo square back contact cells as summarized in Table 5. A typical electroluminescence image of a module pre- and post-lamination is shown in Figures 29 and 30. Scatterplots charting the percentage change in module power as a function of duration are shown in Figures 31 to 34. Each curve represents one of the four units in each test.

For humidity exposed modules (HAST and damp heat), sodium leaching was observed from the glass causing pitting of the glass surface and a drop in short circuit current. For humidity freeze, a malfunction in the chamber caused an over-temperature to 150C for 50hrs at HF-12 which induced defects in the EVA for module 12 causing a significant drop in power. For thermal shock, the power remained stable and within the 5% range beyond 1000 thermal shocks in comparison to the IEC61215 requirement of 200 cycles.

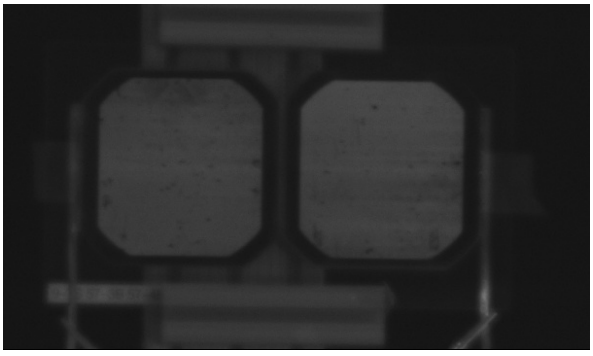


Figure 29. Image of module SXL-2x1-TS-9 pre-lamination.

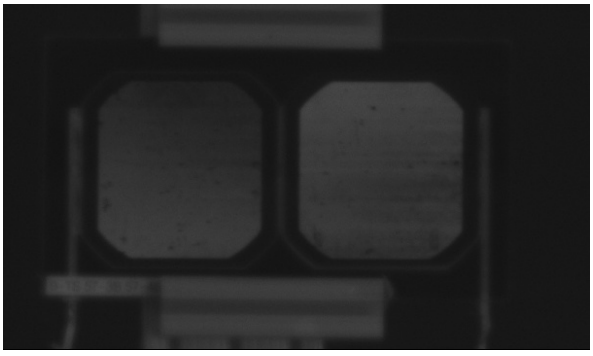


Figure 30. Image of module SXL-2x1-TS-9 post-lamination.

Table 5. Test Matrix for 2x1 TTF (Test to Failure)

Test name	Condition	Duration	No. of units
Damp heat	85C/85%RH	1000hrs	4
Thermal shock	-40C to 90C	1000 cycles	4
Humidity freeze	85C/85%RH to -40C	20 cycles	4
HAST	120C/95% RH	600hrs	4

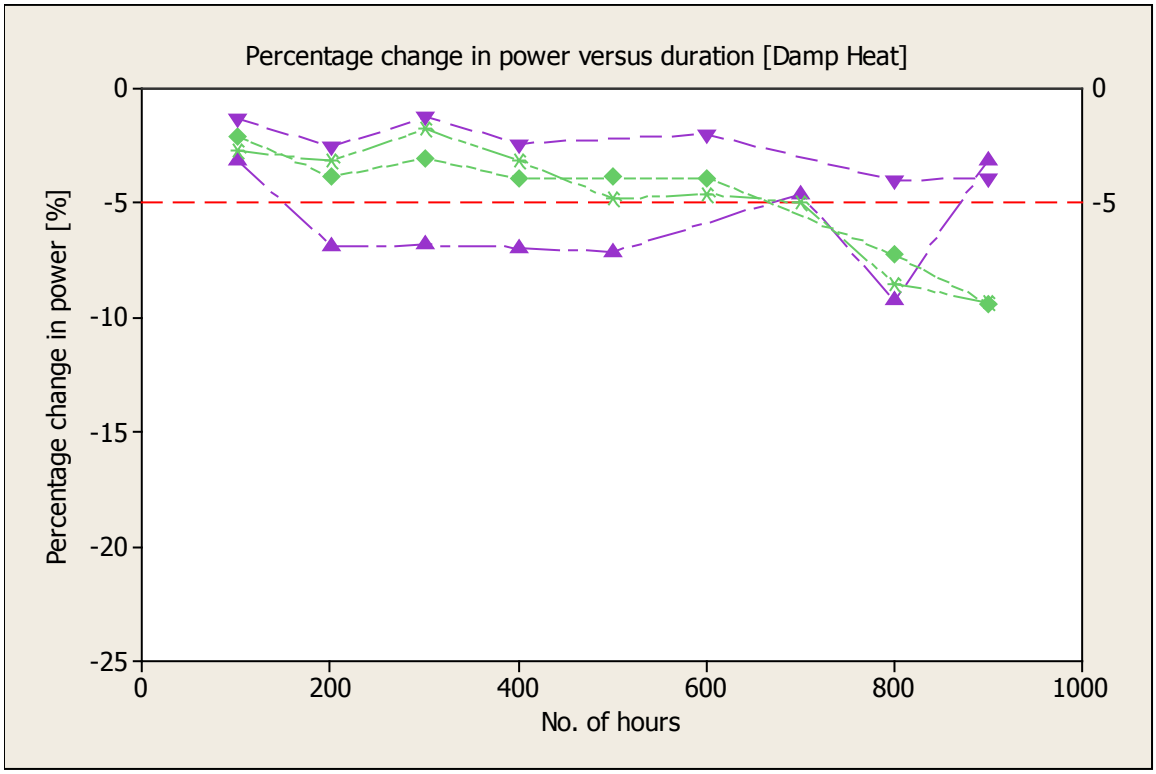


Figure 31. Percentage change in power versus no. of hours in damp heat (85C/85% RH).

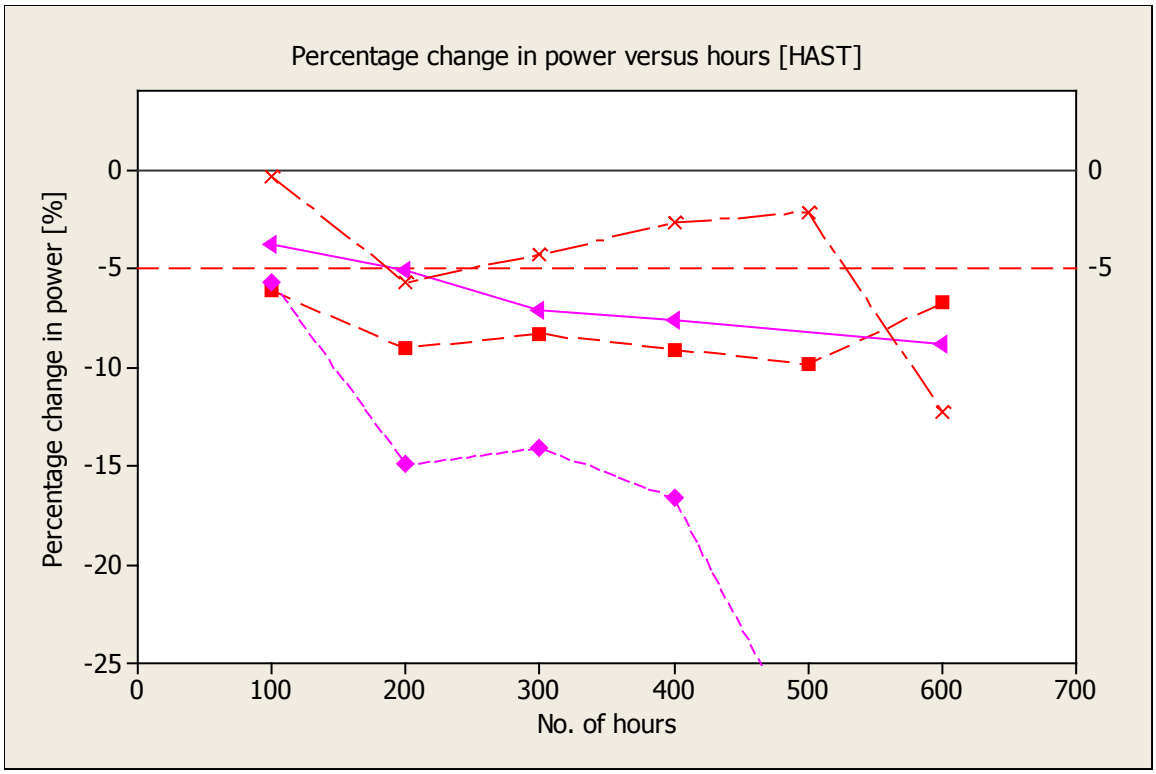


Figure 32. Percentage change in power versus no. of hours in HAST (120C/95%RH).

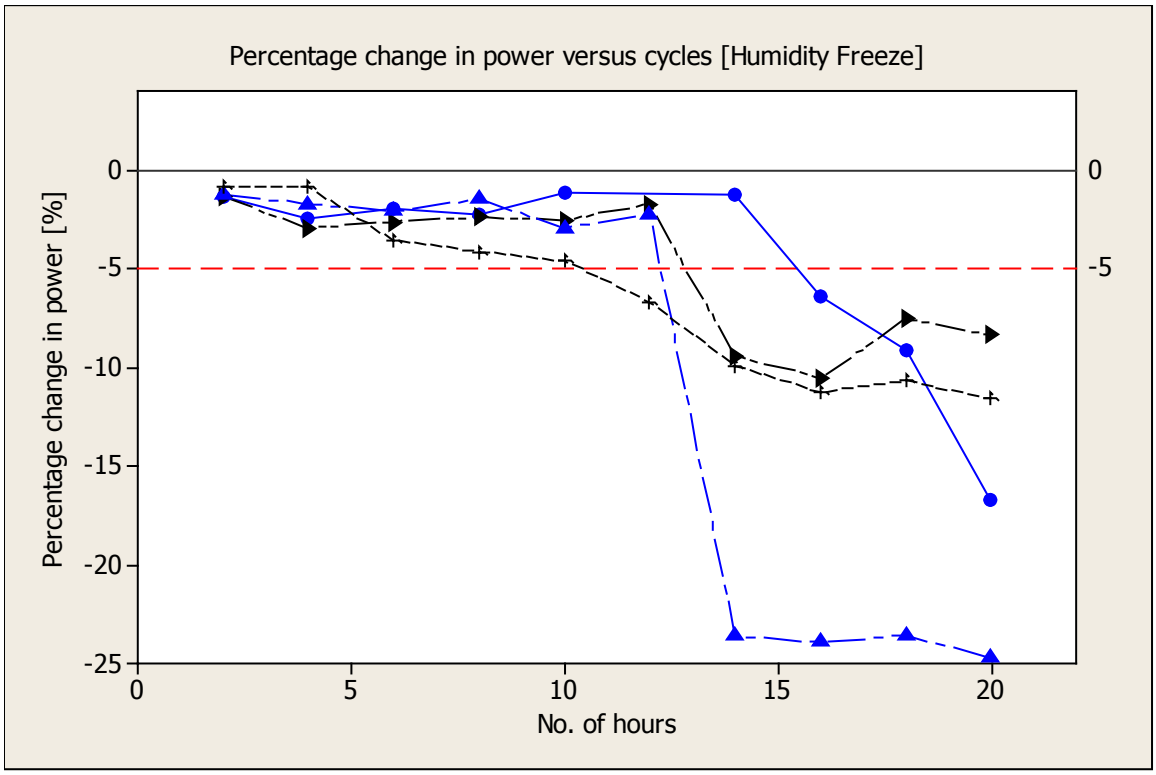


Figure 33. Percentage change in power versus no. of cycles in humidity freeze.

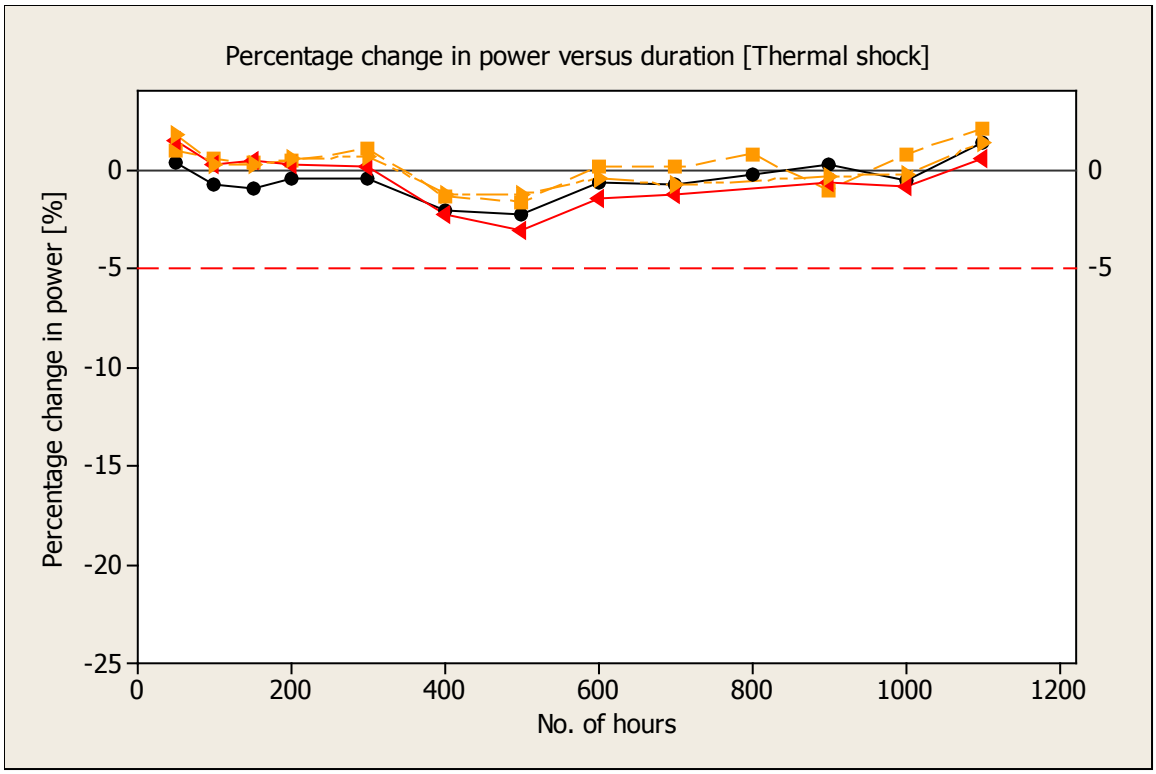


Figure 34. Percentage change in power versus no. of thermal shocks.

Finally a 5x6 module with 90um 156mm pseudo-square TFSS cells assembled using conventional solder-coated copper tab interconnects and encapsulation was submitted for temperature cycle testing at TUV-Rheinland in Arizona. The 2.6ft x 3.1ft module (8ft.sq approx.) was subjected to 200 cycles of thermal cycling from -40C to 90C per the requirements of IEC61215 at 10 cycles per day. The performance of the module pre- and post- lamination as measured at Solexel and TUV-Rheinland is shown in Table 6 below. The module efficiency pre-lamination was 11.8% and 11.1% post lamination as measured at Solexel and 10.4% as measured at TUV-Rheinland (including connectors). After 200 temperature cycles, the module power had dropped by only 3.1% satisfying the performance requirements for IEC61215 per the deliverable. The performance at interim readouts is plotted in Figure 35. After 138 cycles, the module was damaged due to a handling issue in the chamber but nevertheless still passed the IEC requirement confirming the robustness of the design.

Table 6. 5x6 Module Performance Pre- and Post-Lamination and After TC-200

Condition	Power [W]	Vmp [V]	Voc [V]	Imp [A]	Isc [A]	FF [%]
Pre-lamination @ Solexel	95.8	13.83	17.86	6.92	8.16	65.7%
Post-lamination @ Solexel	90.1	14.05	17.78	6.41	7.64	66.3%
Post-lamination @ TUV-Rheinland	84.1	13.4	17.9	6.27	7.47	62.9%
TC-200 @ TUV-Rheinland	81.4	13.4	18.0	6.09	7.29	61.9%

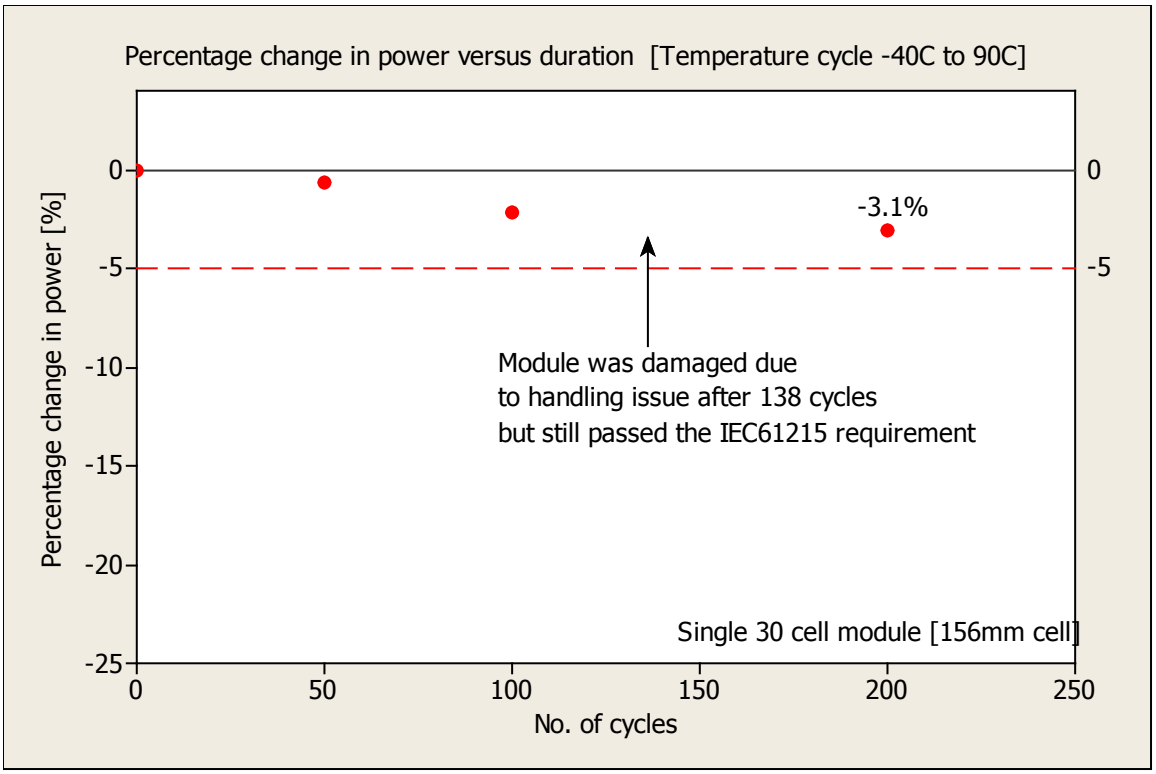


Figure 35. Percentage change in power versus no. of temperature cycles [IEC61215].

Task 5: Pilot Fabrication Development and Low-Volume Production

Solexel started a pilot fab in Milpitas, CA. Pilot fab capacity continued to increase by staffing to cover the process shifts as well as purchasing the necessary tools. The sacrificial layer and epi capacity currently determine the fab capacity as released substrates are supplied to cell processing. In addition to the sacrificial layer tool, Solexel built a batch epitaxial silicon tool. The batch epi tool at Solexel Pilot Fab runs 7x24 to maximize the output. Epi module was staffed to run in 4x12 hour shifts in a compressed work week format. Epi weekly capacity maps to ~20 runs/week or nearly 200 epi substrates/week.

Solexel Pilot Fab was set up for 5x24 coverage for front-end and back-end solar cell processes. These process modules were staffed to run in 3x8 hour shifts in a normal work week format. Total fab shift coverage was at >120 hours/week, for epi being 168 hours/week. Figure 36 shows the increase in staffing at Solexel Pilot Fab with the increase in epi process coverage. Capacity at Pilot Fab was at >20KW/year at targeted efficiency for 156x156 targeted size solar cells. Solexel then ordered a second Epi tool which arrived during the first week of October 2009. This second tool increased available capacity of our Pilot Fab to >50kW/year.

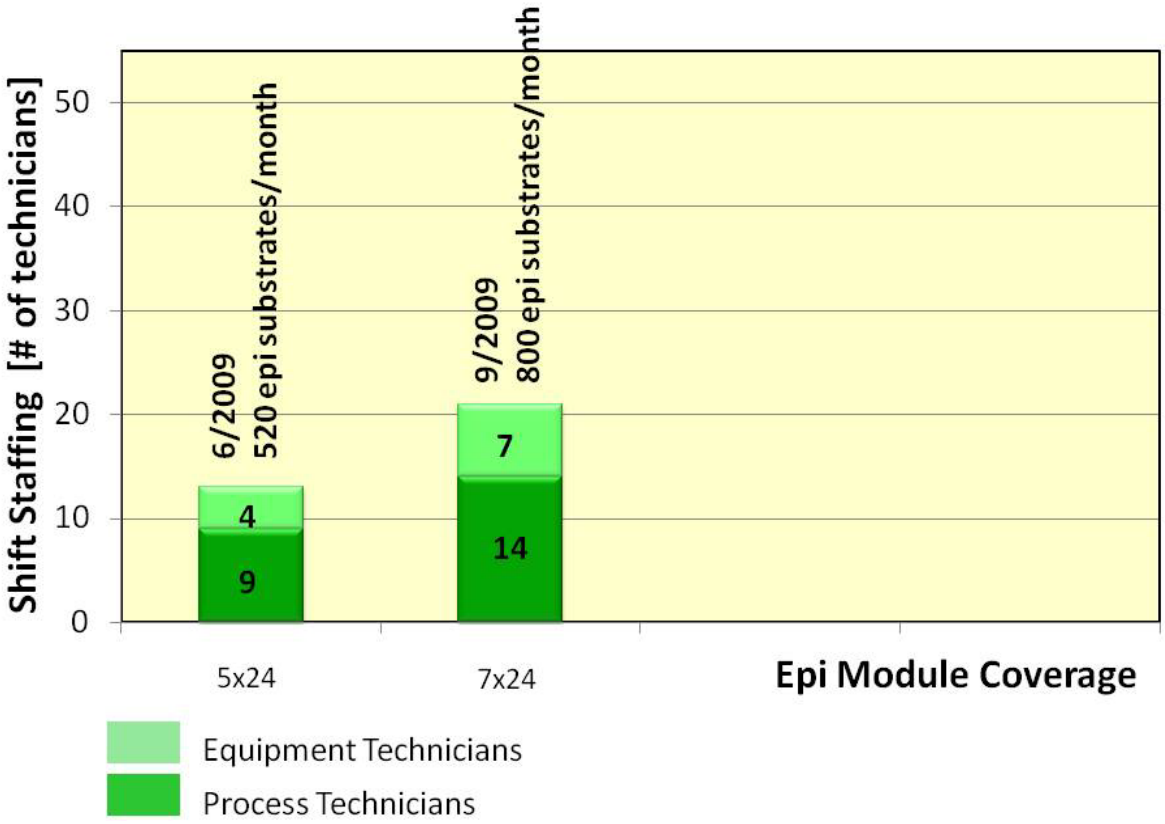


Figure 36. Increased staffing at Solexel Pilot Fab with the increase in epi process coverage.