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Required Materials Properties for High-Efficiency CIGS Modules
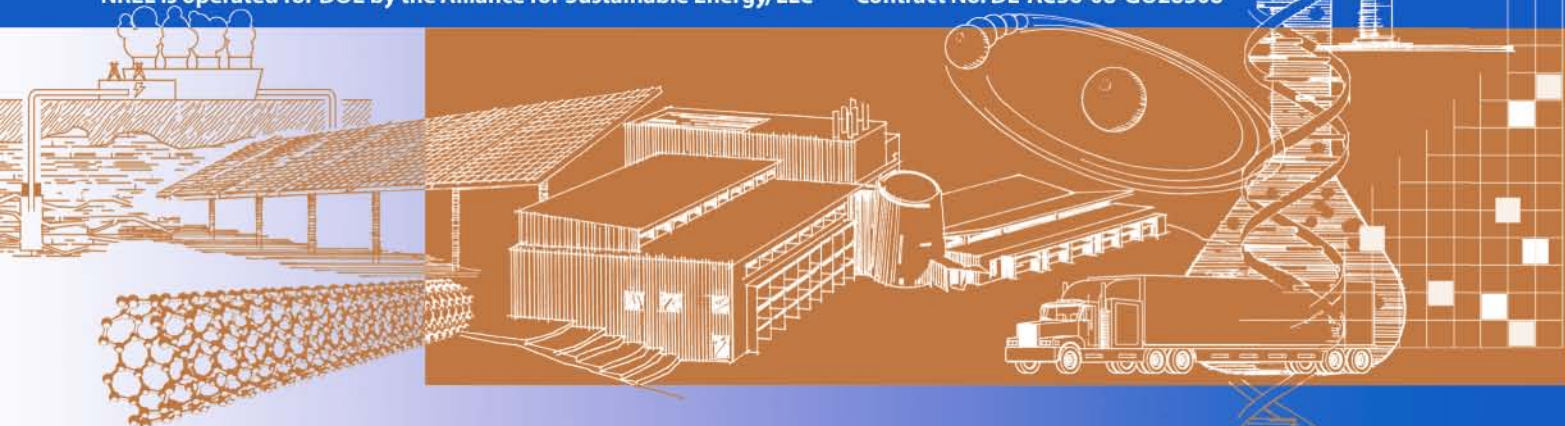
Preprint

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Required Material Properties for High-Efficiency CIGS Modules

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ABSTRACT

Relatively high proven efficiencies of CIGS devices are often cited regarding its choice as a semiconductor for photovoltaic manufacturing. Module efficiency is an important parameter, as a number of factors in the cost per watt are driven downward by increasing efficiency. Some of these factors include materials costs, throughput for a given capital investment, and installation costs. Thus, realizing high-efficiency (e.g. 15%) large-area CIGS modules is key in both reducing cost per watt and differentiating the technology from other thin films. This paper discusses the material properties required of each layer of the CIGS device such that large-area CIGS modules can achieve efficiencies 15%, which is substantially higher than the current industrial state-of-the-art. The sensitivity of module performance to the important material parameters is quantified based on both experimental data and modeling. Necessary performance differences between small-area devices and large-area modules imposed by geometry are also quantified. Potential technical breakthroughs that may relax the requirements for each layer are discussed.

Keywords: CIGS, module, material properties, photovoltaics

1. Overview of material properties

At NREL, small area CIGS device efficiencies of 20.0% have been demonstrated,[1] as shown in Figure 1. Table 1 shows measured material properties for each electrically active layer of an NREL 20% efficient device. These values will be referred to in the discussion as "best proven" values. In the following sections, each layer of the device is discussed, starting from the light-incident side. For each layer, the sensitivities of the performance to deviations from the best proven values of material properties are discussed. For critical properties, a range of acceptable values for 15% module performance is established.

2. Grids and transparent conductor

Grids and the transparent conducting oxide (TCO) must be considered together, as both are involved in lateral current collection and optimized properties are therefore interdependent. Power losses for the grid and TCO are calculated following Green.[2]

These power losses for an NREL 20.0% device are calculated and listed in the second column of Table 2. Power absorbed in the TCO, P_{TCO}, is based on measured TCO absorption (Figure 2), and is calculated by

$$P_{TCO} = V_{mp} \int A(\lambda) \, I_{AM1.5}(\lambda) \, QE(\lambda) \, d\lambda \tag{1}$$

where V_{mp} = maximum power voltage

$A(\lambda)$ = fractional absorption as a function of wavelength

$I(\lambda)$ = AM1.5 photon current per wavelength

$QE(\lambda)$ = 20% device quantum efficiency

The absorbed photon current listed in Table 1 as "ZnO bi-layer AM1.5 absorption" is simply P_{TCO}/V_{mp}.

NREL

CdS/Cu(In,Ga)Se$_2$ Cell

Device ID: M2992-11 #5   Device Temperature: 25.0 ± 1.0 °C
Oct 16, 2007 11:53   Device Area: 0.419 cm^2
Spectrum: ASTM G173 Global   Irradiance: 1000.0 W/m^2

X25 IV System
PV Performance Characterization Team
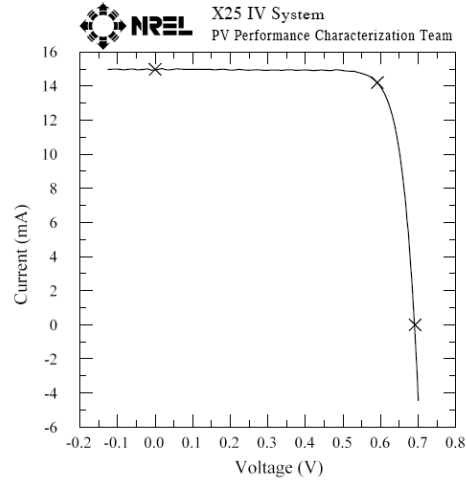
V_{oc} = 0.6918 V I_{max} = 14.20 mA
I_{sc} = 14.97 mA V_{max} = 0.5911 V
J_{sc} = 35.74 mA/cm^2 P_{max} = 8.393 mW
Fill Factor = 81.03 %   Efficiency = 20.0±0.8 %

Figure 1: JV curve of 20.0% CIGS device, using the recently-adopted standard ASTM G173 global spectrum. Note that the same device measures 19.9%, as published, under the earlier standard spectrum.

Table 1: Relevant material properties of NREL 20% device.

Layer	Property	Value	Units	Measurement Technique
Mo	Sheet Resistance	< 0.24	Ω/□	Four-point probe
CIGS	Thickness	2.2	μm	Mechanical profilometer
CIGS	Ga ratio	0.28 / 0.20 / 0.40 notch	unitless	Auger profiling
CIGS	Lifetime	~200	ns	Time-resolved photoluminescence
CIGS	Carrier density	2 x 10^{16}	cm^{-3}	Capacitance-voltage
CdS	Thickness	50	nm	Mechanical profilometer
ZnO bi-layer	Sheet Resistance	69	Ω/□	Four-point probe
ZnO bi-layer	AM1.5 Absorption	1.0	mA/cm^2	Transmission spectrophotometry
ZnO: Al	Carrier density	5.6 x 10^{20}	cm^{-3}	Hall Effect
ZnO: Al	Mobility	13	cm^2/V-sec	Hall Effect
ZnO: Al	Thickness	120	nm	Mechanical profilometer
Grid finger	Sheet resistance	0.009	Ω/□	Resistance test structure
Grid finger	Contact resistance	4.5 x 10^{-7}	Ω-m^2	Resistance test structure
Grid finger	Minimum width	45	μm	Mechanical profilometer

Reflection losses are calculated in an analogous fashion, with $A(\lambda)$ in (1) replaced by the reflection, $R(\lambda)$. Based on the reflection data of Figure 2, these losses integrate to 4.1 mA/cm^2. However, use of a MgF$_2$ anti-reflective (AR) coating increases the short-circuit current by 5% (i.e. by ~1.8 mA/cm^2), implying reflection losses are reduced to 2.3 mA/cm^2. Thus, the remaining power loss due to reflection in a high-efficiency device (coated with MgF$_2$) is approximately 1.4 mW/cm^2.
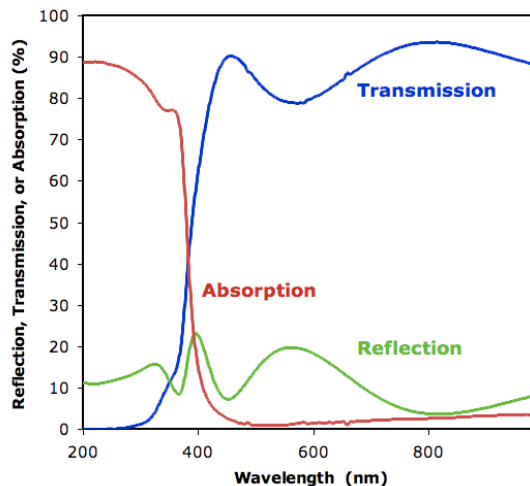

Figure 2: Measured transmission, reflection, and absorption as a function of wavelength for ZnO bilayer on glass companion piece to device M2992 of Figure 1.

When moving to a larger device size, power loss related to lateral current collection necessarily increases. However, these power losses are minimized by adjusting grid spacing, cell dimensions, and TCO conductivity and absorption (via TCO free carrier density). The necessary performance differences imposed by device size should be distinguished from processing choices made for throughput and cost advantages. For example, a manufacturer may utilize a substrate or deposition rate that has a known negative impact on absorber lifetime, but is advantageous in terms of throughput. In this paper, we only discuss material properties needed to achieve a given performance goal, independent of manufacturing trade-offs.

The geometry utilized to examine power losses for a large-area device is shown in Figure 3. A gridded, rather than monolithically-integrated, configuration is analyzed, as grids have been shown both experimentally and by simulation to maximize efficiency.[3] The cell length, A, is fixed at 10 cm, taken to be the smallest size reasonable for integration into a large-area module. The bus bar width, d, is fixed at 1.5 mm, a minimum reasonable size for automated stringing. The maximum bus bar sheet resistance is taken to be 0.14 mΩ/□, consistent with 13 μm (0.5 mil) Cu ribbon. B, one half the cell width, and S, the distance between grid fingers, are optimized to minimize power losses.
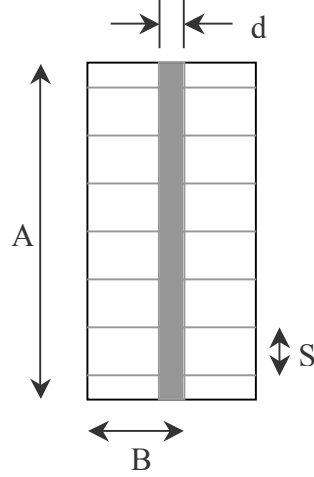
Figure 3: Cell geometry used for analysis of large-area device.

The TCO properties, not just the cell dimensions, must also be optimized for the larger geometry to achieve the highest efficiency. It is assumed for this optimization that the mobility of the TCO is approximately fixed, since the mobility is a function of scattering mechanisms that may not be mutable for a given process or material. The free carrier density, however, is easily varied via oxygen vacancies or dopants in the target. For example, in ZnO films at NREL, changing the Al-doping from 0 to 2% by weight caused a 20x increase in carrier density, but only a 2x decrease in mobility.[4]

Effects of changing the free carrier density on power loss in the device can be calculated using classical harmonic oscillator theory,[5,6] dictating that the absorption in the TCO is related to conduction following

$$\alpha = \frac{q^3 (377 \ ohms)}{\omega^2 m^2 \sqrt{\varepsilon_\infty}} \frac{n}{\mu} \tag{2}$$

$$\sigma = q\mu n \tag{3}$$

$$A = 1 - e^{-\alpha t} \tag{4}$$

where α = absorption coefficient

       σ = conductivity

       A = absorption

       q = electron charge

       μ = mobility

       n = carrier concentration

       ω = angular frequency of light

       m = carrier mass

       ε_∞ = high frequency dielectric constant

       t = film thickness

This theory predicts a linear relationship between ln(1-A) and tn/μ, as is demonstrated in Figure 4 for ZnO films made at NREL. In Figure 4, absorption is measured at 1.1 eV, and Al doping of the films ranges from 0 to 2% by weight. The

comparison between experiment and theory should be considered approximate, as no attempt to account for reflection from the back surface of the film (ZnO/glass interface) has been made.
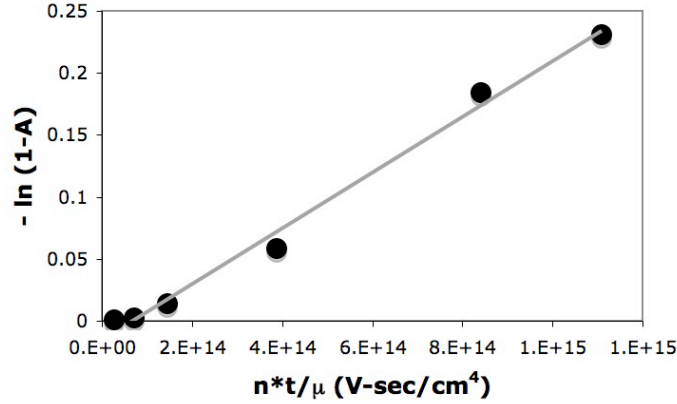

Figure 4: Absorption at 1.1 eV as a function of carrier density, thickness, and mobility measured on NREL ZnO films. The gray line is a linear regression to the data.

Thus, using the material properties of Table 1, the values for B, S, and nt product were adjusted to minimize power loss in the hypothetical large-area device of Figure 3. This minimization was accomplished numerically using a spreadsheet. Resulting parameters are B= 2.0 cm, S=1.1 mm, and nt=2.3 x 10^{15} cm^{-2}. Calculated power losses for this configuration are shown in column 3 of Table 2. Power losses not related to the grids and TCO are assumed to be identical to the 20% small cell. Using the best proven material properties, the highest possible large-area efficiency is thus 19.1%. Alternatively, if the cell width is fixed at 10 cm (i.e. B=5 cm), optimized values are S=0.61 mm and nt=1.3 x 10^{15} cm^{-2}, with a resulting efficiency of 18.1%. The power losses for this configuration are listed in column 4 of Table 2. The 1 to 2% absolute efficiency difference between the small cell and large cell is consistent with published data and modeling.[3]

The 18 to 19% efficient large-area prediction is based upon a minimum finger width of grids deposited by e-beam evaporation. Other deposition techniques may necessitate substantially thicker grids. The maximum achievable large-area efficiency is strongly dependent on minimum grid finger width. As grid fingers are made thicker, they must be spaced further apart, resistive loss in the TCO increases, and the optimized TCO is less transmissive. This effect is illustrated in Figure 5, where optimized efficiency and grid spacing are calculated for a 10 cm wide device. To achieve a module efficiency of 15%, the maximum grid finger width is about 1 mm.
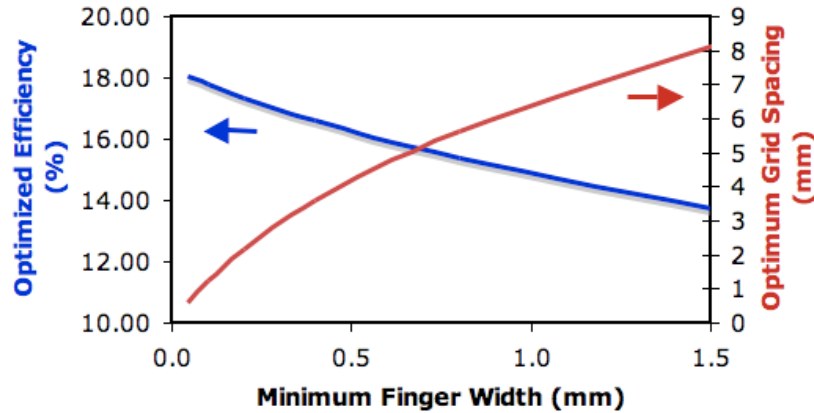

Figure 5: Calculated maximum large-area efficiency as a function of grid finger width. Also shown are the effects of grid finger width on optimum grid spacing.

Table 2: Optical and resistive losses in optimized devices of varying areas, calculated assuming best proven material properties.

Mechanism	NREL 20% small cell losses (mW/cm^2)	Optimized large area cell (mW/cm^2)	Cell width fixed at 10 cm (mW/cm^2)
Grid shading	0.71	0.85	1.49
Grid lateral resistance	0.08	0.32	1.17
Grid contact resistance	0.14	0.12	0.07
TCO resistance	0.24	0.21	0.12
TCO absorption	0.25	0.21	0.12
Bus bar resistance	0.13	0.14	0.36
Bus bar shading	0.13	0.75	0.30
Reflection	1.4	1.4	1.4
Total:	3.1	4.0	5.0
Efficiency (%):	20.0	19.1	18.1

3. CdS

The function of the bath-deposited CdS layer has been described not just as a heterojunction partner, but also in terms of band alignment,[7] lattice matching,[8] surface cleaning,[9,10] and formation of a buried heterojunction via Cd doping of the CIGS.[10,11,12,13,14] It is assumed in this analysis that the CdS deposition conditions allow enough time for adequate surface cleaning and any CIGS doping that might occur. Therefore, the remaining CdS property available for optimization is the CdS thickness.

Device performance as a function of CdS deposition time (i.e. thickness) has been examined at NREL.[15] From this study, Figure 6 shows open-circuit voltage (Voc), fill factor (ff), and current collection below 520 nm (from integrated quantum efficiency measurements) as a function of deposition time. Open circuit voltage and fill factor first increase with CdS deposition time then saturate. Current below 520 nm, on the other hand, decreases steadily as absorption in the CdS increases.

The decrease in current with increasing CdS thickness is well-described by integrating the AM1.5 spectrum times the CdS absorption calculated using published optical constants. To perform this calculation of the CdS absorption, a CdS thickness is assigned to each data point from Figure 6 based on the measured quantum efficiency (QE). Assuming that the ratio of the QE at 520 nm (QE_{520}) to that at 450 nm (QE_{450})is controlled by the transmission through the CdS, the thickness t of the CdS is given by

$$t = \frac{\ln(QE_{450}/QE_{520})}{(\alpha_{520} - \alpha_{450})} \tag{5}$$

where α_{450} and α_{520} are the absorption coefficients at 450 and 520 nm, respectively, as available in published data.[16]

Using CdS thickness extracted by this method, the data of Figure 6 are used to graph device efficiency as a function of CdS thickness, and are shown in Figure 7. Points are measured data, while the dashed line shows the expected dependency at higher thicknesses due to absorption in the CdS. To keep losses from the CdS below 0.5 mW/cm^2, CdS thickness must be 40 nm +40/-10 nm. The fairly gentle decrease in efficiency with increased CdS thickness shown in Figure 7 accounts only for increased absorption in the CdS. In practice, it can be expected that for the largest thicknesses shown in the graph, fill factor decreases will occur due to reduced electric field in the CIGS and the

associated energy position of the CdS/CIGS conduction band offset.[17] The onset of this fill factor reduction is a function of the CdS and i-ZnO thicknesses and carrier densities.
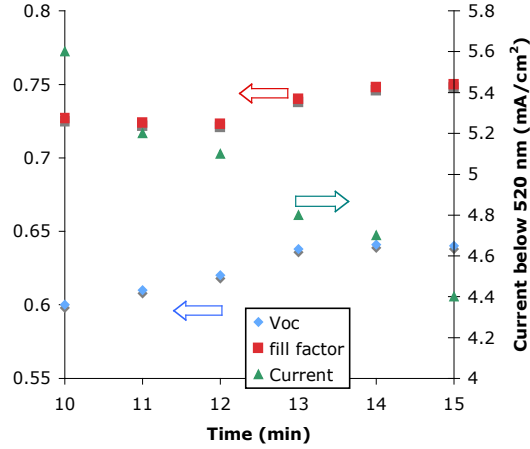

Figure 6: Performance parameters as a function of CdS deposition time (i.e. thickness).
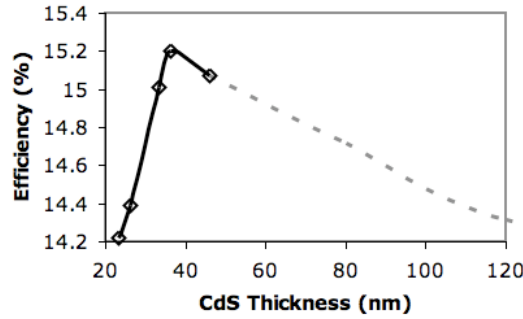

Figure 7: Device efficiency as a function of CdS thickness. Points are measured data, while the dashed line shows the expected dependency at higher thicknesses due to absorption in the CdS.

4. CIGS

CIGS, as the absorber and the depleted semiconductor, is the primary layer in determining junction properties and device performance. Its formation tends to be the chief challenge facing manufacturers, as the highest performing CIGS requires the difficult combination of elevated temperatures, extended deposition times, controlled composition and reaction of four elements, Na doping, and large grain size.

Properties of the CIGS that may change from one film to the next and are expected to affect device performance are band gap (E_g), lifetime (τ), carrier density (p), mobility (μ), and front and rear surface recombination velocities (S_F and S_R). Profiles (gradients) in these properties may occur through the film.

While some of these properties are measured routinely, others are not fully quantified for CIGS. Band gap profile and carrier density profile fall in the more routine category. Band gap profiles are typically deduced from Auger or x-ray photoelectron spectroscopy profiling, and subsequent conversion of the atomic Ga/(In+Ga) ratio to band gap. Carrier densities can be deduced from capacitance-voltage or drive-level capacitance profiling, although the separation of free carrier, interface, and deep-level response can be non-trivial.[18] Lifetime measurements by time-resolved photoluminescence (TRPL) can yield information relevant to device performance,[19,20,21] although only a single value,

rather than a profile, is generally extracted. Some (single-value) measurements of hole mobility in CIGS are available in the literature,[22,23,24] while estimates of the electron mobility are based largely on assumptions regarding the ratio between electron and hole mobilities, or from measurements on single-crystal materials. Little data exists characterizing surface recombination velocities in the CIGS device.

4.1   BAND GAP PROFILE

Band gap profile is one of the most thoroughly characterized and understood properties of the CIGS layer. Numerous publications detail how the band gap profile can be manipulated to match the solar spectrum, decouple optical absorption and voltage, and reduce of the effects of back surface recombination and short diffusion length.[25] In general, the salient features are 1) overall band gap magnitude, 2) single-grading, i.e. increasing the band gap toward the back contact of the device, and 3) double-grading, i.e. creating a "notch" profile that both increases the band gap toward the back and front of the device.

The overall band gap to match the solar spectrum is ideally around 1.4 eV.[26] In practicality, for CIGS, it is presently limited to about 1.15 eV, due to the impact of midgap defects at higher band gaps. The measured band gap profile for the 20.0% device of Figure 1 is shown in Figure 8. In this data, the atomic ratio Ga/(In+Ga) was measured by Auger spectroscopy profiling and converted to band gap (E_g) using constants provided by Alonso.[27] The average band gap is around 1.15 eV.
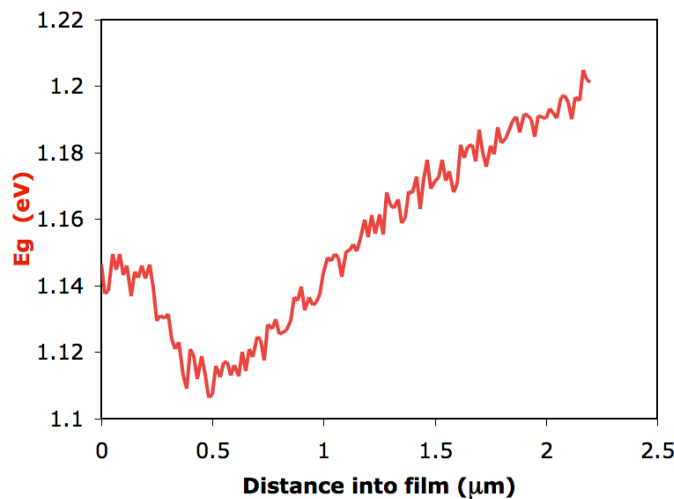

Figure 8: Measured band gap profile of 20.0% device.

A conspicuous feature of Figure 8 is the "notch" in the band gap profile. The measured profile is similar to the optimum identified by modeling efforts,[25,28] although the measured band gap minimum is slightly farther from the sample surface and is slightly more shallow than recommended by the models. Based on modeling, the expected benefits of this profile compared to an ungraded absorber are ~0.5% absolute.[25] Most of this expected benefit is attributed to the grading toward the back of the device, which reduces back surface recombination and assists in collection. The grading toward the front of the device, which to some extent decouples electrical and optical response, makes a smaller contribution to the improvement.

4.2 LIFETIME, CARRIER DENSITY, AND MOBILITY

Lifetime, carrier density, and mobility are logically examined together, as they all occur in a similar fashion in the relationship between forward current and voltage. The forward current density, J_F, in a p-n junction is given by [29]

$$J_F = q \sqrt{\frac{\mu\, kT}{\tau\, q}\, \frac{n_i^2}{p}\, e^{\frac{qV}{kT}} + \frac{qW n_i}{2\tau}\, e^{\frac{qV}{2kT}}} \tag{6}$$

where   q = electron charge

k = Boltzmann constant

T = temperature

μ = electron mobility

τ = electron lifetime

n_i = intrinsic density = $\sqrt{N_C N_V e^{-E_g/kT}}$

N_C = conduction-band density of states

N_V = valence-band density of states

p = hole density

W = depletion width $\cong \sqrt{2\varepsilon V_{bi}/qp}$

ε = dielectric constant

V_{bi} = built-in potential = $E_g - kT\ln(N_V/p)$

V = voltage applied to the junction

The first term in the right hand side of (6) is forward current due to diffusion (J_D), while the second term is forward current due to depletion region recombination (J_R). The equation should only be considered a first-order approximation for transport in CIGS devices, as the calculation neglects the effects of finite absorber thickness and assumes uniform absorber properties. Nevertheless, order of magnitude agreement between voltages and lifetimes using this relationship has been demonstrated,[21] and (6) thus should be a valid vehicle for examining the general trends in expected sensitivity of CIGS device performance to transport parameters.

General trends in the expected impact of μ, τ, and p on device performance can be illustrated by examining the forward current near the maximum power point for several parameter values. For such calculations, μ, τ, and p were varied, while other material parameters were set to baseline values recommended by Gloeckler,[30] apart from the electron and hole effective masses (m_e/m_0 and m_h/m_0, respectively): CIGS m_e/m_0 = 0.09, and CIGS m_h/m_0 = 0.72.[31] The effective masses affect values for band edge densities of states. The lines in Figure 9a show the resulting ratio of the diffusion to recombination current at V= the maximum power voltage V_{mp}. For this exercise, V_{mp} is taken to be 0.591 mV, as in Figure 1. The lines in Figure 9b show the total forward current. Calculations are performed for three values of p and two values of μ, as listed in the figure. The lowest curve (dashed light gray) is calculated using the baseline values for high efficiency devices, p = 2 x 10^{16} cm^{-3} and μ = 100 cm^2/V-sec.[30]
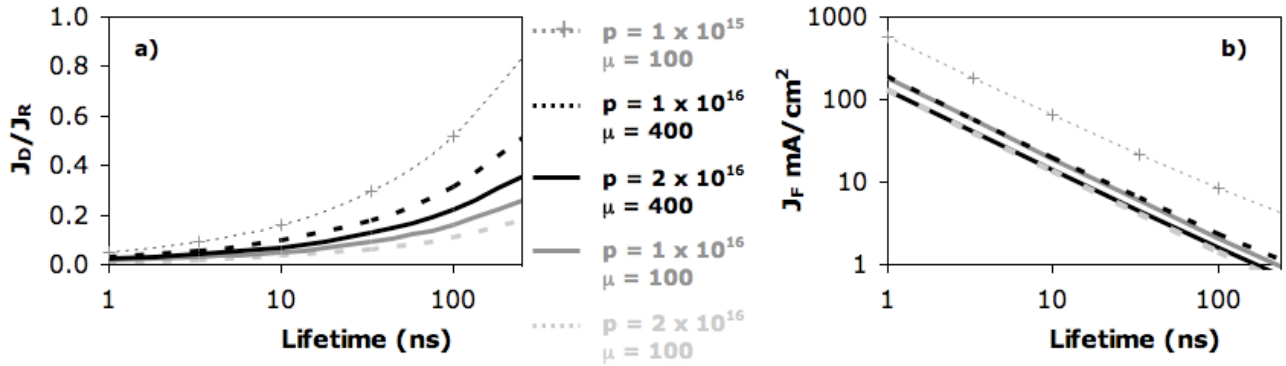

Figure 9: Calculated a) ratio of diffusion current to recombination current, and b) total forward current, as a function of lifetime, for several values of the mobility and carrier density. In the legend, carrier density is listed in cm^{-3}, and mobility as cm^2/V-sec.

For low values of τ, the forward current is dominated by recombination. (i.e. There is a very low value of J_D/J_R in Figure 9a). Even above 10 ns, J_R remains the dominant contribution to J_F, although J_D is non-negligible. The critical task of reducing recombination current to increase efficiency is consistent with recent record efficiencies achieved with

decreasing diode quality factor.[1] Devices measured at NREL whose material properties are consistent with fabrication of >15% modules (i.e. small-area efficiencies ≥17% after application of AR coating) exhibit lifetimes almost exclusively greater than 50 ns. The highest efficiency devices exhibit even longer lifetimes.[20] It should be noted that meaningful comparison of lifetime across studies requires careful control of measurement conditions as described in the references.[19,20]

In Figure 9b, below ~10 ns, the forward current is insensitive to μ, as μ appears only in the prefactor for J_D. , and J_R dominates in this lifetime range. Above ~10 ns, the forward current exhibits some modest dependence on μ (for constant p), as evidenced by the difference between the solid black and dashed gray lines, or between the dashed black and solid gray lines. Measurements for hole mobilities in CIGS range from 0.1 to 20 cm^2/V-sec.[22,23,24] However, little is known about the typical range of electron mobilities in CIGS samples and values required for high performance devices. Because the mobility appears only in the diffusion term of the forward current, it is likely that mobility is of secondary importance compared to lifetime or carrier density. For very high efficiencies, further study of mobility is necessary to comment further on its role in device performance.

For all values of τ, the forward current depends significantly on p, consistent with data in the literature. For small-area devices in the efficiency range of 15 to 18%, a relatively wide range of carrier densities are observed, from around 5 x 10^{15} to 2 x 10^{16} cm^{-3}.[21,24,32,33,34,35] For the devices with efficiencies greater than 19%, however, carrier densities measure over 10^{16} cm^{-3}. Devices with very low carrier density (<10^{15} cm^{-3}) typically exhibit dramatically reduced efficiency (<10%).

4.3   SURFACE RECOMBINATION VELOCITIES

Although recombination at the back surface is recognized as a mechanism for efficiency loss in the CIGS device,[36] little data exists characterizing this quantity. Thus, we are unable to comment here on acceptable ranges or typical values for high efficiency devices.

For high-quality CIGS devices, an upper limit of 10^3 cm/s has been deduced for the bare CIGS surface and the CIGS/CdS interface.[19] Device models predict that a surface recombination velocity of this order of magnitude should have virtually no effect on device performance.

5.   Mo

Primary functions of the Mo layer are to provide a low-resistance back contact, and – in the case of Na-containing substrates- an adequate Na supply for the growing absorber. How well the latter function is performed depends on the Mo thickness and microstructure, and is evident in the absorber lifetime and carrier concentration.

The conductive requirements for the Mo are fairly easily satisfied, since, unlike the case of the TCO, no transmission is needed. Resistive loss in the Mo is calculated as a function of sheet resistance and cell size by standard methods[37] and shown in Figure 10.   The four lines in Figure 10 correspond to four different geometries for connecting to the back contact of the device in Figure 3. For line A (dashed gray), calculations are performed assuming both long edges are contacted with B set at 2.0 cm, as optimized for the TCO. In this geometry, the largest distance any carrier must travel through the Mo is 2.0 cm. For line A, all values of sheet resistance considered – even those substantially above the demonstrated 0.2 $\Omega/\square$ (marked with an arrow) – yield a low power loss. Line B is calculated assuming the same geometry as line A, except only one long edge of the device is contacted. Carriers may travel up to 4 cm in the Mo. Once again power loss is low. Line C is calculated assuming the two short edges of the device are contacted, implying a maximum travel distance of 5 cm. Line D is calculated assuming just one short edge of the device is contacted, implying a maximum travel distance of 10 cm. Only for the largest sheet resistances and maximum travel distances shown does power loss in the Mo exceed 1 mW/cm^2.

The requirements on Mo sheet resistance imposed by Figure 10 apply only to devices on insulating substrates. Conducting substrates, e.g. stainless steel foil, are much thicker than the typical Mo coating, and therefore can carry the necessary current without imposing conductivity requirements on the Mo.
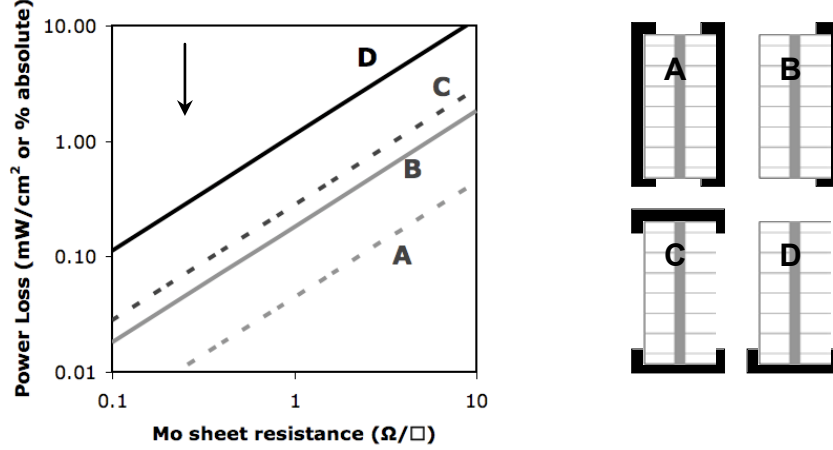
Figure 10: Power loss in the Mo back contact as a function of Mo sheet resistance and geometry. Arrow shows location on graph of demonstrated 0.2 Ω/□ sheet resistance. Schematics on right show geometry used to calculate each line in graph.

6. Impact of Potential Breakthroughs

A number of opportunities exist for technological breakthroughs that may relax the material properties requirements delineated in the sections above. These include larger-bandgap absorbers, non-absorbing heterojunction partners that maintain Voc, improved TCOs, and use of optics.

Improved current collection has been the aim of investigation of both larger band gap heterojunction partners and improved TCO's. In the AM1.5 spectrum, 8 mA/cm^2 of photon current is available below 520 nm, and the optimized CdS layer (Figure 7) absorbs 3 mA/cm^2 of it. Thus, a larger band gap heterojunction partner could allow conversion of 3 mA/cm^2 more current, or approximately 1.8 mW/cm^2 more power. Likewise, a perfect TCO (no absorption, resistance, or reflection) would eliminate the grid and resistive layer losses that are shown, for an optimized module, in column 3 of Table 2. These losses total 4 mW/cm^2 to be gained with the development of a perfect TCO.

Larger bandgap absorbers also provide avenues for potential improvement. In theory, larger band gap materials should yield both a better match of the band gap to the solar spectrum, and lower resistive losses. The efficiency gain due to a better match to the solar spectrum, changing the present ~1.15 eV to the optimum 1.4 eV is estimated at 2.5% absolute.[26] Reduced resistive losses, on the other hand, can be expected to yield about 0.4% absolute efficiency increase. This estimate is produced by repeating the TCO/grid optimization of section 2, using a hypothetical 20.0% efficient wide-band gap device with the same outer dimensions as utilized for the optimized large-area device of Table 2 (4 cm x 10 cm), with V_{mp} = 0.800 V, and J_{mp} = 23.6 mA/cm^2. Presently, however, wide band gap chalcopyrites have not yet achieved the absorber and/or interface quality necessary to realize these benefits.[38]

Use of optics produces some efficiency advantages for CIGS solar cells. It should be noted that optics are a slightly different class of improvements than those already discussed, as they require adding components to the device stack, rather than improving or modifying an existing layer. The use of low concentration (14x) has been demonstrated to improve small-area CIGS device efficiency by 3.6% absolute.[39] Maintaining low resistances is key in achieving this efficiency increase under concentration. Luminescent frequency conversion has been shown to increase short-circuit current.[40,41] In this technique, luminescent dyes absorb blue photons that might otherwise be lost in the CdS or ZnO. The dyes then emit at wavelengths for which the device exhibits a high QE. This technique has been shown to increase short circuit current up to 1.5 mA/cm^2 for CIGS devices[40] (i.e approximately 0.9 mW/cm^2 for a very high-efficiency device). 1.0 mA/cm^2 of this current is due to enhanced blue response, and 0.5 mA/cm^2 due to decreased reflection of a mini-module without antireflective coating.

7. Conclusions

Material properties of each layer in an NREL 20.0%-efficient, small-area, CIGS device have been documented. Based on best proven material properties, 18%-efficient, 100 cm^2 devices suitable for integration into large-area modules are possible. Successful transfer of high efficiencies from small to large areas requires careful attention to minimum grid finger width, optimized cell design, high-quality transparent conductors, and AR coating. For some layers (e.g. CdS, Mo), windows of acceptable material properties for 15% devices are fairly wide. The key challenge in creating 15% large-area modules is likely maintaining long lifetimes (> ~50 ns) and high carrier densities (> ~ 10^{16} cm^{-3}) in the CIGS, particularly in high-throughput processes over large areas. A better understanding of electron mobility in CIGS devices is needed to put firm limits on the required values for lifetime and carrier density. New developments related to high-quality large-bandgap absorbers, non-absorbing heterojunction partners that maintain Voc, improved TCO's, and use of optics have the potential to add a few percent to module efficiency, thus relaxing requirements on the CIGS.

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Relatively high proven efficiencies of CIGS devices are often cited regarding its choice as a semiconductor for photovoltaic manufacturing. Module efficiency is an important parameter, as a number of factors in the cost per watt are driven downward by increasing efficiency. Some of these factors include materials costs, throughput for a given capital investment, and installation costs. Thus, realizing high-efficiency (e.g. 15%) large-area CIGS modules is key in both reducing cost per watt and differentiating the technology from other thin films. This paper discusses the material properties required for each layer of the CIGS device such that large-area CIGS modules can achieve efficiencies of >15%, substantially higher than the current industrial state of the art. The sensitivity of module performance to the important material parameters is quantified based on both experimental data and modeling. Necessary performance differences between small-area devices and large-area modules imposed by geometry are also quantified. Potential technical breakthroughs that may relax the requirements for each layer are discussed.

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